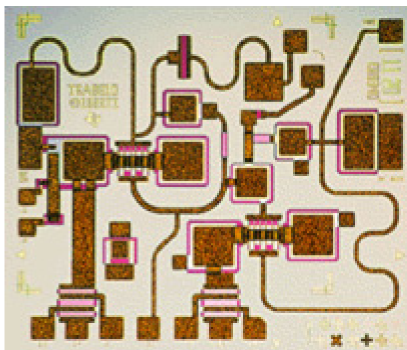
TriQuint SEMICONDUCTOR®

Product Datasheet

April 3, 2007

2-10 GHz Gain Block Amplifier TGA8810-SCC



Key Features and Performance

- 2 to 10-GHz Frequency Range
- Operates from Single 5-V Supply
- Unconditionally Stable
- 17-dB Typical Gain
- Typical ± 0.6-dB Gain Flatness
- 1,8796 x 1,6510 x 0,1524 mm
  (0.074 x 0.065 x 0.006 in.)

The TriQuint TGA8810-SCC is a self-biased general purpose amplifier. Two gain stages employ shunt feedback to produce flat gain to 10-GHz. Output power at 1-dB gain compression is typically 17-dBm and noise figure is 6-dB. The TGA8810-SCC uses on-chip DC blocks to allow direct cascading. Three different on-chip self-bias resistors provide the flexibility of selecting bias current and RF performance.

The TGA8810-SCC is available in chip form and is readily assembled using automated equipment. Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic wire-bonding processes.

TABLE I
MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE
V^+	POSITIVE SUPPLY VOLTAGE V_{D1}, V_{D2}	8.5 V
I^-	NEGATIVE SUPPLY CURRENT	-2.91mA
P_D	POWER DISSIPATION AT (OR BELOW) 25°C BASE-PLATE TEMPERATURE *	2.4 W
T_{CH} **	OPERATING CHANNEL TEMPERATURE	150 ^{0}C
T_M	MOUNTING TEMPERATURE (30 SECONDS)	320 ^{0}C
T_{STG}	STORAGE TEMPERATURE	-65 to 150 ^{0}C

Ratings over channel temperature range, T_{CH} (unless otherwise noted)

Stresses beyond those listed under "Maximum Ratings" may cause permanent damage to the device.
These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "RF Characteristics" is not implied. Exposure to maximum rated conditions for extended periods may affect device reliability.

*For operation above 25°C base-plate temperature, derate linearly at the rate of 5mW/°C.
** Operating channel temperature, T_{CH}, directly affects the device MTTF. For maximum life, it is recommended that channel temperature be maintained at the lowest possible level.

TABLE II
DC SPECIFICATIONS (100%)
(T_A = 25 °C ± 5 °C)

NOTES	SYMBOL	TEST CONDITIONS 2/	LIMITS		UNITS
			MIN	MAX	
	I_{DSS1}	STD	50	150	mA
	I_{DSS2}	STD	50	150	mA
	G_{M1}	STD	70	140	mS
	G_{M2}	STD	70	140	mS
1/,3/	$\|V_{P1}\|$	STD	0.5	2.3	V
1/,3/	$\|V_{P2}\|$	STD	0.5	2.3	V
1/,3/	$\|V_{BVGD1}\|$	STD	6	30	V
1/,3/	$\|V_{BVGD2}\|$	STD	6	30	V
1/,3/	$\|V_{BVGS1}\|$	STD	6	30	V

1/ V_P, V_{BVGD}, and V_{BVGS} are negative.

2/ The measurement conditions are subject to change at the manufacture's discretion (with appropriate notification to the buyer).

3/ STD refers to Standard Test Conditions, see Table IV.

TABLE III
RF SPECIFICATIONS
(T_A = 25°C ± 5°C)

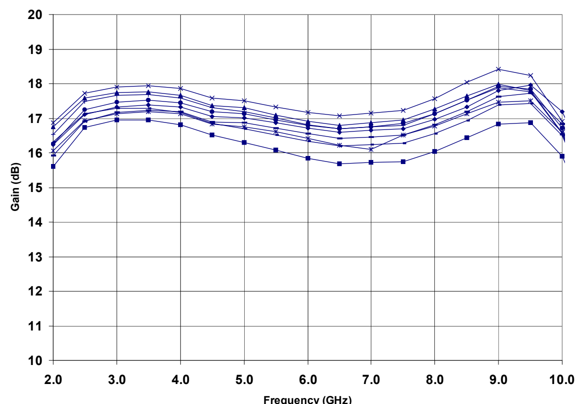
TEST	MEASUREMENT CONDITIONS V^+ = 5V, I^+ = 60mA Self Bias	VALUE			UNITS
		MIN	TYP	MAX	
SMALL-SIGNAL GAIN MAGNITUDE	F = 2 – 10 GHz	14	17		dB
INPUT STANDING WAVE RATIO	F = 2 – 10 GHz		1.9:1		
OUTPUT STANDING WAVE RATIO	F = 2 – 10 GHz		1.2:1		
SMALL-SIGNAL GAIN RIPPLE	F = 2 – 10 GHz		± 0.6	3.0	dB
POWER OUTPUT AT 1 dB GAIN COMPRESSION	F = 2 – 10 GHz	13	17		dBm
NOISE FIGURE	F = 2 – 10 GHz		6	7.5	dB
INPUT RETURN LOSS MAGNITUDE	F = 2 GHz	7			dB
	F = 2.5 – 9 GHz	8			dB
	F = 9.5 GHz	4			dB
	F = 10 GHz	2			dB
OUTPUT RETURN LOSS MAGNITUDE	F = 2 – 2.5 GHz	9			dB
	F = 3 – 5.5 GHz	7.5			dB
	F = 6 – 10 GHz	9			dB
OUTPUT THIRD ORDER INTERCEPT	F = 2 GHz		24		dBm
	F = 5 GHz		26		dBm
	F = 8 GHz		25		dBm
GAIN TEMPERATURE COEFFICIENT (T_{BP} = -40°C to 90°C)	F = 2 GHz		-0.01		dB/°C
	F = 6 GHz		-0.02		dB/°C
	F = 10 GHz		-0.02		dB/°C

TABLE IV
AUTOPROBE FET PARAMETER MEASUREMENT CONDITONS

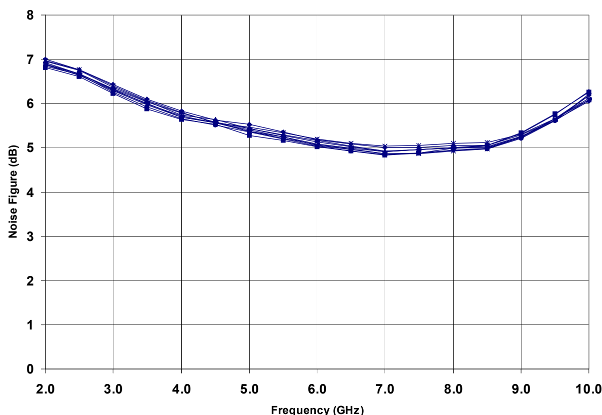
FET Parameters	Test Conditions
I_{DSS} : Maximum drain current (I_{DS}) with gate voltage (V_{GS}) at zero volts.	V_{GS} = 0.0 V, drain voltage (V_{DS}) is swept from 0.5 V up to a maximum of 3.5 V in search of the maximum value of I_{DS}; voltage for I_{DSS} is recorded as VDSP.
G_m : Transconductance; $\frac{(I_{DSS} - IDS1)}{VG1}$	For all material types, V_{DS} is swept between 0.5 V and VDSP in search of the maximum value of I_{ds}. This maximum I_{DS} is recorded as IDS1. For Intermediate and Power material, IDS1 is measured at V_{GS} = VG1 = -0.5 V. For Low Noise, HFET and pHEMT material, V_{GS} = VG1 = -0.25 V. For LNBECOLC, use V_{GS} = VG1 = -0.10 V.
V_P : Pinch-Off Voltage; V_{GS} for I_{DS} = 0.5 mA/mm of gate width.	V_{DS} fixed at 2.0 V, V_{GS} is swept to bring I_{DS} to 0.5 mA/mm.
V_{BVGD} : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I_{BD}) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V_{GD}) measured is V_{BVGD} and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V_{BVGS} : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I_{BS}) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V_{GS}) measured is V_{BVGS} and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.

TGA8810 - Fixture Data Summary
V+=5V, Self Biased, Ta=25C

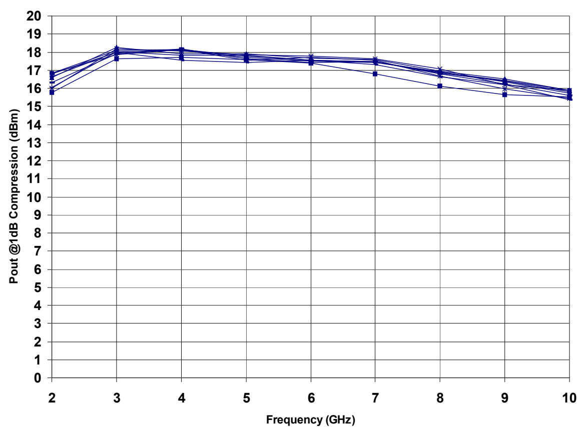
s21



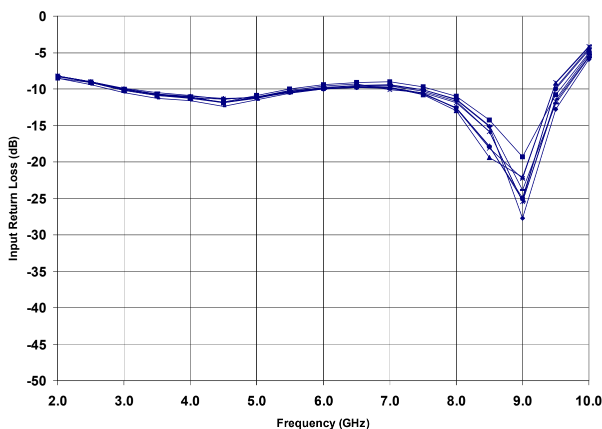
Noise Figure



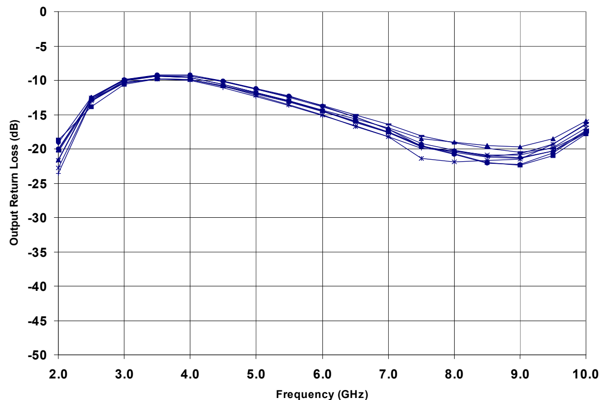
P1dB



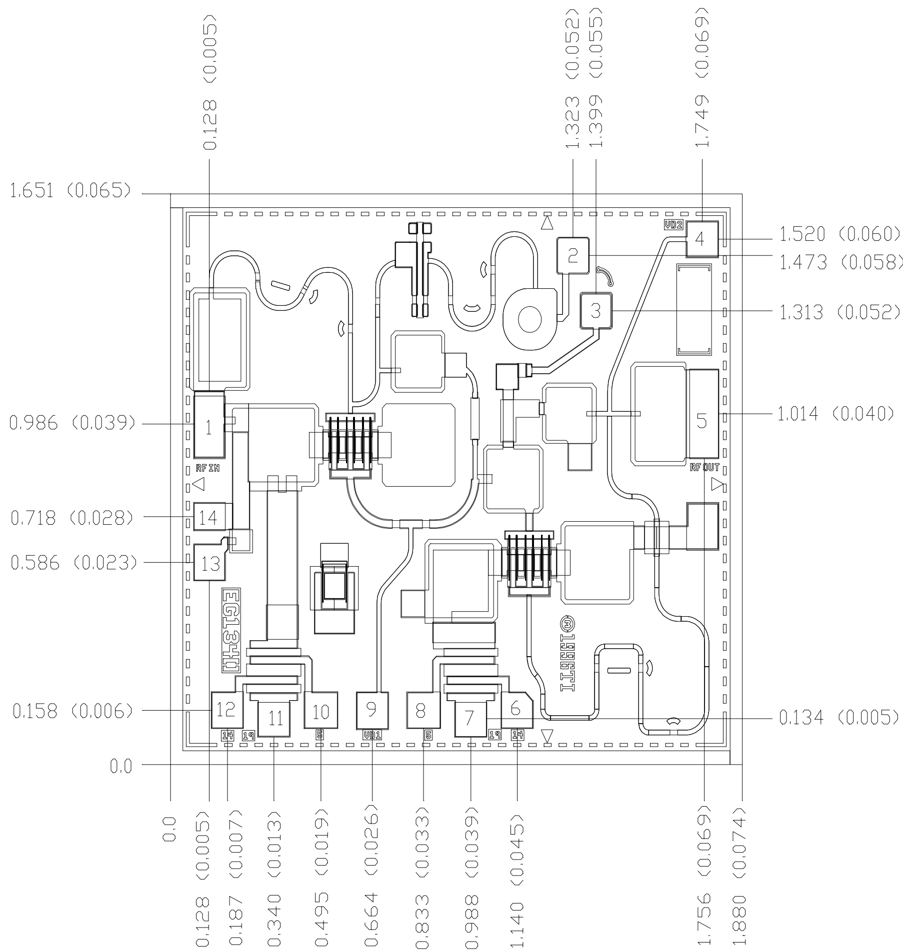
s11



s22



Mechanical Characteristics



Units: millimeters (inches)
Thickness: 0.1524 (0.006) (reference only)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/-0.0508 (0.002)

Bond pad #1 (RF Input)	0.0996 x 0.1905 (0.0039 x 0.0075)
Bond pad #2	0.1016 x 0.1016 (0.0040 x 0.0040)
Bond pad #3	0.1016 x 0.1016 (0.0040 x 0.0040)
Bond pad #4 (VD2)	0.1016 x 0.1016 (0.0040 x 0.0040)
Bond pad #5 (RF Output)	0.0965 x 0.2591 (0.0038 x 0.0102)
Bond pad #6 (Rs22)	0.1016 x 0.1016 (0.0040 x 0.0040)
Bond pad #7 (Rs23)	0.1016 x 0.0787 (0.0040 x 0.0031)
Bond pad #8 (Rs21)	0.1067 x 0.1016 (0.0042 x 0.0040)
Bond pad #9 (VD1)	0.1016 x 0.1041 (0.0040 x 0.0041)
Bond pad #10 (Rs11)	0.1067 x 0.1016 (0.0042 x 0.0040)
Bond pad #11 (Rs13)	0.1016 x 0.0787 (0.0040 x 0.0031)
Bond pad #12 (Rs12)	0.1016 x 0.1016 (0.0040 x 0.0040)
Bond pad #13 (C2)	0.0762 x 0.0762 (0.0030 x 0.0030)
Bond pad #14 (C1)	0.0762 x 0.0762 (0.0030 x 0.0030)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Chip Assembly and Bonding Diagram

RF connections: bond using two 1-mil diameter, 20 to 25-mil-length gold bond wires at both RF Input and RF Output for optimum RF performance.

Close placement of external components is essential to stability

Bond using 0.7-mil diameter wires on bond pads 7, 11, 13, and 14 since they are less than the .004 x .004 needed for 1-mil diameter wire.

One on-chip to on-chip wire bonds 2 and 3.

Refer to TriQuint Semiconductor Gallium Arsenide Products Designers' Information on TriQuint's website or order literature number GMNA002.

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Typical S-Parameters

Frequenc (GHz)	S_{11} MAG	S_{11} ANG(°)	S_{21} MAG	S_{21} ANG(°)	S_{12} MAG	S_{12} ANG(°)	S_{22} MAG	S_{22} ANG(°)	GAIN (dB)
0.5	0.38	-104	0.03	-148	0.001	-13	0.92	-130	-30.8
1.0	0.29	-125	0.99	-177	0.003	180	0.79	165	-0.1
1.5	0.36	-134	4.24	114	0.009	122	0.48	111	12.5
2.0	0.40	-156	6.88	42	0.011	72	0.07	125	16.8
2.5	0.36	-169	7.49	-8	0.009	43	0.21	180	17.5
3.0	0.33	-173	7.58	-45	0.007	27	0.27	164	17.6
3.5	0.31	-175	7.59	-77	0.006	10	0.29	150	17.6
4.0	0.30	-175	7.53	-106	0.004	9	0.28	137	17.5
4.5	0.30	-176	7.36	-133	0.002	5	0.26	126	17.3
5.0	0.29	179	7.10	-157	0.002	2	0.22	115	17.0
5.5	0.31	-178	7.02	179	0.001	-53	0.17	109	16.9
6.0	0.33	179	6.98	156	0.001	-152	0.12	110	16.9
6.5	0.33	173	6.86	134	0.002	-178	0.07	111	16.7
7.0	0.32	166	6.90	113	0.003	169	0.04	120	16.8
7.5	0.29	156	7.01	90	0.004	173	0.02	140	16.9
8.0	0.23	140	7.22	67	0.005	168	0.00	2	17.2
8.5	0.15	110	7.48	43	0.007	177	0.02	0	17.5
9.0	0.11	33	7.75	15	0.009	175	0.03	24	17.8
9.5	0.24	-37	7.87	-15	0.011	170	0.06	52	17.9
10.0	0.44	-75	7.39	-49	0.013	162	0.09	58	17.4
10.5	0.64	-106	6.34	-83	0.016	153	0.11	51	16.0

Thermal Information

Parameter	Test condition	Nom	Unit
$R_{\theta JC}$ Thermal Resistance (channel to backside)	V^+ = 5V, Self Biased, Ta=25°C	60	°C/W

Reflow process assembly notes:

- AuSn (80/20) solder with limited exposure to temperatures at or above 300▪C
- alloy station or conveyor furnace with reducing atmosphere
- no fluxes should be utilized
- coefficient of thermal expansion matching is critical for long-term reliability
- storage in dry nitrogen atmosphere

Component placement and adhesive attachment assembly notes:

- vacuum pencils and/or vacuum collets preferred method of pick up
- avoidance of air bridges during placement
- force impact critical during auto placement
- organic attachment can be used in low-power applications
- curing should be done in a convection oven; proper exhaust is a safety concern
- microwave or radiant curing should not be used because of differential heating
- coefficient of thermal expansion matching is critical

Interconnect process assembly notes:

- thermosonic ball bonding is the preferred interconnect technique
- force, time, and ultrasonics are critical parameters
- aluminum wire should not be used
- discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- maximum stage temperature: 200▪C

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