

## L-BAND SPDT SWITCH

### DESCRIPTION

$\mu$ PG132G is an L-Band SPDT (Single Pole Double Throw) GaAs FET switch which was developed for digital cellular or cordless telephone application.

The device can operate from 100 MHz to 2.5 GHz, having the low insertion loss.

It housed in an original 8 pin SSOP that is smaller than usual 8 pin SOP and easy to install and contributes to miniaturizing the system.

It can be used in wide-band switching applications.

### FEATURES

- Maximum transmission power : 0.6 W (typ.)
- Low insertion loss : 0.6 dB (typ.) at  $f = 2$  GHz
- High switching speed : 30 ns
- +3 V/0 V control voltage
- Small package : 8 pins SSOP

### APPLICATION

- Digital cordless telephone : PHS, PCS, DECT etc.
- Digital hand-held cellular phone, WLAN

### ORDERING INFORMATION

PART NUMBER	PACKAGE	PACKING FORM
$\mu$ PG132G-E1	8 pin plastic SSOP	Carrier tape width 12 mm. QTY 2kp/Reel.

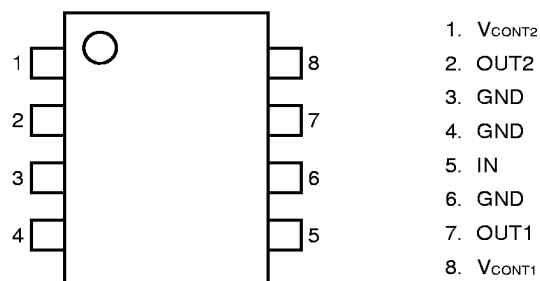
For evaluation sample order, please contact your local NEC sales office.

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C)

Control Voltage	$V_{CONT}$	-0.6 to +6	V
Input Power	$P_{in}$	31	dBm
Total Power Dissipation	$P_{tot}$	0.4	W
Operating Case Temperature	$T_{opt}$	-65 to +90	°C
Storage Temperature	$T_{stg}$	-65 to +150	°C

**CAUTION:** The IC must be handled with care to prevent static discharge because its circuit is composed of GaAs MES FET.

## PIN CONNECTION DIAGRAM (Top View)

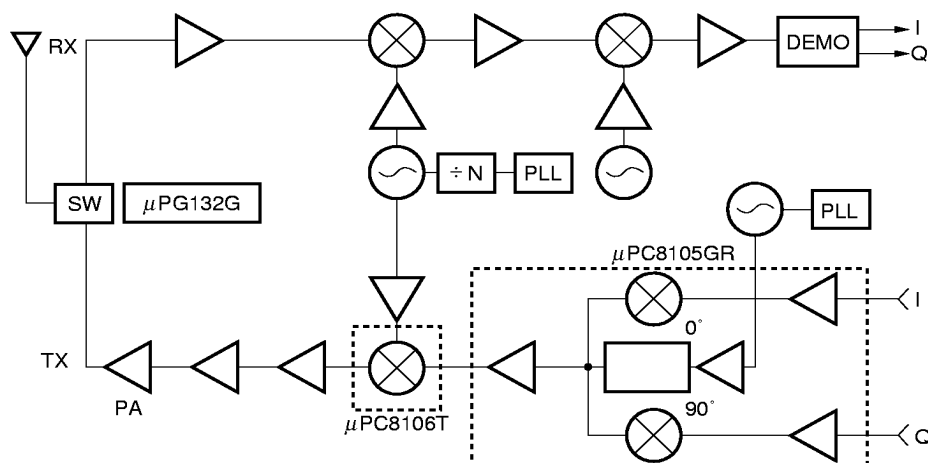


## SPDT SWITCH IC SERIES PRODUCTS

PART NUMBER	P <sub>in</sub> (1dB) (dBm)	L <sub>INS</sub> (dB)	ISL (dB)	V <sub>CONT</sub> (V)	PACKAGE	APPLICATIONS
$\mu$ PG130GR	+34	0.5 @1G	32 @1G	-5/0	8 pin SOP (225 mil)	PDC, IS-136, PHS
$\mu$ PG131GR	+30	0.6 @2G	23 @2G	-4/0		PHS, PCS, WLAN
$\mu$ PG130G	+34	0.5 @1G	32 @1G	-5/0	8 pin SSOP (175 mil)	PDC, IS-136, PHS
$\mu$ PG131G	+30	0.6 @2G	23 @2G	-4/0		PHS, PCS, WLAN
$\mu$ PG132G	+30	0.6 @1G	22 @2G	+3/0		PHS, PCS, WLAN
$\mu$ PG133G	+25	0.6 @2G	20 @2G	-3/0		DIVERSITY etc

**Remark:** As for detail information of series products, please refer to each data sheet.

## APPLICATION EXAMPLE (PHS)



## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Control Voltage (ON)	V <sub>CONT</sub>	+2.7	+3.0	+5.0	V
Control Voltage (OFF)	V <sub>CONT</sub>	−0.2	0	+0.2	V
Input Power Level	P <sub>in</sub>		27	29	dBm

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Insertion Loss	L <sub>INS</sub>		0.6	1.0	dB	f = 2.5 GHz
			0.8 <sup>Note1</sup>			
Isolation	ISL	20	22		dB	f = 2.5 GHz
		20 <sup>Note1</sup>				
Input Return Loss	RL <sub>in</sub>	11			dB	f = 100 MHz to 2 GHz
Output Return Loss	RL <sub>out</sub>	11			dB	V <sub>CONT1</sub> = 0 V
Input Power at 1dB Compression Point	P <sub>in</sub> (1dB) <sup>Note2</sup>	27	30		dBm	V <sub>CONT2</sub> = +3 V
						or
Switching Speed	t <sub>sw</sub>		30		ns	V <sub>CONT1</sub> = +3 V
Control Current	I <sub>CONT</sub>			50	μA	V <sub>CONT2</sub> = 0 V

**Notes 1:** Characteristic for reference at 2.0 to 2.5 GHz.

**2:** P<sub>in</sub> (1dB) is measured the input power level when the insertion loss increase more 1dB than that of linear range.

All other characteristics are measured in linear range.

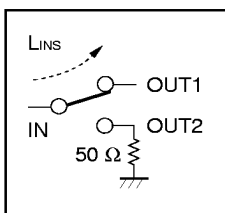
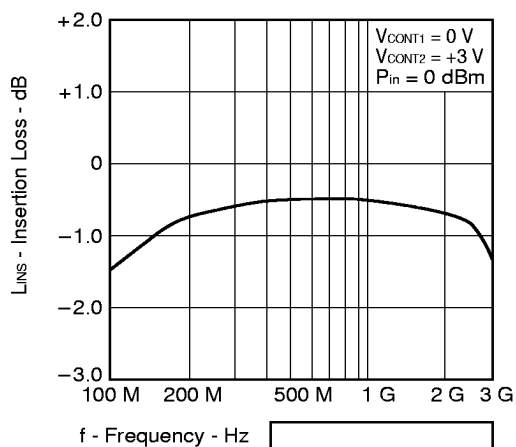
## NOTE ON CORRECT USE

- When the  $\mu$ PG132G is used it is necessary to use DC blocking capacitor for No. 2 pin (OUT2), No. 5 pin (IN) and No. 7 pin (OUT1). The value of DC blocking capacitors should be chosen to accommodate the frequency of operation.
- Insertion loss and isolation of the IN-OUT2 is better than that of IN-OUT1, because No. 7 pin (OUT1) is placed to same side of No. 5 pin (IN).
- The distance between IC's GND pins and ground pattern of substrate should be as shorter as possible to avoid parasitic parameters.

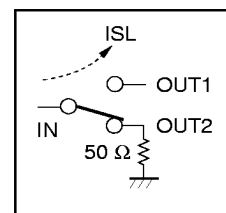
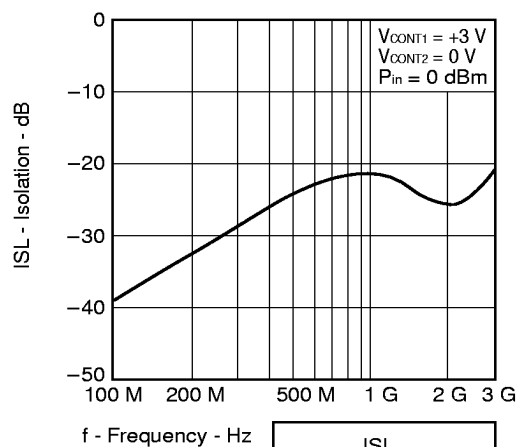
**TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )**

**Note** This data is including loss of the test fixture.

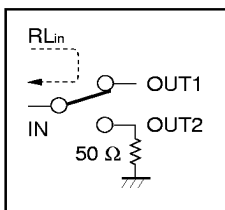
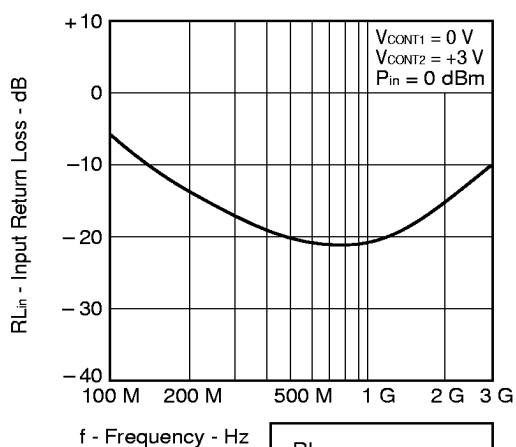
IN-OUT1 INSERTION LOSS vs. FREQUENCY



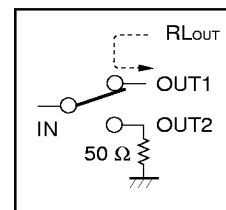
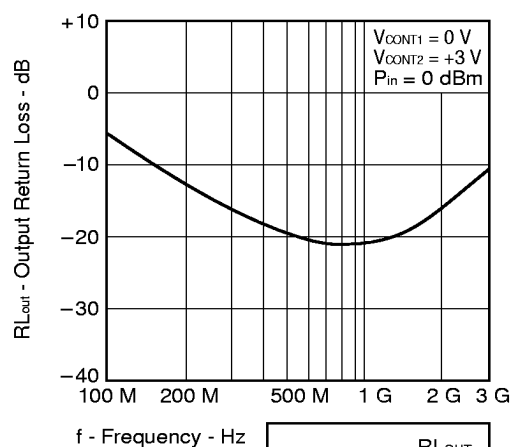
IN-OUT1 ISOLATION vs. FREQUENCY



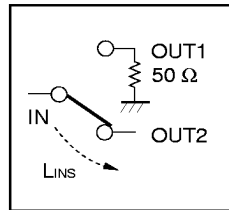
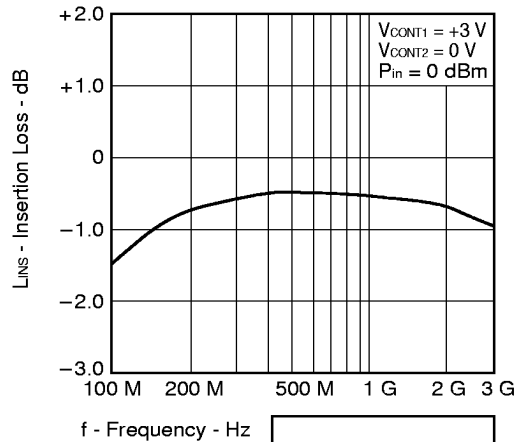
IN-OUT1 INPUT RETURN LOSS vs. FREQUENCY



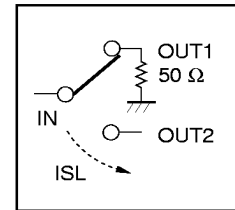
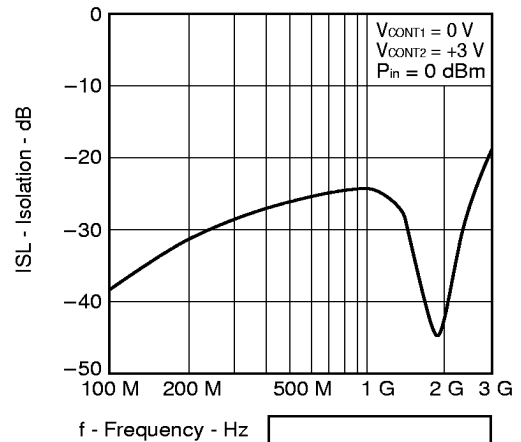
IN-OUT1 OUTPUT RETURN LOSS vs. FREQUENCY



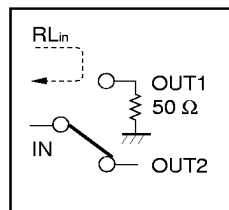
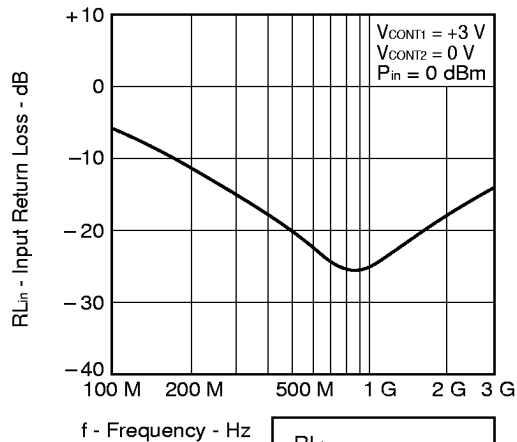
IN-OUT2 INSERTION LOSS vs. FREQUENCY



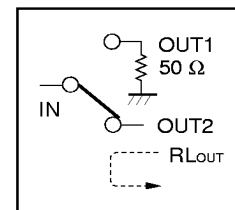
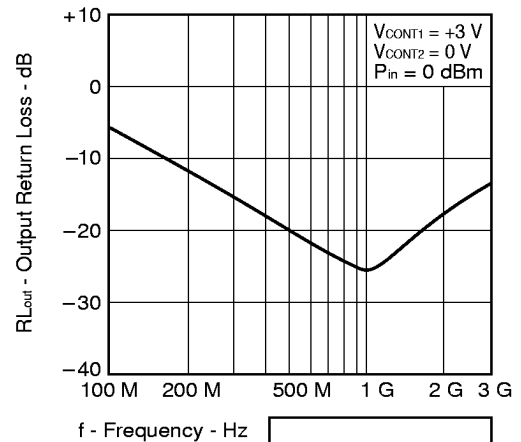
IN-OUT2 ISOLATION vs. FREQUENCY

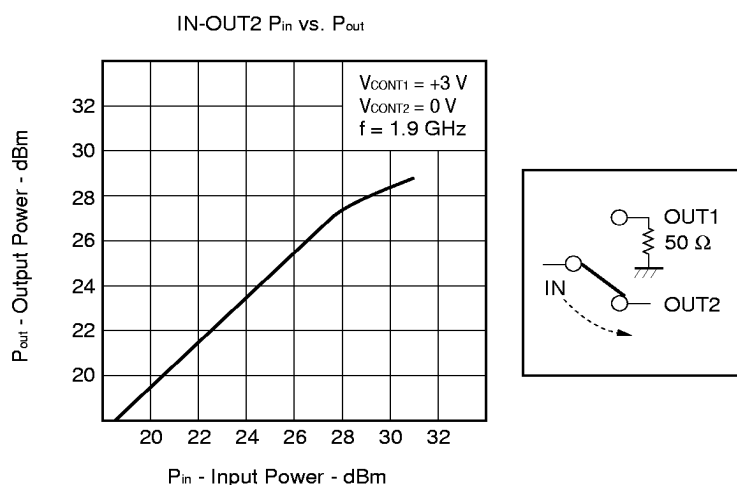


IN-OUT2 INPUT RETURN LOSS vs. FREQUENCY



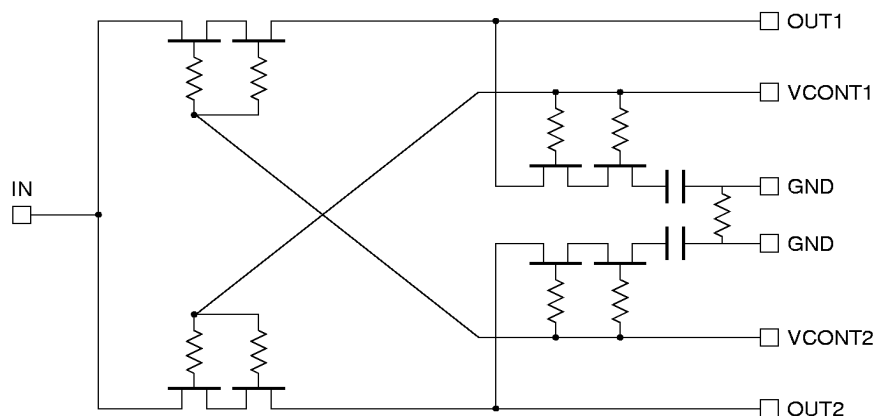
IN-OUT2 OUTPUT RETURN LOSS vs. FREQUENCY



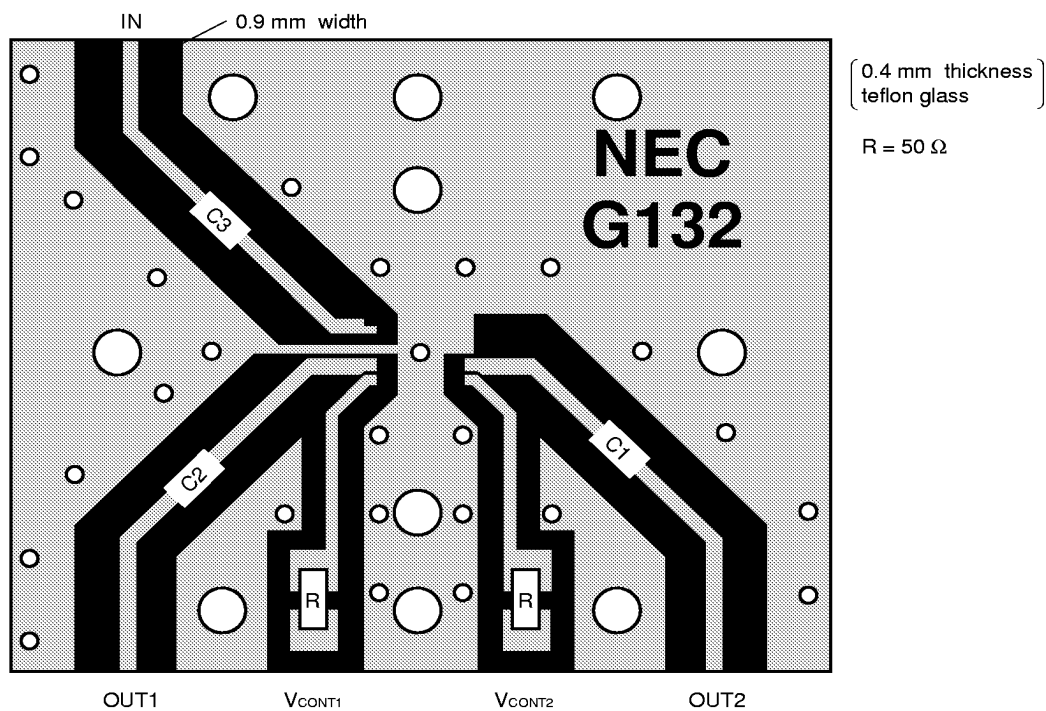


### Internal Equivalent Circuit

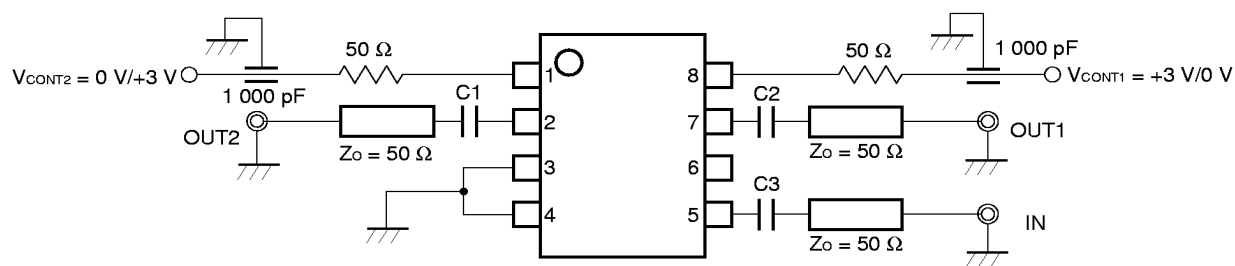
Between the GND pins and FETs of this IC, a capacitor of 3.6 pF for floating is inserted to realize switching between positive voltages of +3 V and 0 V. However, the basic configuration of the  $\mu$ PG132G is the same as that of the  $\mu$ PG131G. In addition, the  $\mu$ PG132G has a monitor pin and a resistor to check the internal circuitry.



# TEST BOARD



# TEST CIRCUIT



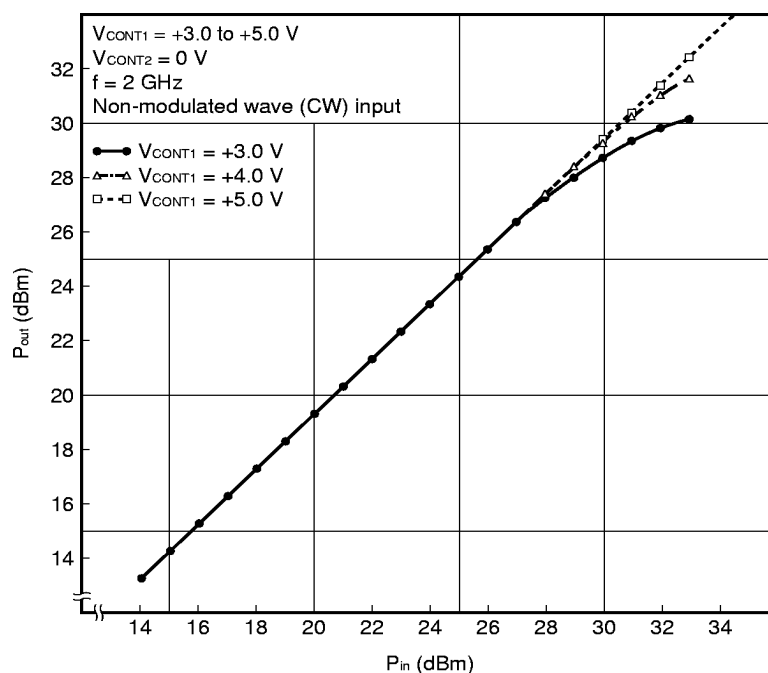
$C1, C2, C3 = 51 \text{ pF}$

## APPLICATIONS

## Dependency on control voltage

The input/output characteristics, insertion loss, and isolation characteristics hardly fluctuate up to  $P_{in}$  (1 dB) = +27 dBm, even if the control voltage is changed in a range of +3.0 V to +5.0 V. When the IC is used at  $P_{in}$  = +22 dBm in a PHS extension, therefore, the characteristics of the IC do not fluctuate even if a battery whose discharging characteristics fluctuate, such as a lithiumion battery, is used.

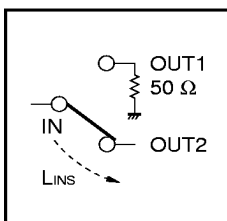
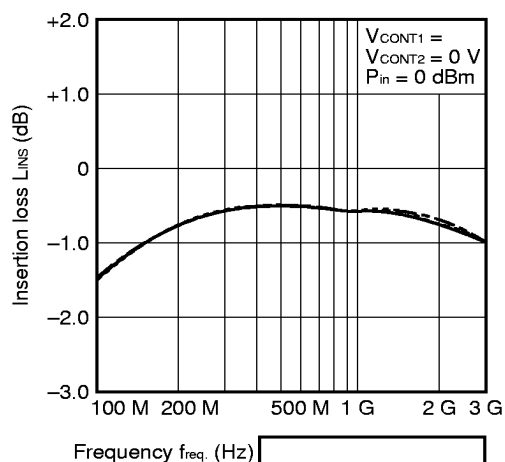
Relation between Control Voltage and Input/Output Characteristics



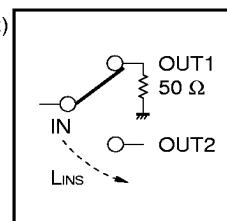
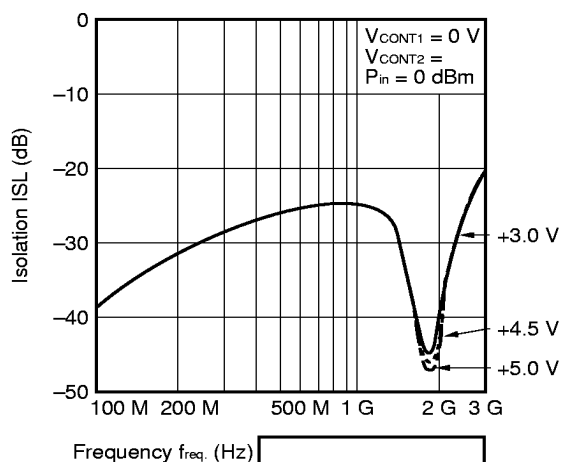


## Relation between Small Signal Characteristics and Control Voltage

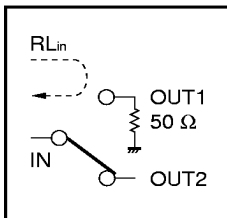
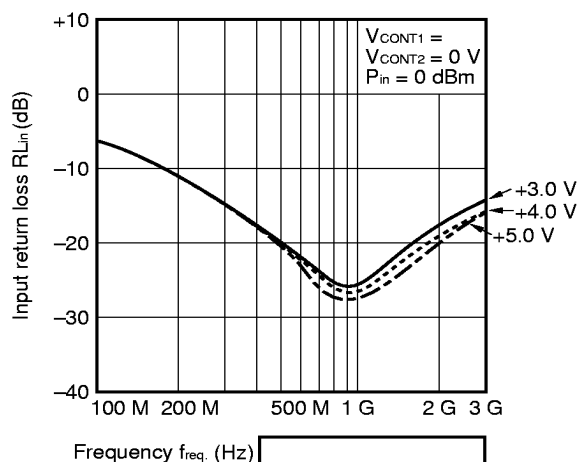
IN-OUT2 INSERTION LOSS vs. FREQUENCY



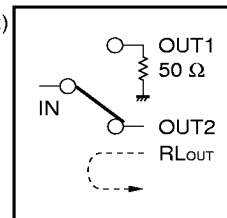
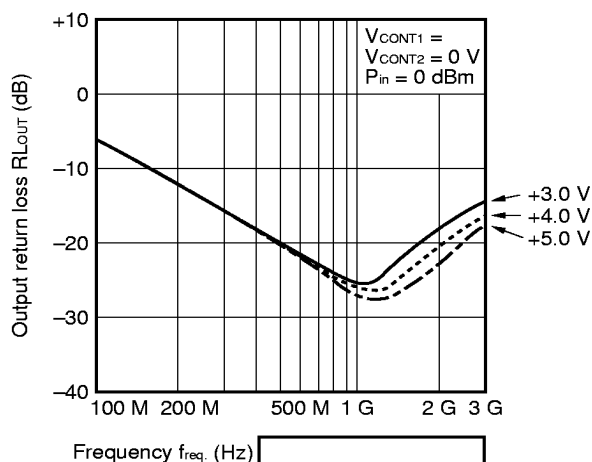
IN-OUT2 ISOLATION vs. FREQUENCY



IN-OUT2 RETURN LOSS vs. FREQUENCY



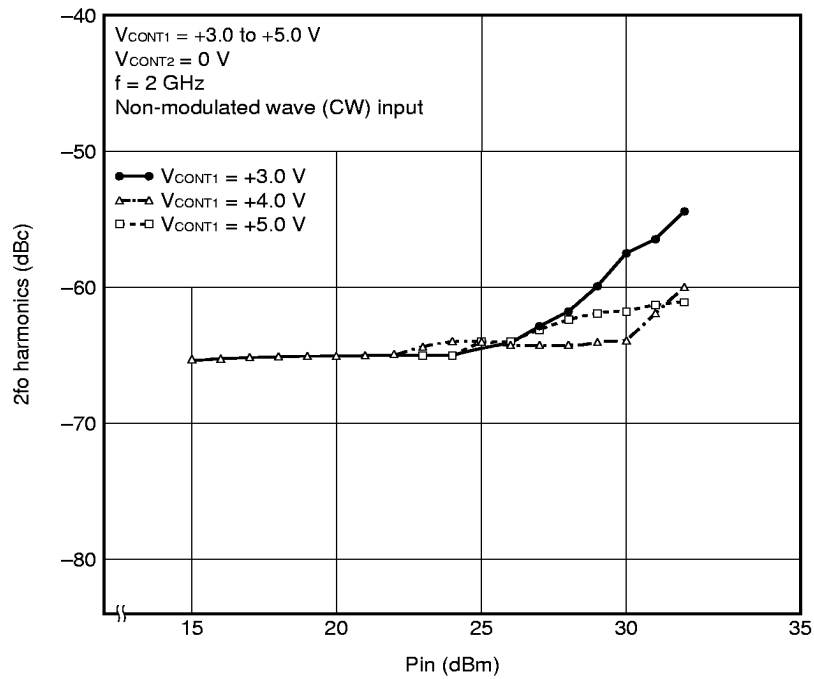
IN-OUT2 OUTPUT RETURN LOSS vs. FREQUENCY



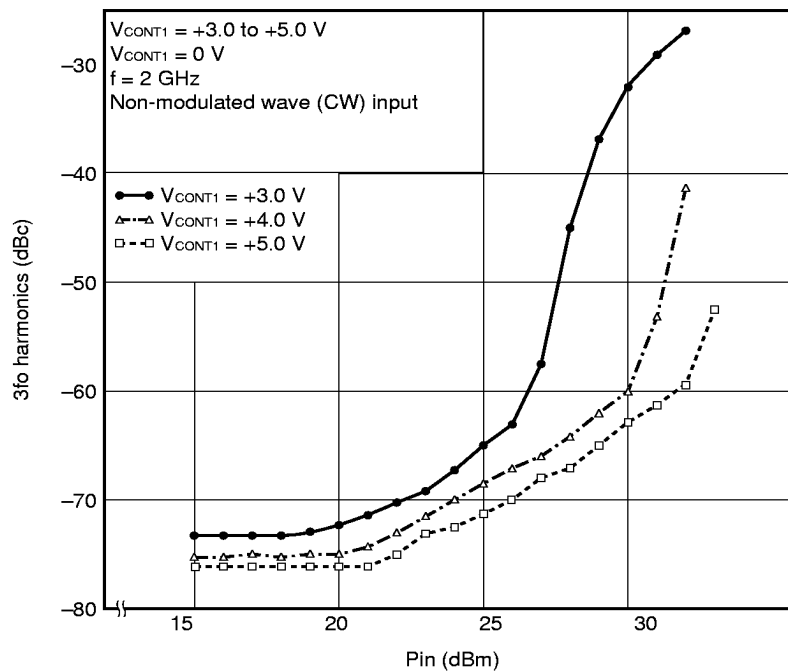
- $V_{CONT1} = +3$  V (isolation only,  $V_{CONT2} = +3$  V)
- $V_{CONT1} = +4$  V (isolation only,  $V_{CONT2} = +4$  V)
- - -  $V_{CONT1} = +5$  V (isolation only,  $V_{CONT2} = +5$  V)

The measured values include all losses of the measuring jig.

Relation between Control Voltage and Second Harmonic



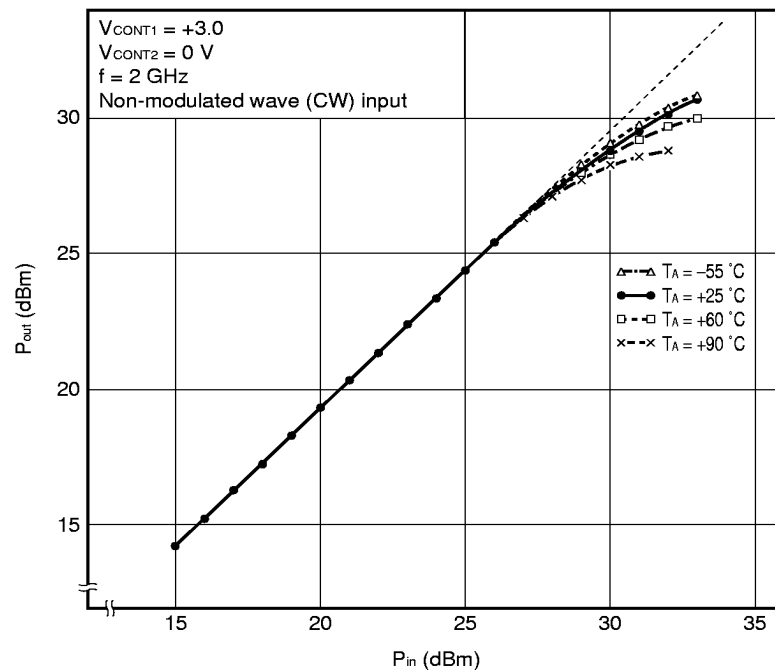
Relation between Control Voltage and Third Harmonic



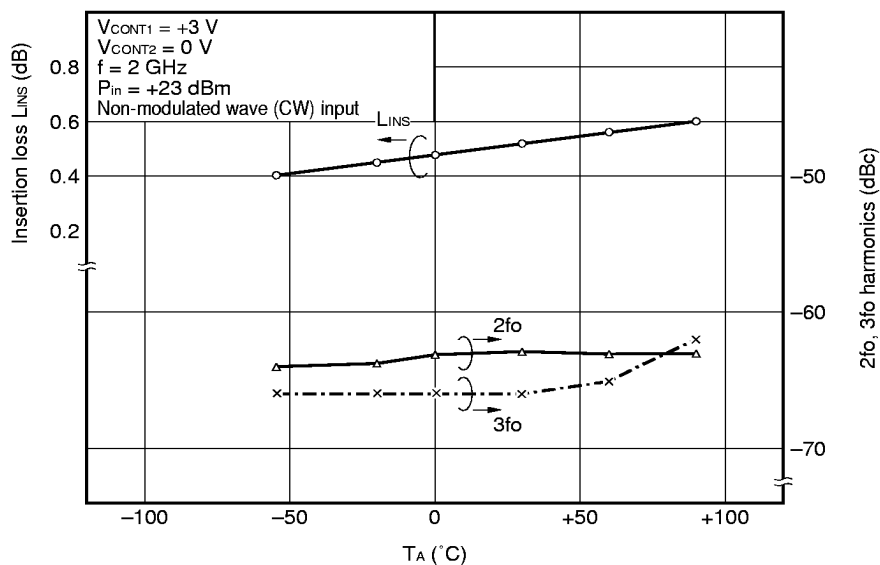
### Temperature characteristics

Next, results from evaluating the temperature characteristics of the  $\mu$ PG132G are shown. As shown, favorable characteristics are obtained in a range of  $T_A = -55$  to  $+90$  °C. The temperature coefficient of the insertion loss is about  $+0.0014$  dB/°C, indicating that the higher the temperature, the more the insertion loss.

### Temperature Characteristics of Input/Output



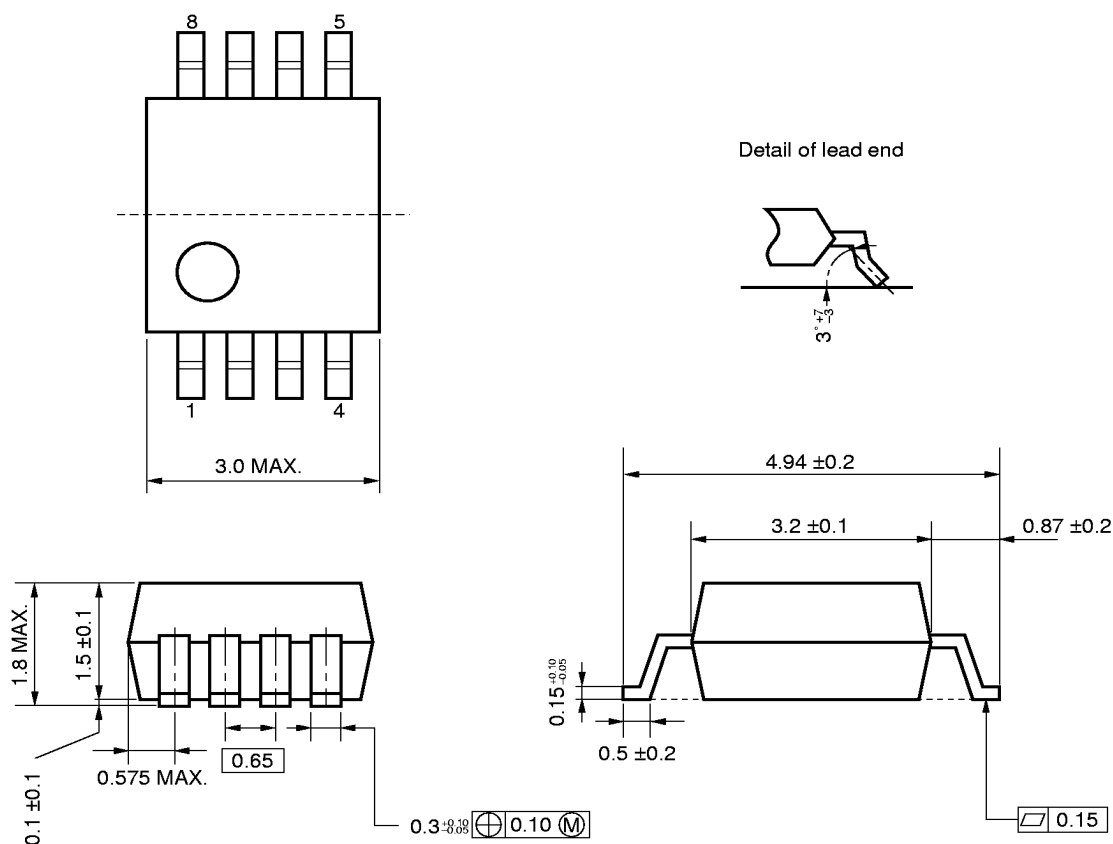
### Temperature Characteristics of Insertion Loss, and Double and Triple Harmonics



μPG132G TRUTH TABLE OF SWITCHING BY CONDITION OF CONTROL VOLTAGE

		V <sub>CONT1</sub>	
		+3 V	0 V
V <sub>CONT2</sub>	+3 V		
	0 V		

8-PIN PLASTIC SHRINK SOP (175 mil) (Unit mm)



**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

[μPG132G]

Soldering process	Soldering conditions	Recommended condition symbol
Infrared ray reflow	Package peak temperature: 230 °C Hour: within 30 s. (more than 210 °C) Time: 2 time, Limited days: no. <b>Note</b>	IR30-00-2
VPS	Package peak temperature: 215 °C Hour: within 40 s. (more than 200 °C), Time: 2 time, Limited days: no. <b>Note</b>	VP15-00-2
Wave Soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no. <b>Note</b>	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 10 s. Limited days: no. <b>Note</b>	

**Note** It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 %, RH.

**Caution** The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535EJ7V0IF00)**.