VG112

PCS/UMTS-band Variable Gain Amplifier

Product Features

- 1800 – 2200 MHz bandwidth
- 25 dB Gain at 1.9 GHz
- 28 dB Attenuation Range
- +46 dBm Output IP3
- +30 dBm P1dB
- Constant IP3 & P1dB over attenuation range
- +5V Single voltage supply
- Pb-free / green / RoHS-compliant 6x6 mm QFN package
- MTTF > 100 years

Applications

- Xmit & Rcv AGC circuitry for mobile infrastructure

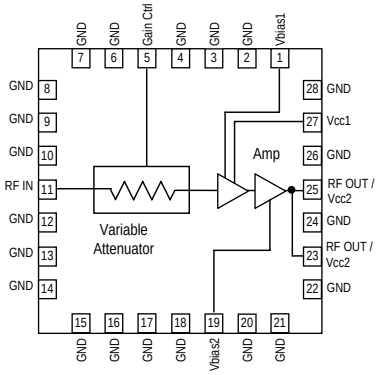
Product Description

The VG112 is a PCS / UMTS-band high dynamic range variable gain amplifier (VGA) housed in a low profile Pb-free / green / RoHS-compliant surface-mount leadless QFN package that measures 6 x 6 mm square.

The +30 dBm output compression point and +46 dBm output intercept point of the amplifier are maintained over the entire attenuation range, making the VG112 ideal for use in transmitter and receiver AGC circuits. The high gain of the dual-stage amplifier allows for more integration in a transceiver board while requiring minimal printed circuit board space.

Superior thermal design allows the product to have a minimum MTTF rating of 100 years at a mounting temperature of +85 ºC. All devices are 100% RF & DC tested and packaged on tape and reel for automated surface-mount assembly.

Functional Diagram



Specifications (1)

Parameter	Units	Min	Typ	Max	Conditions
Operational Bandwidth	MHz	1800		2200	
Test Frequency	MHz		2140		See note 1
Gain at min. attenuation	dB	20.5	23		
Input Return Loss	dB		18		
Output Return Loss	dB		8.2		
Output P1dB	dBm		+30		
Output IP3	dBm	+43	+46		See note 2
Noise Figure at min. attenuation	dB		8		V_{CTRL} = 0 V
Gain Variation Range	dB	23.5	28		See note 3
Gain Variation Control Voltage, V_{CTRL}	V	0		4.5	See note 1
Supply Voltage, V_{CC}	V		+5		
Operating Amplifier Current Range	mA	350	415	475	Pin 25
Gain Control Pin Current	mA			20	V_{CTRL} = 4.5 V. See note 1.

1. Test conditions unless otherwise noted: 25 ºC, Vcc = +5 V in a tuned application circuit. Vctrl is the control voltage through a 220 Ω dropping resistor as shown in the same application circuit.
2. 3OIP measured with two tones at an output power of +15 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.
3. The gain variation range is measured as the difference in gain with Vctrl = 0V and Vctrl = 4.5V at 2.14 GHz.

Absolute Maximum Rating

Parameter	Rating
Storage Temperature	-55 to +125 °C
Thermal Resistance, Rth	33 °C / W
Pin 5 (Gain Control) Current	30 mA
Max. Junction Temperature	+200 °C

Operation of this device above any of these parameters may cause permanent damage.

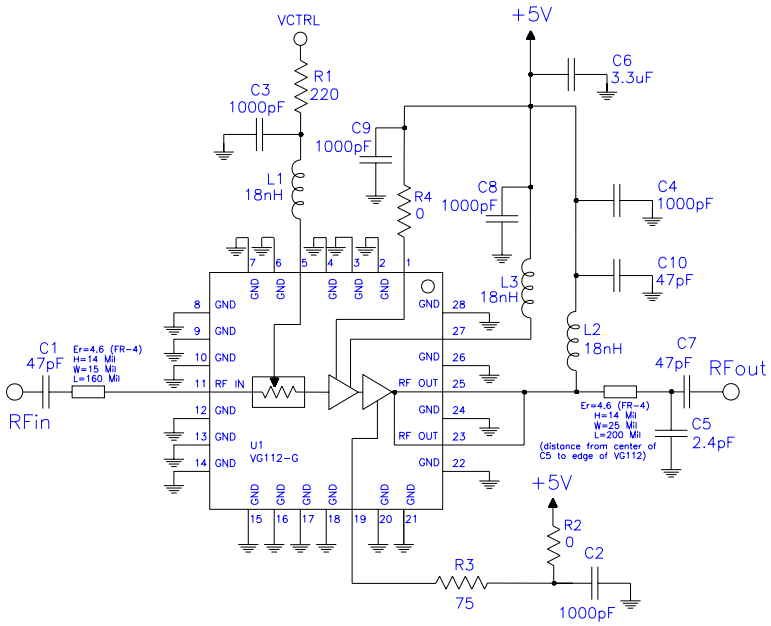
Ordering Information

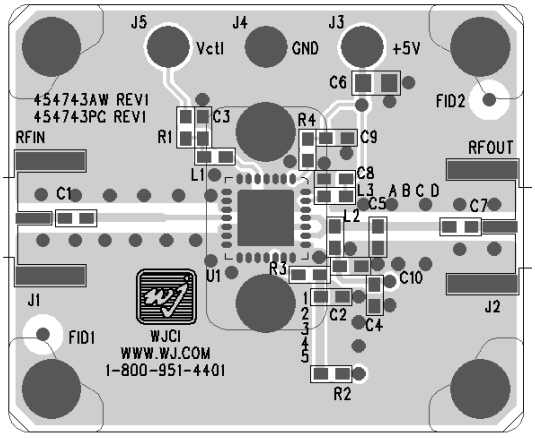
Part No.	Description
VG112-G	PCS/UMTS-band Variable Gain Amplifier (lead-free/green/RoHS-compliant QFN package)
VG112-PCB2140	2140 MHz Fully Assembled Application Board

Standard tape / reel size = 500 pieces on a 7″ reel

Specifications and information are subject to change without notice

2140 MHz Application Circuit Performance
Performance using the circuitry on the VG112-PCB Evaluation Board



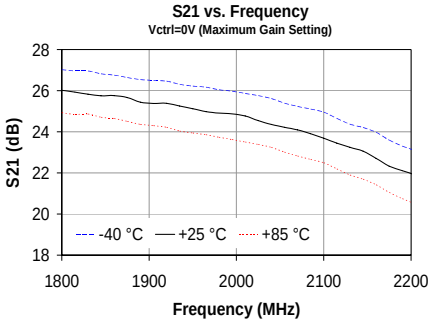


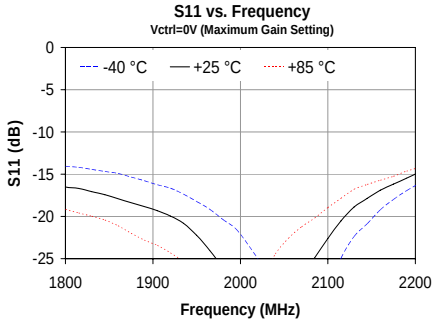
Circuit Board Material: .014" FR-4, 4 layers, .062" total thickness

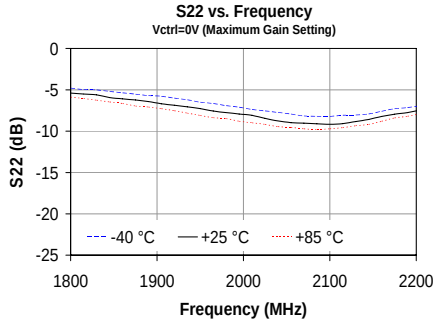
- The center of C5 should be placed 5mm (.197") away from the edge of the VG112.
- The input trace is a high impedance line and is needed to get a good input match into the VGA.
- The board is optimized for performance at 2140 MHz. Performance at 1960 MHz can be optimized by replacing C5 with 2.7 pF at location A on the WJ VG112 evaluation board.

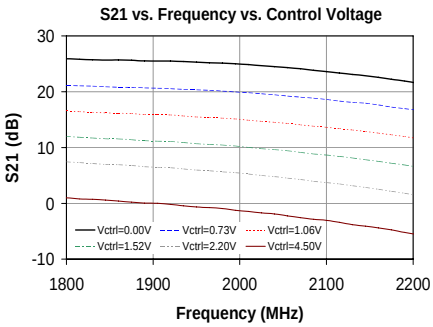
Bill of Materials

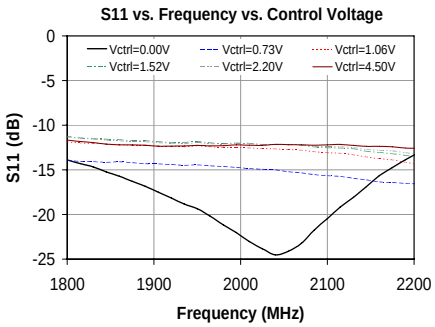
Ref. Des.	Description	Size
C1, C7, C10	47 pF Chip Capacitor	0603
C2, C3, C4, C8, C9	1000 pF Chip Capacitor	0603
C5	2.4 pF Chip Capacitor	0603
C6	3.3 µF Chip Capacitor	0805
L1, L2	18 nH Chip Inductor	0603
R1	220 Ω Chip Resistor	0603
R3	75 Ω Chip Resistor	0603
R2, R4	0 Ω Chip Resistor	0603
U1	VG112-G VGA	QFN 6x6

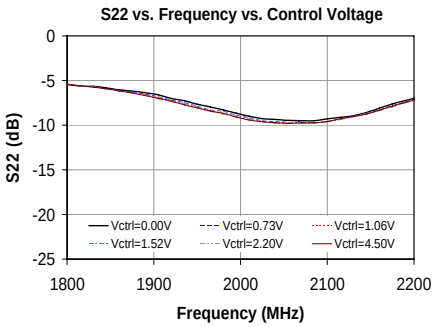






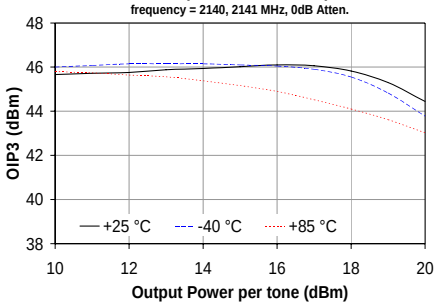




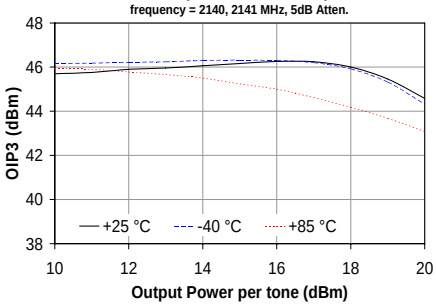


2140 MHz Application Circuit Performance

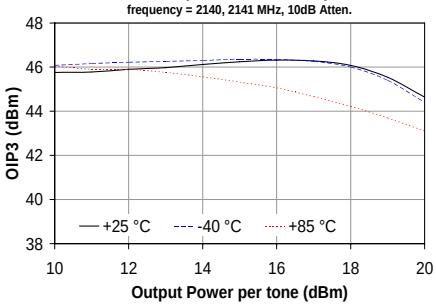
OIP3 vs. Output Power vs. Temperature
frequency = 2140, 2141 MHz, 0dB Atten.



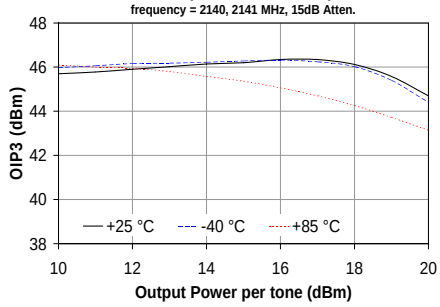
OIP3 vs. Output Power vs. Temperature
frequency = 2140, 2141 MHz, 5dB Atten.



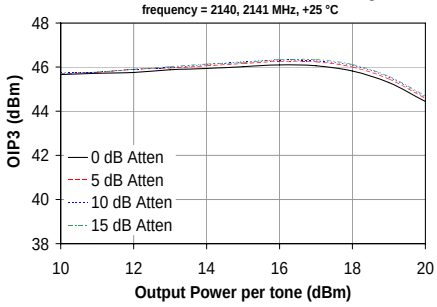
OIP3 vs. Output Power vs. Temperature
frequency = 2140, 2141 MHz, 10dB Atten.



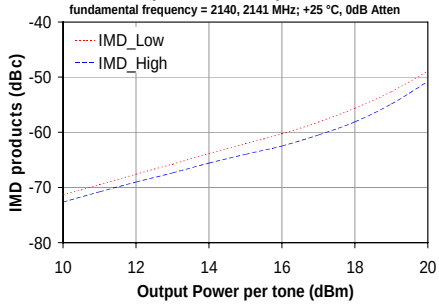
OIP3 vs. Output Power vs. Temperature
frequency = 2140, 2141 MHz, 15dB Atten.



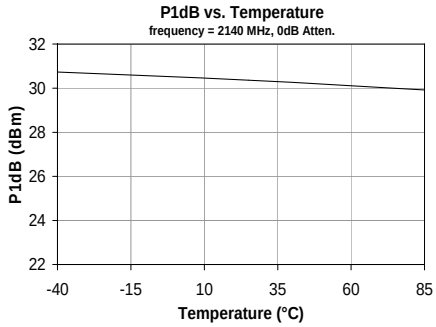
OIP3 vs. Pout vs. Attenuation Setting
frequency = 2140, 2141 MHz, +25 °C



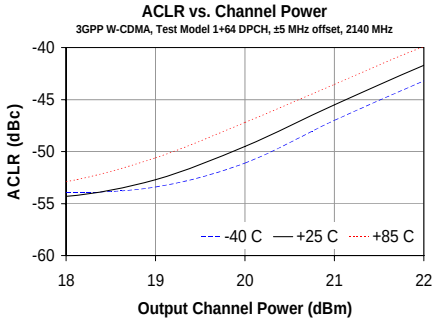
IMD products vs. Output Power
fundamental frequency = 2140, 2141 MHz; +25 °C, 0dB Atten



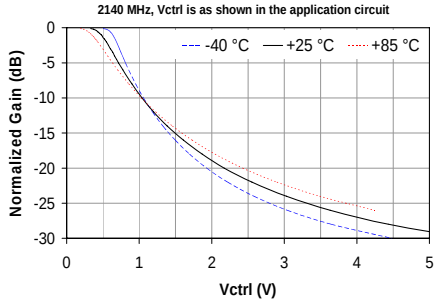
P1dB vs. Temperature
frequency = 2140 MHz, 0dB Atten.



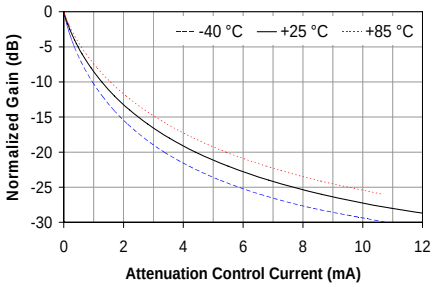
ACLR vs. Channel Power
3GPP W-CDMA, Test Model 1+64 DPCH, ±5 MHz offset, 2140 MHz



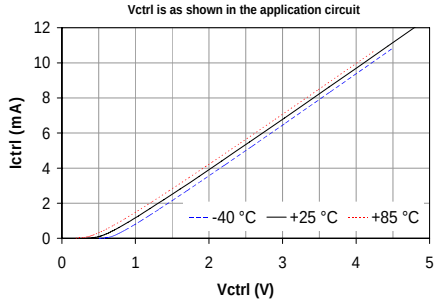
Normalized Gain vs. Vctrl
2140 MHz, Vctrl is as shown in the application circuit



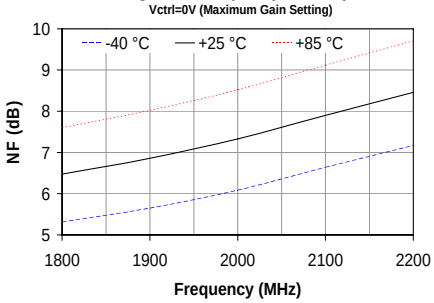
Normalized Gain vs. Ictrl
2140 MHz



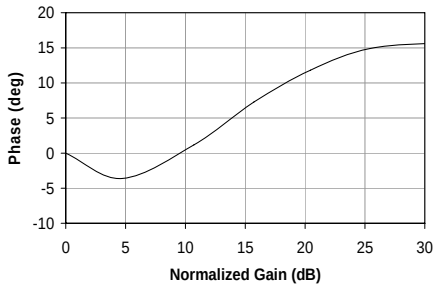
Ictrl vs. Vctrl
Vctrl is as shown in the application circuit



Noise Figure vs. Frequency vs. Temperature
Vctrl=0V (Maximum Gain Setting)



Phase vs. Normalized Gain
2140 MHz



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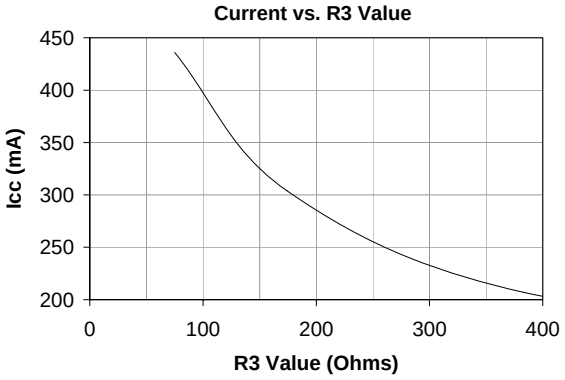
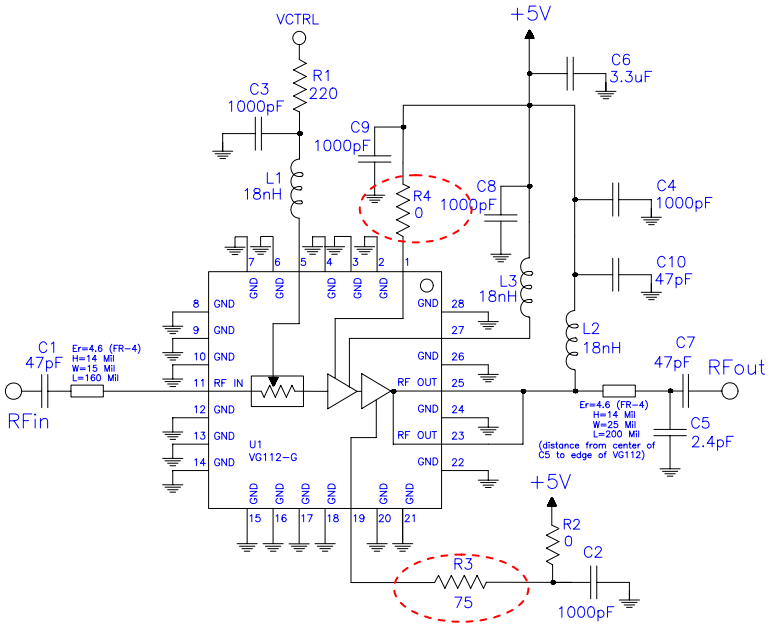
Application Note: Reduced Bias Configurations

The VG112 can be configured to be operated with lower bias current by varying the bias-adjust resistors – R3 and R4 – which set the current draw for the two stages of the amplifier. The recommended circuit configurations shown previously in this datasheet have the device operating in Class A operation. Lowering the current moderately can be done at the expense of the linearity performance of the device. Measured data is given below and represents the VG112 configured for 2.14 GHz applications. Since the second stage amplifier dominates the current draw of the 2-stage amplifier inside the VG112, modifying R3 will have the greatest effect upon the overall current draw of the device. Data is shown though to display the Icc and performance effects of the device when R4, the bias-adjust resistor for the first-stage amplifier, is modified when R3 is fixed.

Performance Data at 2.14 GHz

R3 (Ω)	R4 (Ω)	Icq (mA)	P_{diss} (W)	Gain (dB)	OIP3 (dBm)	P1dB (dBm)
75	0	436	2.18	24.0	46.3	30.7
174	0	304	1.52	23.7	42.5	30.8
383	0	207	1.04	23.3	33.4	30.9
787	0	155	0.78	22.5	27.7	29.7
174	101	284	1.42	23.5	42.3	30.6
174	270	264	1.32	23.3	41.6	30.4
174	499	251	1.26	23.0	40.2	29.8
174	699	244	1.22	22.7	38.9	29.1

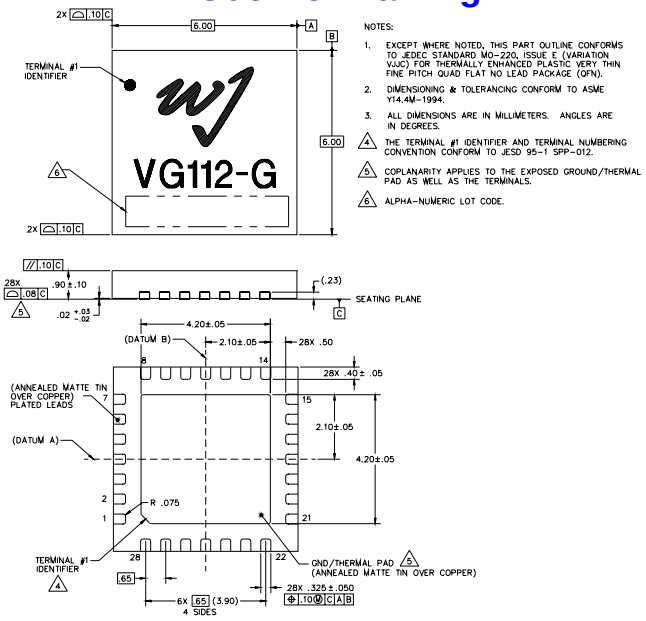




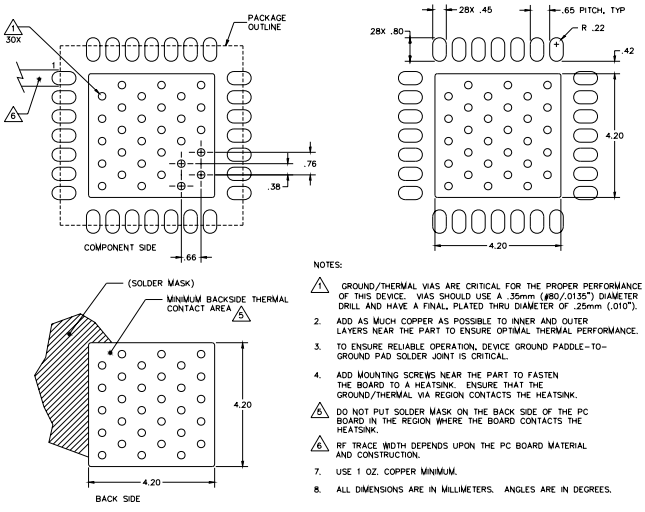
Mechanical Information

This package is lead-free/green/RoHS-compliant. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

Outline Drawing



Mounting Configuration / Land Pattern



Product Marking

The component will be lasermarked with a "VG112-G" designator with an alphanumeric lot code on the top surface of the package.

Tape and reel specifications for this part will be located on the website in the "Application Notes" section.

ESD / MSL Information

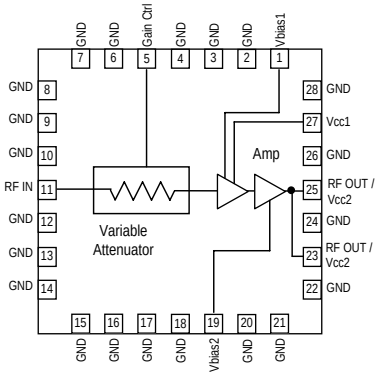
Caution! ESD sensitive device.

ESD Rating: Class 1B
Value: Passes ⩾500V to <1000V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV
Value: Passes ⩾1000V to <2000V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating: Level 2 at +260 °C convection reflow
Standard: JEDEC Standard J-STD-020

Functional Pin Layout



Pin No	Function
1	Vbias1
5	Gain Control
11	RF Input
19	Vbias2
23, 25	RF Output / Vcc2
27	Vcc1
Even numbered pins and backside paddle	Ground
3, 7, 9, 13, 15, 17, 21	No connect or ground