16K (2K x 8) PCMCIA Nonvolatile Attribute Memory

Features

- **Ideal Rewriteable Attribute Memory**
- **Simple Write Operation**
  - **Self-Timed Byte Writes**
  - **On-chip Address and Data Latch for SRAM-like Write Operation**
  - **Fast Write Cycle Time - 1 ms**
  - **5-Volt-Only Nonvolatile Writes**
- **End of Write Detection**
  - **RDY/$\overline{\text{BUSY}}$ Output**
  - **$\overline{\text{DATA}}$ Polling**
- **High Reliability**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 10 Years Minimum**
- **Single 5-Volt Supply for Read and Write**
- **Very Low Power**
  - **30 mA Active Current**
  - **100 µA Standby Current**

Description

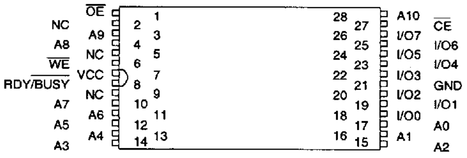
The AT28C16-T is the ideal nonvolatile attribute memory: it is a low power, 5-volt-only byte writeable nonvolatile memory (E^2PROM). Standby current is typically less than 100 µA. The AT28C16-T is written like a Static RAM, eliminating complex programming algorithms. The fast write cycle times of 1 ms, allow quick card reconfiguration in-system. Data retention is specified as 10 years minimum, precluding the necessity for batteries. Three access times have been specified to allow for varying layers of buffering between the memory and the PCMCIA interface.

The AT28C16-T is accessed like a Static RAM for read and write operations. During a byte write, the address and data are latched internally. Following the initiation of a write cycle, the device will go to a busy state and automatically write the latched data using an internal control timer. The device provides two methods for detecting the end of a write cycle; the RDY/$\overline{\text{BUSY}}$ output and $\overline{\text{DATA}}$ polling of I/O7.

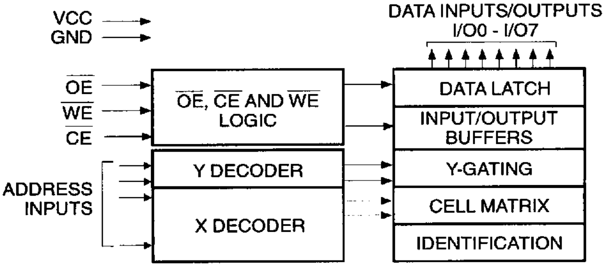
Pin Configurations

Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/$\overline{\text{BSY}}$	Ready/Busy Output
NC	No Connect

TSOP
Top View



Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +125°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to V_{CC} +0.6 V
Voltage on $\overline{\text{OE}}$ and A9 with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ:The AT28C16-T is accessed like a Static RAM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location detemined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C16-T is similar to writing into a Static RAM. A low pulse on $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{OE}}$ high and $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) initiates a byte write. The address is latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ (whichever occurs last) and the data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ (whichever occurs first). Once a byte write is started it will automatically time itself to completion. For the AT28C16-T the write cycle time is 1 ms maximum. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

READY/$\overline{\text{BUSY}}$: Pin 1 is an open drain READY/$\overline{\text{BUSY}}$ output that indicates the current status of the self-timed internal write cycle. READY/$\overline{\text{BUSY}}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain output allows OR-tying of several devices to a common interrupt input.

$\overline{\text{DATA}}$ POLLING: The AT28C16-T also provides $\overline{\text{DATA}}$ polling to signal the completion of a write cycle. During a write cycle, an attempted read of the the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all ouputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense— if V_{CC} is below 3.8 V (typical) the write function is inhibited; (b) V_{CC} power on delay— once V_{CC} has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a byte write; (c) Write Inhibit— holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C16-T may be set to the high state by the Chip Clear operation. By setting $\overline{\text{CE}}$ low and $\overline{\text{OE}}$ to 12 V, the chip is cleared when a 10ms low pulse is applied to $\overline{\text{WE}}$.

DEVICE IDENTIFICATION: An extra 32 bytes of E^2PROM memory are available to the user for device identifcation. By raising A_9 to 12 V (±0.5 V) and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

D.C. and A.C. Operating Range

		AT28C16-15T	AT28C16-20T	AT28C16-25T
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write(2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X(1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H (3)	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1\ V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O} = 0\ V$ to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}-0.3\ V$ to $V_{CC} + 1.0\ V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0\ V$ to $V_{CC} + 1.0\ V$	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current	$f = 5\ MHz$; $I_{OUT} = 0\ mA$	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\ mA$			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) (1)

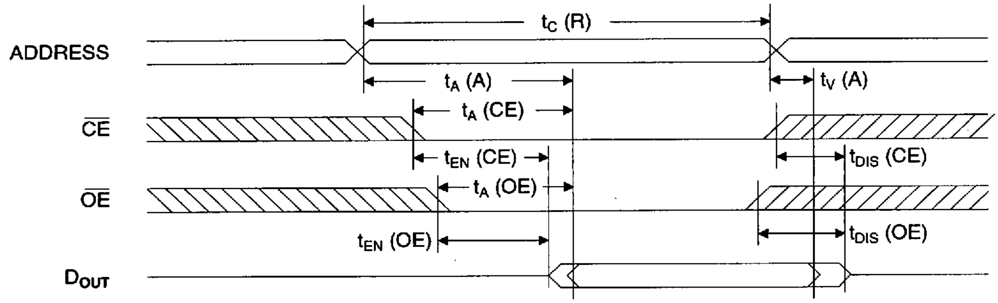
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0\ V$
C_{OUT}	8	12	pF	$V_{OUT} = 0\ V$

Note: 1. This parameter is characterized and is not 100% tested.

A.C. Read Characteristics

PCMCIA Symbol	Atmel Symbol	Parameter	AT28C16-15T		AT28C16-20T		AT28C16-25T		Units
			Min	Max	Min	Max	Min	Max	
t_C (R)	t_{RC}	Read Cycle Time	150		200		250		ns
t_A (A)	t_{ACC}	Address Access Time		150		200		250	ns
t_A (CE)	t_{CE} (1)	$\overline{CE}$ Access Time		150		200		250	ns
t_A (OE)	t_{OE} (2)	$\overline{OE}$ Access Time	0	75	0	80	0	100	ns
t_{EN} (CE)	t_{LZ} (4)	Output Enable Time From $\overline{CE}$	0		0		0		ns
t_{EN} (OE)	t_{OLZ} (4)	Output Enable Time From $\overline{OE}$	0		0		0		ns
t_V (A)	t_{OH}	Output Hold Time	0		0		0		ns
t_{DIS} (CE)	t_{DF} (3,4)	Output Disable Time From $\overline{CE}$	0	50	0	55	0	60	ns
t_{DIS} (OE)	t_{DF} (3,4)	Output Disable Time From $\overline{OE}$	0	50	0	55	0	60	ns

A.C. Read Waveforms(1,2,3,4)



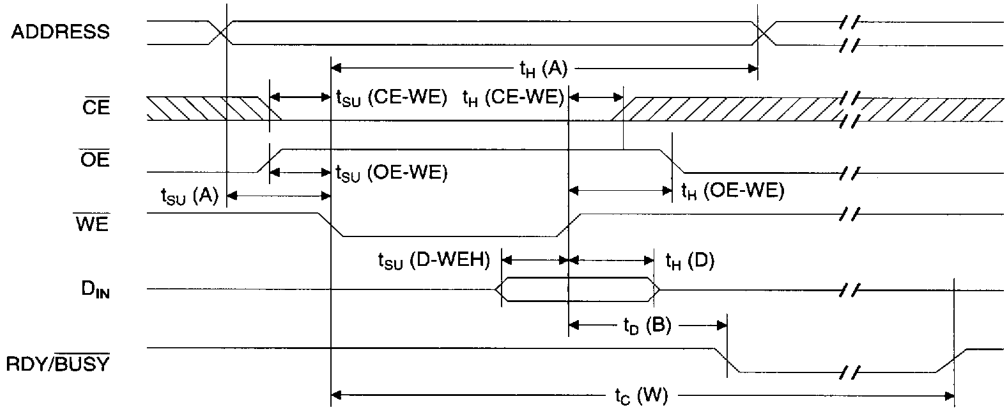
Notes:

1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

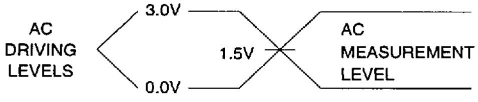
A.C. Write Characteristics

PCMCIA Symbol	Atmel Symbol	Parameter	Min	Max	Units
t_{SU} (A)	t_{AS}	Address Setup Time	10		ns
t_{SU} (OE-WE)	t_{OES}	Output Disable Time To $\overline{\text{WE}}$	10		ns
t_{SU} (CE-WE)	t_{CS}	Chip Enable Time To $\overline{\text{WE}}$	0		ns
t_W (WE)	t_{WP}	Write Enable Pulse Width	100	1000	ns
t_{SU} (D-WEH)	t_{DS}	Data Setup To $\overline{\text{WE}}$ High	50		ns
t_H (A)	t_{AH}	Address Hold Time From $\overline{\text{WE}}$	50		ns
t_H (D)	t_{DH}	Data Hold Time From $\overline{\text{WE}}$ High	10		ns
t_H (OE-WE)	t_{OEH}	Output Enable Hold Time From $\overline{\text{WE}}$ High	10		ns
t_H (CE-WE)	t_{CH}	Chip Enable Hold Time From $\overline{\text{WE}}$ High	0		ns
t_D (B)	t_{DB}	Delay From $\overline{\text{WE}}$ High To $\overline{\text{BUSY}}$ Asserted		50	ns
t_C (W)	t_{WC}	Write Cycle Time		1	ms

A.C. Write Waveforms

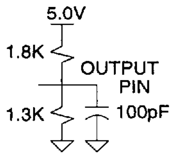


Input Test Waveforms and Measurement Level

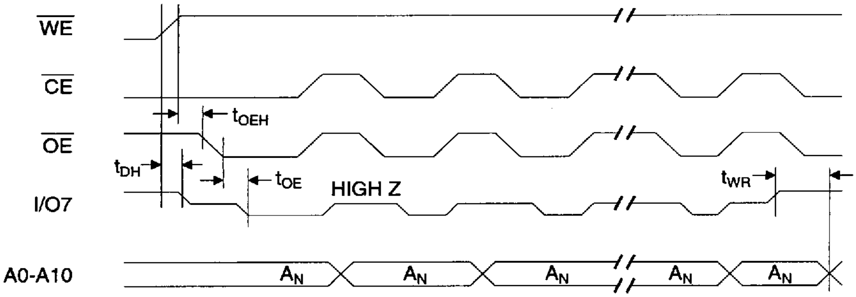


t_R, $t_F < 5$ ns

Output Test Load

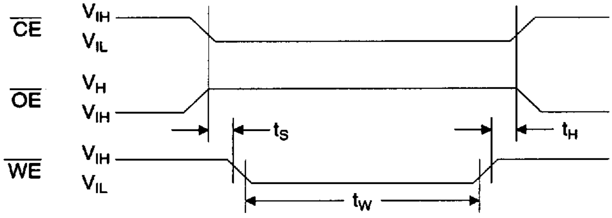


Data Polling Waveforms



Note: Data Polling A.C. Timing Characteristics are the same as the A.C. Read Characteristics.

Chip Erase Waveforms



$t_S = t_H = 1$ μsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0 \pm 0.5$ V

Ordering Information(1)

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C16-15TC	28T	Commercial (0°C to 70°C)
150	45	0.1	AT28C16-15TI	28T	Industrial (-40°C to 85°C)
200	30	0.1	AT28C16-20TC	28T	Commercial (0°C to 70°C)
200	45	0.1	AT28C16-20TI	28T	Industrial (-40°C to 85°C)
250	30	0.1	AT28C16-25TC	28T	Commercial (0°C to 70°C)
250	45	0.1	AT28C16-25TI	28T	Industrial (-40°C to 85°C)

Note: 1. See Valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C16	12	TC, TI
AT28C16	15	TC, TI
AT28C16	20	TC, TI
AT28C16	25	TC, TI

Package Type	
28T	28 Lead, Plastic Thin Small Outline Package (TSOP)