

6501128 NATL SEMICOND, (UP/UC)

18C 32843

D

T-49-19-59

T-49-19-05



October 1980

## INS8048-Series Microcomputer/Microprocessor Family

### General Description

The INS8048/49/50-Series microcomputers and the INS8035/39/40-Series microprocessors (hereinafter referred to as the 48-Series) are self contained, 8-bit parallel, 40-pin, dual in-line devices fabricated using National Semiconductor's scaled N-channel, silicon gate MOS process, XMOS. The 48-Series devices contain the system timing, control logic, ROM (where applicable) program memory, RAM data memory and 27 I/O lines necessary to implement dedicated control functions. All 48-Series devices are pin compatible, differing only in the size of on-board ROM (where applicable) and RAM as shown below:

| DEVICE  | RAM ARRAY | ROM ARRAY |
|---------|-----------|-----------|
| INS8048 | 64 x 8    | 1K x 8    |
| INS8049 | 128 x 8   | 2K x 8    |
| INS8050 | 256 x 8   | 4K x 8    |
| INS8035 | 64 x 8    | N/A       |
| INS8039 | 128 x 8   | N/A       |
| INS8040 | 256 x 8   | N/A       |

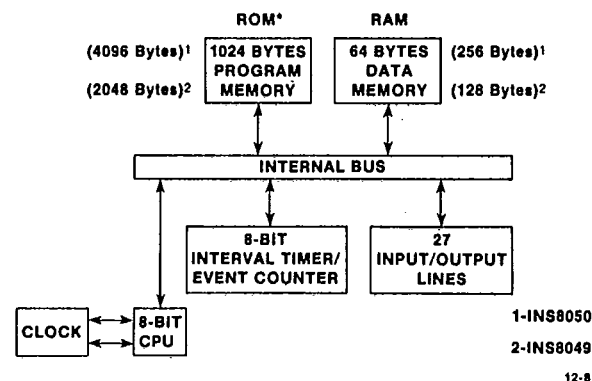
The devices are designed to be efficient controllers. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory is derived from an instruction set comprised predominantly of single bytes. The remaining instructions are two bytes in length. Additional external memory may be added up to a maximum of 4K bytes of program memory and 256 bytes of data memory without paging.

### Features

- 8-Bit CPU, RAM, ROM, I/O in Single Package
- 2.5  $\mu$ sec Cycle, 6 MHz Clock; 1.36  $\mu$ sec Cycle, 11 MHz Clock
- On-Chip Oscillator Circuit and Clock (or External Source)
- 27 I/O Lines
- Expandable Memory and I/O
- 8-Bit Timer/Counter
- Single Level Interrupt
- Interrupt has Schmitt Trigger with Hysteresis\*
- Over 90 Instructions (Most Single Byte)
- Binary and BCD Arithmetic
- Single 15V Power Supply
- Low Standby Power Mode\*
- Low Voltage Standby (2.2V Min)\*
- On-Chip Battery Charging\*

\*NOTE: Transparent improvements over industry standard part.

### 48-Series Block Diagram



\*Not Applicable to INS8035/39/40

INS8048-Series Microcomputer/Microprocessor Family

6501128 NATL SEMICOND, (UP/UC)

18C 32844

D

T-49-19-59

T-49-19-05

**Absolute Maximum Ratings**

Temperature Under Bias ..... 0°C to +70°C  
 Storage Temperature ..... -65°C to +150°C  
 All Input or Output Voltages with respect V<sub>SS</sub> ..... -0.5V to +7.0V  
 Power Dissipation ..... 1.5 Watt

NOTE: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

**DC Electrical Characteristics**

T<sub>A</sub> = 0° C to +70° C, V<sub>CC</sub> = +5V ±10%, V<sub>SS</sub> = 0V, unless otherwise specified.

| Symbol                            | Parameter   | Min  | Typ | Max             | Units | Test Conditions  |
|-----------------------------------|---|------|-----|-----------------|-------|--|
| V <sub>IL</sub>                   | Input Low Voltage (All except XTAL1, XTAL2)             | -0.5 |     | 0.8             | V     |  |
| V <sub>IL1</sub>                  | Input Low Voltage (XTAL1, XTAL2)                        | -0.5 |     | 0.6             | V     |  |
| V <sub>IH</sub>                   | Input High Voltage                                      | 2.0  |     | V <sub>CC</sub> | V     |  |
| V <sub>IH1</sub>                  | Input High Voltage (RESET, XTAL1, XTAL2)                | 3.0  |     | V <sub>CC</sub> | V     |  |
| V <sub>OL</sub>                   | Output Low Voltage                                      |      |     | 0.4             | V     | I <sub>OL</sub> = 2.0mA                                    |
| V <sub>OH</sub>                   | Output High Voltage All except ports 1 and 2            | 3.0  |     | V <sub>CC</sub> | V     | I <sub>OH</sub> = 100 μA                                   |
| V <sub>OH1</sub>                  | Port TTL  | 2.4  |     |                 | V     | I <sub>OH</sub> ≥ 125 μA                                   |
| I <sub>IL</sub>                   | Input Leakage Current (T1, EA, INT)                     |      |     | ±10             | μA    | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>        |
| I <sub>OL</sub>                   | Output Leakage Current (BUS, T0) (High Impedance State) |      |     | -10.0           | μA    | V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub> + 0.45 |
| I <sub>DD</sub> (64)              | 64 words on Standby Current (2)                         |      |     | 2.5             | mA    | 8048   |
| I <sub>DD</sub> (128)             | 128 words on Standby Current (2)                        |      |     | 4.5             | mA    | 8049   |
| I <sub>DD</sub> (256)             | 256 words on Standby Current (2)                        |      |     | 8.5             | mA    | 8050   |
| I <sub>DD</sub> + I <sub>CC</sub> | Total Supply Current 8048                               |      | 30  | 65              | mA    | T <sub>A</sub> = 25° C                                     |
| I <sub>DD</sub> + I <sub>CC</sub> | Total Supply Current 8048L                              |      | 25  | 40              | mA    | T <sub>A</sub> = 25° C                                     |
| I <sub>DD</sub> + I <sub>CC</sub> | Total Supply Current 8049                               |      | 32  | 70              | mA    | T <sub>A</sub> = 25° C                                     |
| I <sub>DD</sub> + I <sub>CC</sub> | Total Supply Current 8049L                              |      | 30  | 45              | mA    | T <sub>A</sub> = 25° C                                     |
| I <sub>DD</sub> + I <sub>CC</sub> | Total Supply Current 8050                               |      | 35  | 75              | mA    | T <sub>A</sub> = 25° C                                     |
| I <sub>DD</sub> + I <sub>CC</sub> | Total Supply Current 8050L                              |      | 35  | 50              | mA    | T <sub>A</sub> = 25° C                                     |
| I <sub>DDC</sub>                  | Battery Charging Current                                |      |     | TBD             | mA    | See Figure 5   |
| V <sub>DD</sub>                   | Standby Power Supply                                    | 2.4  |     | V <sub>CC</sub> | V     | See Figure 5   |

Notes: 1. The Series-48 family of parts are also available in Industrial Temperature Range -40°C to +80°C. Industrial Temperature Range versions are denoted with an I following the part number (i.e., INS8048-6XXX/NI).

2. The low power versions (L parts), and the Industrial Temperature Range (I parts), are currently available throughout the Series-48 Family.

6501128 NATL SEMICONDUCT, (UP/UC)

18C 32845

D

T-49-19-59

T-49-19-05

**AC Electrical Characteristics - INS80XX-6 (1-6 MHz part)**T<sub>A</sub> = 0° C to +70° C, V<sub>CC</sub> = +5V ±10%, V<sub>SS</sub> = 0V, unless otherwise specified.

| Symbol           | Parameter                           | Min | Typ | Max  | Units | Test Conditions        |
|------------------|-------------------------------------|-----|-----|------|-------|------------------------|
| t <sub>LL</sub>  | ALE Pulse Width                     | 400 |     |      | ns    | Note 1                 |
| t <sub>AL</sub>  | Address Setup to ALE                | 150 |     |      | ns    | Note 1                 |
| t <sub>LA</sub>  | Address Hold from ALE               | 80  |     |      | ns    | Note 1                 |
| t <sub>CC</sub>  | Control Pulse Width<br>PSEN, RD, WR | 700 |     |      | ns    | Note 1                 |
| t <sub>DW</sub>  | Data Set-Up Before WR               | 500 |     |      | ns    | Note 1                 |
| t <sub>WD</sub>  | Data Hold After WR                  | 120 |     |      | ns    | C <sub>L</sub> = 20 pF |
| t <sub>CY</sub>  | Cycle Time                          | 2.5 |     | 15.0 | μs    | 1 to 6 MHz XTAL        |
| t <sub>DR</sub>  | Data Hold                           | 0   |     | 200  | ns    | Note 1                 |
| t <sub>RD</sub>  | PSEN, RD to Data In                 |     |     | 500  | ns    | Note 1                 |
| t <sub>AW</sub>  | Address Setup to WR                 | 230 |     |      | ns    | Note 1                 |
| t <sub>AD</sub>  | Address Setup to Data In            |     |     | 950  | ns    | Note 1                 |
| t <sub>AFG</sub> | Address Float to RD, PSEN           | 0   |     |      | ns    | Note 1                 |
| t <sub>CA</sub>  | Control Pulse to ALE                | 10  |     |      | ns    | Note 1                 |

**Port 2 Timing**

| Symbol          | Parameter   | Min  | Typ | Max | Units | Test Conditions |
|-----------------|---|------|-----|-----|-------|-----------------|
| t <sub>CP</sub> | Port Control Setup before<br>Falling Edge of PROG | 110  |     |     | ns    | Note 1          |
| t <sub>PC</sub> | Port Control Hold after<br>Falling Edge of PROG   | 140  |     |     | ns    | Note 1          |
| t <sub>PR</sub> | PROG to Time P2 Input<br>must be Valid            |      |     | 810 | ns    | Note 1          |
| t <sub>DP</sub> | Output Data Setup Time                            | 250  |     |     | ns    | Note 1          |
| t <sub>PD</sub> | Output Data Hold Time                             | 65   |     |     | ns    | Note 1          |
| t <sub>PF</sub> | Input Data Hold Time                              | 0    |     | 150 | ns    | Note 1          |
| t <sub>PP</sub> | PROG Pulse Width                                  | 1510 |     |     | ns    | Note 1          |
| t <sub>PL</sub> | Port 2 I/O Data Setup                             | 400  |     |     | ns    | Note 1          |
| t <sub>LP</sub> | Port 2 I/O Data Hold                              | 150  |     |     | ns    | Note 1          |

**AC Electrical Characteristics - INS80XX-11 (4-11 MHz Part)**T<sub>A</sub> = 0° C to +70° C, +5V ±10%, V<sub>SS</sub> = 0V, unless otherwise specified.

| Symbol          | Parameter                           | Min  | Typ | Max  | Units | Test Conditions        |
|-----------------|-------------------------------------|------|-----|------|-------|------------------------|
| t <sub>LL</sub> | ALE Pulse Width                     | 150  |     |      | ns    | Note 1                 |
| t <sub>AL</sub> | Address Setup to ALE                | 70   |     |      | ns    | Note 1                 |
| t <sub>LA</sub> | Address Hold from ALE               | 50   |     |      | ns    | Note 1                 |
| t <sub>CC</sub> | Control Pulse Width<br>PSEN, RD, WR | 300  |     |      | ns    | Note 1                 |
| t <sub>DW</sub> | Data Set-Up Before WR               | 250  |     |      | ns    | Note 1                 |
| t <sub>WD</sub> | Data Hold After WR                  | 40   |     |      | ns    | C <sub>L</sub> = 20 pF |
| t <sub>CY</sub> | Cycle Time                          | 1.36 |     | 3.75 | μs    | 4 to 11 MHz XTAL       |
| t <sub>DR</sub> | Data Hold                           | 0    |     | 100  | ns    | Note 1                 |
| t <sub>RD</sub> | PSEN, RD to Data In                 |      |     | 200  | ns    | Note 1                 |

6501128 NATL SEMICONDUCTOR, (UP/UC)

18C 32846

D

T-49-19-59

T-49-19-05

**AC Electrical Characteristics - INS80XX-11 (Cont'd.)**

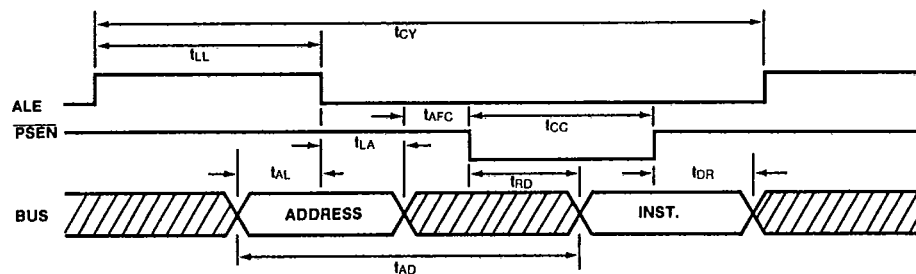
| Symbol           | Parameter  | Min | Typ | Max | Units | Test Conditions |
|------------------|--|-----|-----|-----|-------|-----------------|
| t <sub>AW</sub>  | Address Set-Up to $\overline{WR}$                    | 200 |     |     | ns    | Note 1          |
| t <sub>AD</sub>  | Address Set-up to Data In                            |     |     | 400 | ns    | Note 1          |
| t <sub>AFC</sub> | Address Float to $\overline{RD}$ , $\overline{PSEN}$ | -10 |     |     | ns    | Note 1          |
| t <sub>CA</sub>  | Control Pulse to ALE                                 | 10  |     |     | ns    | Note 1          |

**Port 2 Timing**

| Symbol          | Parameter                                      | Min | Typ | Max | Units | Test Conditions |
|-----------------|--|-----|-----|-----|-------|-----------------|
| t <sub>CP</sub> | Port Control Setup before Falling Edge of PROG | 100 |     |     | ns    | Note 1          |
| t <sub>PC</sub> | Port Control Hold after Falling Edge of PROG   | 60  |     |     | ns    | Note 1          |
| t <sub>PR</sub> | PROG to Time P2 Input must be Valid            |     |     | 650 | ns    | Note 1          |
| t <sub>DP</sub> | Output Data Setup Time                         | 200 |     |     | ns    | Note 1          |
| t <sub>PD</sub> | Output Data Hold Time                          | 20  |     |     | ns    | Note 1          |
| t <sub>PF</sub> | Input Data Hold Time                           | 0   |     | 150 | ns    | Note 1          |
| t <sub>PP</sub> | PROG Pulse Width                               | 700 |     |     | ns    | Note 1          |
| t <sub>PL</sub> | Port 2 I/O Data Setup                          | 150 |     |     | ns    | Note 1          |
| t <sub>LP</sub> | Port 2 I/O Data Hold                           | 20  |     |     | ns    | Note 1          |

Note 1. Control outputs C<sub>L</sub> = 80 pF; Bus outputs C<sub>L</sub> = 150 pF**Capacitance** T<sub>A</sub> = 25° C, V<sub>CC</sub> = V<sub>SS</sub> = 0V

| Symbol           | Parameter                    | Min | Typ | Max | Units | Test Conditions                             |
|------------------|------------------------------|-----|-----|-----|-------|---|
| C <sub>IN</sub>  | Input Capacitance            |     | 6   | 10  | pF    | f <sub>c</sub> = 1 MHz                      |
| C <sub>OUT</sub> | OUTPUT AND RESET Capacitance |     | 10  | 20  | pF    | Unmeasured pins returned to V <sub>SS</sub> |

**Timing Waveforms**

Instruction Fetch from External Program Memory

12-14

NOTE: Diagonal lines indicate interval of high impedance.

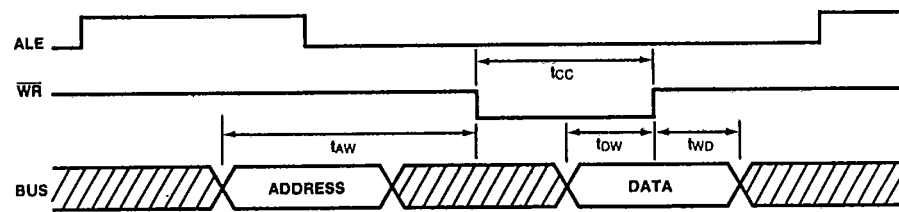
6501128 NATL SEMICOND. (UP/UC)

18C 32847

D

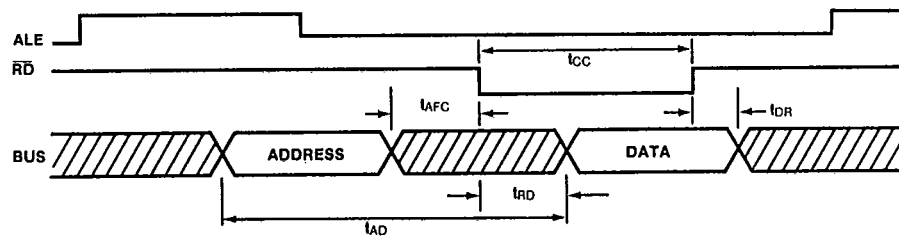
T-49-19-59

T-49-19-05



Write to External Data Memory

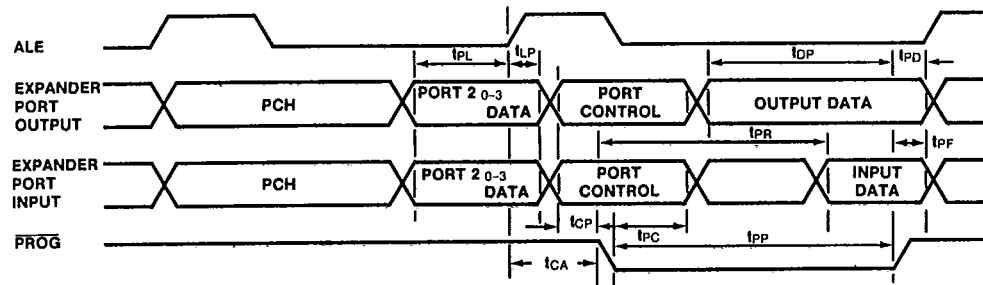
12-15



Read from External Data Memory

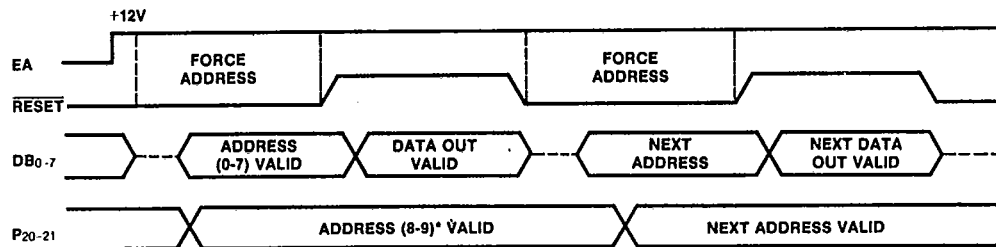
NOTE: Diagonal lines indicate interval of high impedance.

12-11



12-12

Port 2 Timing



\*8049 = 8-10  
8050 = 8-11

Verify Mode Timing

12-13

6501128 NATL SEMICOND, (UP/UC)

18C 32848

D

T-49-19-59

T-49-19-05

**Functional Pin Description****INPUT SIGNALS**

**Reset (RESET):** An active low (0) input that initializes the processor and is used to verify program memory. (See note #1.)

**Single Step (SS):** Active low (0) input which, in conjunction with ALE, can single step the processor through each instruction.

**External Access (EA):** An active high (1) input that forces all program memory fetches to reference external program memory.

**Testable Input 0 (T0):** Testable input pin using conditional branch functions JT0 (T<sub>0</sub> = 1) or JNT0 (T<sub>0</sub> = 0). T<sub>0</sub> can be designated as the clock output using instruction ENT0 CLK.

**Testable Input 1 (T1):** Testable input pin using conditional branch functions JT1 (T<sub>1</sub> = 1) or JNT1 (T<sub>1</sub> = 0). T<sub>1</sub> can be designated as the Timer/Counter input from an external source using instruction STRT CNT.

**Interrupt (INT):** An active low input that initiates an interrupt when interrupt is enabled. Interrupt is disabled after a reset. Also can be tested with instruction JNI (INT 0). (See Note 2).

**OUTPUT SIGNALS**

**Read Strobe (RD):** An active low output strobe activated during a Bus read. Can be used to enable data onto the BUS from an external device. Used as a Read Strobe to External Data Memory.

**Write Strobe (WR):** An active low output strobe activated during a Bus write. Used as a Write Strobe to External Data Memory.

**Program Store Enable (PSEN):** An active low output that occurs only during an external program memory fetch.

**Address Latch Enable (ALE):** An active high output that occurs once during each cycle and is useful as a clock output. The negative going edge of ALE strobes the address into external data or program memory.

**Program (PROG):** This output (active high) provides the output strobe for INS8243 I/O Expander.

**INPUT/OUTPUT SIGNALS**

**Crystal Input (XTAL1, XTAL2):** These two pins connect the crystal for internal oscillator operation. XTAL1 is the timing input for external source.

**Port 1 (P10-P17):** 8-bit quasi-bidirectional port.

**Port 2 (P20-P27):** 8-bit quasi-bidirectional port. During an external program memory fetch, the four high-order program counter bits occur at P20-P23. They also serve as a 4-bit I/O expander bus when the INS8243 I/O Expander is used. (See note 3).

**BUS (DB0-DB7):** True bidirectional port, either statically latched or synchronous. Can be written to using WR Strobe, or Read from using RD Strobe. During an external program memory fetch, the 8 lower order program counter bits are preset at this port. The addressed instruction appears on this bus when PSEN is low. During an external RAM data store instruction. This port presents address and data under control of ALE, RD, and WR.

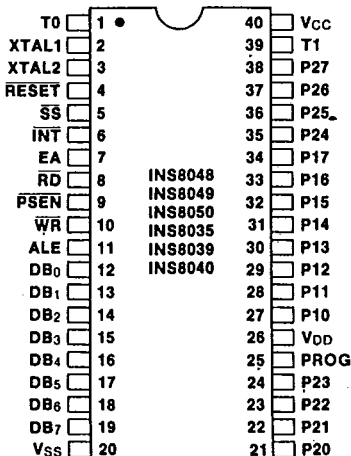
**Vss:** Processor Ground potential.

**VDD:** VDD functions as the Low Power Stand-by Voltage and can vary from 2.2V to 5.5V.

**Vcc: Pin 40:** Primary Power Source for 48-Series Devices.

**Functional Description**

The following paragraphs contain the functional description of the major elements of the 48-Series microcomputer/microprocessor. Figure 1 is a block diagram of the 48-Series devices. The data paths are illustrated in simplified form to show how the various logic elements communicate with each other to implement the instruction set common to all devices.

**Pin Configuration**

T-49-19.05

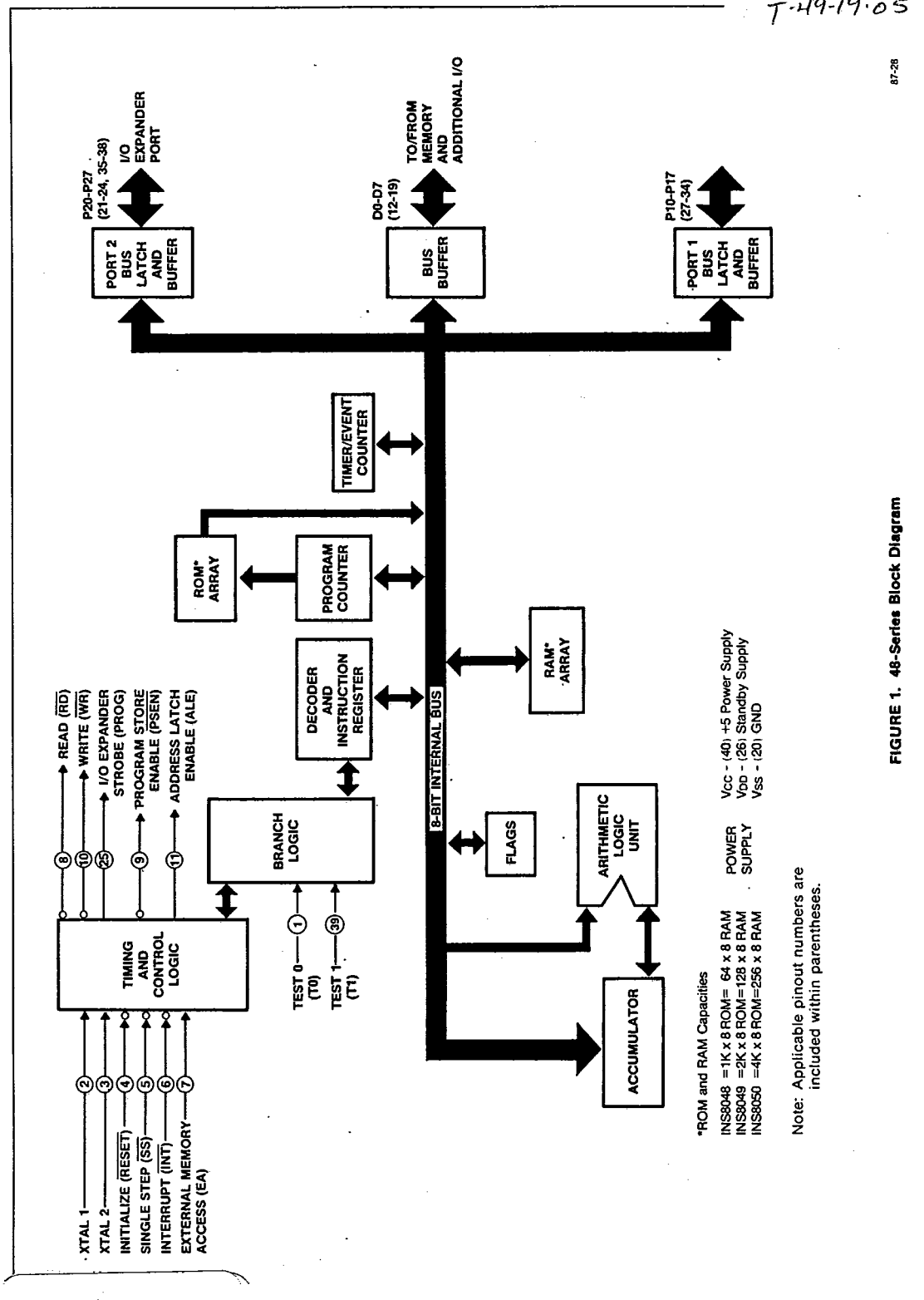


FIGURE 1. 48-Series Block Diagram

6501128 NATL SEMICOND, (UP/UC)

18C 32850

D

T-49-19-59

T-49-19-05

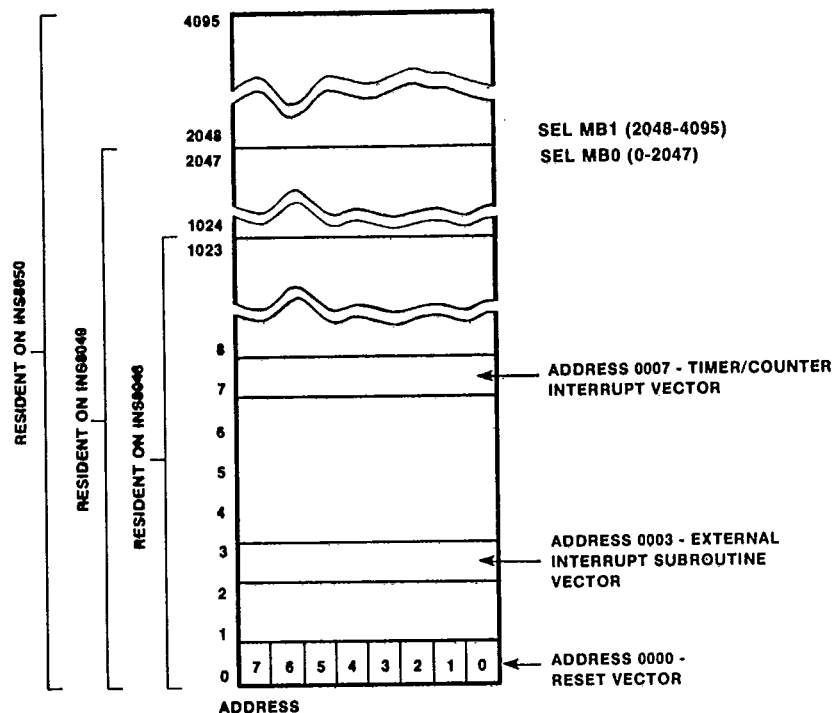
**Program Memory**

The Program Memory (ROM) contained on the INS8048/49/50 devices is comprised of 1024, 2048 or 4096 8-bit bytes, respectively. As is seen by examining the 48-Series instruction set, these bytes may be program instructions, program data or ROM addressing data. The ROM for the above devices must be mask programmed at the National Semiconductor factory. The ROMless microprocessors, INS8035, INS8039 and INS8040 use external program memory. This makes program development straightforward using standard UV erasable PROMs to emulate a possible future single chip (using the on-board ROM) system. ROM addressing, up to a maximum of 4K, is accomplished by a 12-bit Program Counter (PC). The INS8048 and INS8049 will automatically address external memory when the boundary of their internal memories, 1K and 2K respectively, are exceeded. The binary value of the address selects one of the 8-bit bytes contained in ROM. A new address is loaded into the PC register during each

instruction cycle. Unless the instruction is a transfer of control instruction, the PC register is loaded with the next sequential binary count value.

With reference to the Program Memory Map (see Figure 2) there are three ROM addresses which provide for the control of the microcomputer.

1. Memory Location 0000 - Resetting the Reset (negative true) input to the microcomputer forces the first instruction to be fetched from address 0000.
2. Memory Location 0003 - Asserting the Interrupt (negative true) input to the microcomputer (when interrupt is enabled) forces a jump to subroutine.
3. Memory Location 0007 - A timer/counter interrupt that results from timer/counter overflow (when enabled) forcing a jump to subroutine.



12-2

FIGURE 2. INS8048/49/50 Resident ROM Program Memory Map



6501128 NATL SEMICOND, (UP/UC)

18C 32851

D

T-49-19-59

T-49-19-05

**Data Memory (RAM)**

The resident RAM data memory is arranged as 64 (INS8035/8048), 128 (INS8039/8049) or 256 (INS8040/8050) bytes. RAM addressing is implemented indirectly via either of two 8-bit RAM pointer registers R0 and R1. These pointer registers are essentially the first two locations in the RAM (see Figure 3), addresses 000 and 001. RAM addressing may also be performed directly by 11 direct register instructions. The pointer register area of the RAM array is made up of eight working registers that occupy either the first bank (0), locations (0 to 7), or the second bank (1), locations (8 to 15). The second bank of working registers is selected by using the Register Bank Switch instruction (SEL RB). If this bank is not used for working registers, it can be used as user RAM.

There is an 8-level stack after Bank 0 that occupies address locations 16 to 23. These RAM locations are addressed indirectly through R0, R1 or the 3-bit Stack Pointer (SP). The stack pointer keeps track of the return address and pushes each return address down into the stack. There are 8 levels of subroutine nesting possible in the stack because each address occupies 10 bits or more using two bytes in RAM. When the level of subroutine nesting is less than 8, the stacks not used may be utilized as user RAM locations.

**Input/Output**

The 48-Series devices have 27 lines of input/output organized as three, 8-bit ports plus three test inputs. The three ports may be used as inputs, outputs or bidirectional ports. Ports 1 and 2 differ from port 3 (Bus Port) in that they are quasi-bidirectional ports. Ports 1 and 2 can be used as input and output while being statically latched. If more I/O lines are required, Port 2 can also serve as a 4-bit I/O bus expander when used in conjunction with the INS8243 I/O Expander.

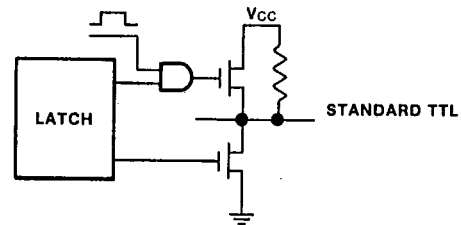


FIGURE 4. Input/Output Options

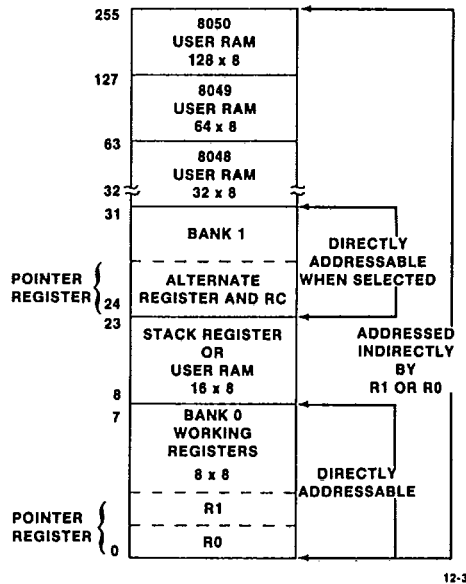


FIGURE 3. 48-Series Resident RAM Data Memory Map

6501128 NATL SEMICOND, (UP/UC)

18C 32852

D

T-49-19-59

T-49-19-05

The bus port is a true bidirectional port and is either statically latched or synchronous. It can be written to using  $\overline{WR}$  strobe or read from using  $\overline{RD}$  strobe. During an external program memory fetch, the 8 lower order program counter bits are preset at this port. The addressed instruction appears on this bus when  $\overline{PSEN}$  is low. During an external RAM data store instruction, this port presents address and data under control of  $\overline{ALE}$ ,  $\overline{RD}$ , and  $\overline{WR}$ .

#### Transparent Improvements

National has made some additional improvements to the standard industry parts. These include a battery charging circuit, and interrupt pin with hysteresis. Also, these improvements are transparent to the user. See Figure 5.

#### Power Down Mode

During the power down mode,  $V_{DD}$  which normally maintains the RAM cells, is the only pin that receives power.  $V_{CC}$ , which serves the CPU and ports is dropped from nominal 5 volts to 0 volt, after the CPU is reset, so that the RAM cells are unaltered by the loss of power. When power is restored, the processor goes through the normal power-on procedure.

#### Battery Charging Circuit

All 48-Series devices contain a circuit to provide external battery charging capabilities. Power for all on-board circuits are provided by  $V_{CC}$  (pin 40). As shown in Figure 5 under normal operating conditions the RESET input is a logic high holding the internal switch in the closed position.  $V_{CC}$  is supplied to the program selectable portion of the RAM array through the closed contact of the internal switch. The normally closed contacts of the switch also provide charging power to the external NiCad cells. In the event of power failure, the RESET pin must be pulled low before  $V_{CC}$  drops below 4.5 volts in order to guarantee the RAM will not lose data. When the RESET pin becomes a logic low (0V) the internal switch is forced to the open condition. DC power to sustain the desired RAM data is provided by the two NiCad batteries (approximately 2.2 volts). Normally, approximately 5 volts are required to provide RAM data protection in the event of a power failure. National's innovative advances in NMOS technology provide the user with a RAM that requires 50% less voltage and 10% of the power to protect data during power failure. The on-chip charging circuit and lower RAM power requirements provide the user with a twofold saving; no external circuits required for the battery charging and only 2 NiCad cells as opposed to the normal requirement of 4 to 5 NiCad cells.

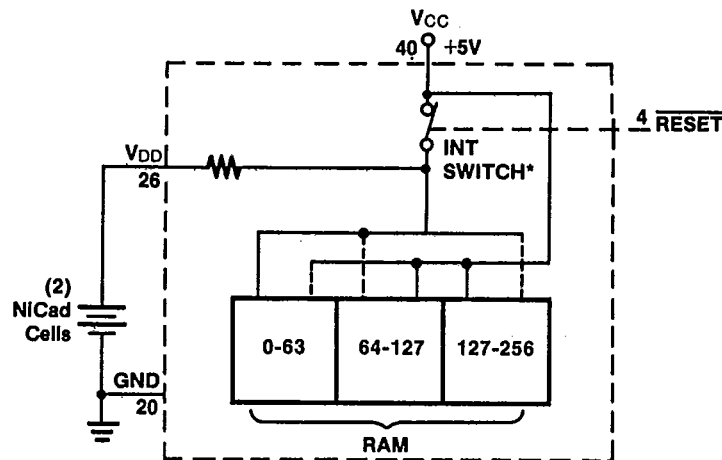


FIGURE 5. INS8049 Battery Charging Circuit

12-5

6501128 NATL SEMICOND, (UP/UC)

18C 32853

D T-49-19-59

T-49-19-05

**Instruction Set**

Table 1 details the 96 instructions common to both the microcomputers and the microprocessors. The table provides the mnemonic, function and description, instruction code, number of cycles and, where applicable, flag settings.

**Table 1 Instruction Set**

| MNEMONIC        | FUNCTION  | DESCRIPTION   | CYCLES | BYTES | FLAGS |   |    |    |
|-----------------|---|---|--------|-------|-------|---|----|----|
|                 |   |   |        |       | C     | A | F0 | F1 |
| CONTROL         |   |   |        |       |       |   |    |    |
| EN I            |   | Enable the External Interrupt input.  | 1      | 1     |       |   |    |    |
| DIS I           |   | Disable the External Interrupt input.   | 1      | 1     |       |   |    |    |
| ENT0 CLK        |   | Enable T0 as the Clock Output.  | 1      | 1     |       |   |    |    |
| SEL MB0         | (DBF) ← 0   | Select Bank 0 (locations 0 - 2047) of Program Memory.   | 1      | 1     |       |   |    |    |
| SEL MB1         | (DBF) ← 1   | Select Bank 1 (locations 2048 - 4095) of Program Memory.  | 1      | 1     |       |   |    |    |
| SEL RB0         | (BS) ← 0  | Select Bank 0 (locations 0 - 7) of Data Memory.   | 1      | 1     |       |   |    |    |
| SEL RB1         | (BS) ← 1  | Select Bank 1 (locations 24 - 31) of Data Memory.   | 1      | 1     |       |   |    |    |
| DATA MOVES      |   |   |        |       |       |   |    |    |
| MOV A, #data    | (A) ← data  | Move Immediate the specified data into the Accumulator.   | 2      | 2     |       |   |    |    |
| MOV A, Rr       | (A) ← (Rr); r = 0 - 7                                 | Move the contents of the designated registers into the Accumulator.   | 1      | 1     |       |   |    |    |
| MOV A, @ Rr     | (A) ← ((Rr)); r = 0 - 1                               | Move Indirect the contents of data memory location into the Accumulator.  | 1      | 1     |       |   |    |    |
| MOV A, PSW      | (A) ← (PSW)   | Move contents of the Program Status Word into the Accumulator.  | 1      | 1     |       |   |    |    |
| MOV Rr, #data   | (Rr) ← data; r = 0 - 7                                | Move Immediate the specified data into the designated register.   | 2      | 2     |       |   |    |    |
| MOV Rr, A       | (Rr) ← (A); r = 0 - 7                                 | Move Accumulator contents into the designated register.   | 1      | 1     |       |   |    |    |
| MOV @ Rr, A     | ((Rr)) ← (A); r = 0 - 1                               | Move Indirect Accumulator contents into data memory location.   | 1      | 1     |       |   |    |    |
| MOV @ Rr, #data | ((Rr)) ← data; r = 0 - 1                              | Move Immediate the specified data into data memory.   | 2      | 2     |       |   |    |    |
| MOV PSW, A      | (PSW) ← (A)   | Move contents of Accumulator into the Program Status Word.  | 1      | 1     |       |   | •  | •  |
| MOVP A, @ A     | (PC 0 - 7) ← (A)<br>(A) ← ((PC))                      | Move the content of program memory location in the current page addressed by the content of accumulator into the accumulator. | 2      | 1     |       |   |    |    |
| MOVP3 A, @ A    | (PC 0 - 7) ← (A)<br>(PC 8 - 10) ← 011<br>(A) ← ((PC)) | Move the content of program memory location in page 3 address by the content of accumulator into the accumulator.             | 2      | 1     |       |   |    |    |
| MOVX A, @ R     | (A) ← ((Rr)); r = 0 - 1                               | Move Indirect the contents of external data memory into the Accumulator.  | 2      | 1     |       |   |    |    |

6501128 NATL SEMICOND, (UP/UC)

18C 32854 D

T-49-19-59

T-49-19-05

Table 1. Instruction Set (Cont'd.)

| MNEMONIC             | FUNCTION                                  | DESCRIPTION  | CYCLES | BYTES | FLAGS |   |    |    |
|----------------------|---|--|--------|-------|-------|---|----|----|
|                      |   |  |        |       | C     | A | F0 | F1 |
| DATA MOVES (Cont'd.) |   |  |        |       |       |   |    |    |
| MOVX @R, A           | ((Rr)) ← (A); r = 0 - 1                   | Move Indirect the contents of the Accumulator into external data memory.         | 2      | 1     |       |   |    |    |
| XCH A, Rr            | (A) ↔ (Rr); r = 0 - 7                     | Exchange the Accumulator and designated register's contents.                     | 1      | 1     |       |   |    |    |
| XCH A, @Rr           | (A) ↔ ((Rr)); r = 0 - 1                   | Exchange Indirect contents of Accumulator and location in data memory.           | 1      | 1     |       |   |    |    |
| XCHD A, @Rr          | (A0 - A3) ↔ (((Rr)) 0 - 3); r = 0 - 1     | Exchange Indirect 4-bit contents of Accumulator and data memory.                 | 1      | 1     |       |   |    |    |
| TIMER COUNTER        |   |  |        |       |       |   |    |    |
| EN TCNTI             |   | Enable Internal Interrupt Flag for Timer/Counter output.                         | 1      | 1     |       |   |    |    |
| DIS TCNTI            |   | Disable Internal Interrupt Flag for Timer/Counter output.                        | 1      | 1     |       |   |    |    |
| MOV A, T             | (A) ← (T)                                 | Move contents of Timer/Counter into Accumulator.                                 | 1      | 1     |       |   |    |    |
| MOV T, A             | (T) ← (A)                                 | Move contents of Accumulator into Timer/Counter.                                 | 1      | 1     |       |   |    |    |
| STOP TCNT            |   | Stop Count for Event Counter.  | 1      | 1     |       |   |    |    |
| STRT CNT             |   | Start Count for Event Counter.   | 1      | 1     |       |   |    |    |
| STRT T               |   | Start Count for Timer.   | 1      | 1     |       |   |    |    |
| ACCUMULATOR          |   |  |        |       |       |   |    |    |
| ADD A, #data         | (A) ← (A) + data                          | Add Immediate the specified Data to the Accumulator.                             | 2      | 2     | •     | • |    |    |
| ADD A, Rr            | (A) ← (A) + (Rr)<br>for r = 0 - 7         | Add contents of designated register to the Accumulator.                          | 1      | 1     | •     | • |    |    |
| ADD A, @Rr           | (A) ← (A) + ((Rr))<br>for r = 0 - 1       | Add Indirect the contents the data memory location to the Accumulator.           | 1      | 1     | •     | • |    |    |
| ADDC A, #data        | (A) ← (A) (C) + data                      | Add Immediate with carry the specified data to the Accumulator.                  | 2      | 2     | •     | • |    |    |
| ADDC A, Rr           | (A) ← (A) + (C) + (Rr)<br>for r = 0 - 7   | Add with carry the contents of the designated register to the Accumulator.       | 1      | 1     | •     | • |    |    |
| ADDC A, @Rr          | (A) ← (A) + (C) + ((Rr))<br>for r = 0 - 1 | Add Indirect with carry the contents of data memory location to the Accumulator. | 1      | 1     | •     | • |    |    |
| ANL A, #data         | (A) ← (A) AND data                        | Logical AND specified Immediate Data with Accumulator.                           | 2      | 2     |       |   |    |    |
| ANL A, Rr            | (A) ← (A) AND (Rr)<br>for r = 0 - 7       | Logical AND contents of designated register with Accumulator.                    | 1      | 1     |       |   |    |    |
| ANL A, @Rr           | (A) ← (A) AND ((Rr))<br>for r = 0 - 1     | Logical AND Indirect the contents of data memory with Accumulator.               | 1      | 1     |       |   |    |    |
| CPL A                | (A) ← NOT (A)                             | Complement the contents of the Accumulator.                                      | 1      | 1     |       |   |    |    |
| CLR A                | (A) ← 0                                   | CLEAR the contents of the Accumulator.   | 1      | 1     |       |   |    |    |
| DA A                 |   | DECIMAL ADJUST the contents of the Accumulator.                                  | 1      | 1     | •     |   |    |    |
| DEC A                | (A) ← (A) - 1                             | DECREMENT by 1 the accumulator's contents.                                       | 1      | 1     |       |   |    |    |
| INC A                | (A) ← (A) + 1                             | Increment by 1 the accumulator's contents  | 1      | 1     |       |   |    |    |
| ORL A, #data         | (A) ← (A) OR data                         | Logical OR specified immediate data with Accumulator.                            | 2      | 2     |       |   |    |    |
| ORL A, Rr            | (A) ← (A) OR (Rr)<br>for r = 0 - 7        | Logical OR contents of designated register with Accumulator.                     | 1      | 1     |       |   |    |    |
| ORL A, @Rr           | (A) ← (A) OR ((Rr))<br>for r = 0 - 1      | Logical OR Indirect the contents of data memory location with Accumulator.       | 1      | 1     |       |   |    |    |

6501128 NATL SEMICOND, (UP/UC)

18C 32855 D T-49-19-59

T-49-19-05

Table 1. Instruction Set (Cont'd.)

| MNEMONIC              | FUNCTION  | DESCRIPTION   | CYCLES | BYTES | FLAGS |   |    |    |
|-----------------------|---|---|--------|-------|-------|---|----|----|
|                       |   |   |        |       | C     | A | F0 | F1 |
| ACCUMULATOR (Cont'd.) |   |   |        |       |       |   |    |    |
| RLA                   | (An ± 1) ← (An)<br>for n = 0 - 6<br>(A0) ← (A7)                     | Rotate Accumulator left by 1-bit without carry.                                   | 1      | 1     |       |   |    |    |
| RLC A                 | (An ± 1) ← (An); n = 0-6<br>(A0) ← (C)<br>(C) ← (A7)                | Rotate Accumulator left by 1-bit through carry.                                   | 1      | 1     | •     |   |    |    |
| RR A                  | (An) ← (An ± 1); n = 0-6<br>(A7) ← (A0)                             | Rotate Accumulator right by 1-bit without carry.                                  | 1      | 1     |       |   |    |    |
| RRC A                 | (An) ← (An ± 1); n = 0-6<br>(A7) ← (C)<br>(C) ← (A0)                | Rotate Accumulator right by 1-bit through carry.                                  | 1      | 1     | •     |   |    |    |
| SWAP A                | (A4-A7) ↔ (A0 - A3)   | Swap the 2, 4-bit nibbles in the Accumulator.                                     | 1      | 1     |       |   |    |    |
| XRL A, #data          | (A) ← (A) XOR data  | Logical XOR immediate specified data with Accumulator.                            | 2      | 2     |       |   |    |    |
| XRL A, Rr             | (A) ← (A) XOR (Rr)<br>for r = 0 - 7                                 | Logical XOR contents of designated register with Accumulator.                     | 1      | 1     |       |   |    |    |
| XRL A, @ Rr           | (A) ← (A) XOR ((Rr))<br>for r = 0 - 1                               | Logical XOR Indirect the contents of data memory location with Accumulator.       | 1      | 1     |       |   |    |    |
| BRANCH                |   |   |        |       |       |   |    |    |
| DJNZ Rr, addr         | (Rr) ← (Rr) - 1; r = 0-7<br>if (Rr) ≠ 0;<br>(PC ± 0-7) ← addr       | Decrement the specified register and test contents.                               | 2      | 2     |       |   |    |    |
| JBb addr              | (PC ± 0-7) ← addr if Bb = 1<br>(PC) ← (PC) + 2 if Bb = 0            | Jump to specified address if Accumulator bit is set.                              | 2      | 2     |       |   |    |    |
| JC addr               | (PC ± 0-7) ← addr if C = 1<br>(PC) ← (PC) + 2 if C = 0              | Jump to specified address if carry flag is set.                                   | 2      | 2     |       |   |    |    |
| JF0 addr              | (PC ± 0-7) ← addr if F0 = 1<br>(PC) ← (PC) + 2 if F0 = 0            | Jump to specified address if Flag F0 is set.                                      | 2      | 2     |       |   |    |    |
| JF1 addr              | (PC ± 0-7) ← addr if F1 = 1<br>(PC) ← (PC) + 2 if F1 = 0            | Jump to specified address if Flag F1 is set.                                      | 2      | 2     |       |   |    |    |
| JMP addr              | (PC ± 8-10) ← addr 8-10<br>(PC ± 0-7) ← addr 0-7<br>(PC ± 11) ← DBF | Direct Jump to specified address within the 2K address block.                     | 2      | 2     |       |   |    |    |
| JMPP @ A              | (PC ± 0-7) ← ((A))  | Jump indirect to specified address pointed to by the accumulator in current page. | 2      | 1     |       |   |    |    |
| JNC addr              | (PC ± 0-7) ← addr if C = 0<br>(PC) ← (PC) + 2 if C = 1              | Jump to specified address if carry flag is low.                                   | 2      | 2     |       |   |    |    |
| JNI addr              | (PC ± 0-7) ← addr if I = 0<br>(PC) ← (PC) + 2 if I = 1              | Jump to specified address if Interrupt is low.                                    | 2      | 2     |       |   |    |    |
| JNT0 addr             | (PC ± 0-7) ← addr if T0 = 0<br>(PC) ← (PC) + 2 if T0 = 1            | Jump to specified address if Test 0 is low.                                       | 2      | 2     |       |   |    |    |
| JNT1 addr             | (PC ± 0-7) ← addr if T1 = 0<br>(PC) ← (PC) + 2 if T1 = 1            | Jump to specified address if Test 1 is low.                                       | 2      | 2     |       |   |    |    |
| JNZ addr              | (PC ± 0-7) ← addr if A ≠ 0<br>(PC) ← (PC) + 2 if A = 0              | Jump to specified address if accumulator is non-zero.                             | 2      | 2     |       |   |    |    |
| JTF addr              | (PC ± 0-7) ← addr if TF = 1<br>(PC) ← (PC) + 2 if TF = 0            | Jump to specified address if Timer Flag is set to 1.                              | 2      | 2     |       |   |    |    |
| JT0 addr              | (PC ± 0-7) ← addr if T0 = 1<br>(PC) ← (PC) + 2 if T0 = 0            | Jump to specified address if Test 0 is a 1.                                       | 2      | 2     |       |   |    |    |
| JT1 addr              | (PC ± 0-7) ← addr if T1 = 1<br>(PC) ← (PC) + 2 if T1 = 0            | Jump to specified address if Test 1 is a 1.                                       | 2      | 2     |       |   |    |    |
| JZ addr               | (PC ± 0-7) ← addr if A = 0<br>(PC) ← (PC) + 2 if A = 1              | Jump to specified address if Accumulator is 0.                                    | 2      | 2     |       |   |    |    |

6501128 NATL SEMICOND, (UP/UC)

18C 32856

D

T-49-19-59

T-49-19-05

Table 1. Instruction Set (Cont'd.)

| MNEMONIC       | FUNCTION   | DESCRIPTION   | CYCLES | BYTES | FLAGS |   |    |    |
|----------------|--|---|--------|-------|-------|---|----|----|
|                |  |   |        |       | C     | A | F0 | F1 |
| INPUT/OUTPUT   |  |   |        |       |       |   |    |    |
| ANL BUS, data  | (BUS) ← (BUS) AND data   | Logical AND Immediate specified data with contents of BUS.          | 2      | 2     |       |   |    |    |
| ANL Pp, data   | (Pp) ← (Pp) AND data; p 1 - 2  | Logical AND immediate specified data with designated port (1 or 2). | 2      | 2     |       |   |    |    |
| ANLD Pp, A     | (Pp) ← (Pp) AND (A0 - A3); p 4-7   | Logical AND contents of Accumulator with designated port (4 - 7).   | 2      | 1     |       |   |    |    |
| IN A, Pp       | (A) ← (Pp); p 1-2  | Input data from designated port (1 - 2) into Accumulator.           | 2      | 1     |       |   |    |    |
| INS A, BUS     | (A) ← (BUS)  | Input strobed BUS data into Accumulator                             | 2      | 1     |       |   |    |    |
| MOVD A, Pp     | (A0-A3) ← (Pp); p 4-7 (A4-A7) ← 0  | Move contents of designated port (4 - 7) into Accumulator.          | 2      | 1     |       |   |    |    |
| MOVD Pp, A     | (Pp) ← (A0 - A3); p 4 - 7  | Move contents of Accumulator to designated port (4 - 7).            | 2      | 1     |       |   |    |    |
| ORL BUS, #data | (BUS) ← (BUS) OR data  | Logical OR Immediate specified data with contents of BUS.           | 2      | 2     |       |   |    |    |
| ORLD Pp, A     | (Pp) ← (Pp) OR (A0 - A3); p 4-7.   | Logical OR contents of Accumulator with designated port (4 - 7).    | 2      | 1     |       |   |    |    |
| ORL Pp, #data  | (Pp) ← (Pp) OR data; p 1 - 2.  | Logical OR Immediate specified data with designated port (1 - 2).   | 2      | 2     |       |   |    |    |
| OUTL BUS, A    | (BUS) ← (A)  | Output contents of Accumulator onto BUS.                            | 2      | 1     |       |   |    |    |
| OUTL Pp, A     | (Pp) ← (A); p 1 - 2  | Output contents of Accumulator to designated port (1 - 2).          | 1      | 1     |       |   |    |    |
| REGISTERS      |  |   |        |       |       |   |    |    |
| DEC Rr         | (Rr) ← (Rr) -1; r 0-7  | Decrement by 1 contents of designated register.                     | 1      | 1     |       |   |    |    |
| INC Rr         | (Rr) ← (Rr) +1; r 0-7  | Increment by 1 contents of designated register.                     | 1      | 1     |       |   |    |    |
| INC @ Rr       | ((Rr)) ← ((Rr)) + 1; r 0-1.  | Increment Indirect by 1 the contents of data memory location.       | 1      | 1     |       |   |    |    |
| SUBROUTINE     |  |   |        |       |       |   |    |    |
| CALL addr      | ((SP)) ← (PC)<br>((SP)) ← (PSW 4-7)<br>(SP) ← (SP) + 1<br>(PC8-10) ← addr 8-10<br>(PC 0-7) ← addr 0-7<br>(PC 11) ← DBF | Call designated Subroutine.   | 2      | 2     |       |   |    |    |
| RET            | (SP) ← (SP) - 1<br>(PC) ← ((SP))   | Return from Subroutine without restoring Program Status Word.       | 2      | 1     |       |   |    |    |
| RETR           | (SP) ← (SP) - 1<br>(PC) ← ((SP))<br>(PSW 4-7) ← ((SP))   | Return from Subroutine restoring Program Status Word.               | 2      | 1     | •     | • |    |    |
| FLAGS          |  |   |        |       |       |   |    |    |
| CPL C          | (C) ← NOT (C)  | Complement Content of carry bit.                                    | 1      | 1     | •     |   |    |    |
| CPL F0         | (F0) ← NOT (F0)  | Complement Content of Flag F0.                                      | 1      | 1     |       |   | •  |    |
| CPL F1         | (F1) ← NOT (F1)  | Complement Content of Flag F1.                                      | 1      | 1     |       |   |    | •  |
| CLR C          | (C) ← 0  | Clear content of carry bit to 0.                                    | 1      | 1     | •     |   |    |    |
| CLR F0         | (F0) ← 0.  | Clear content of Flag 0 to 0.                                       | 1      | 1     |       |   | •  |    |
| CLR F1         | (F1) ← 0   | Clear content of Flag 1 to 0.                                       | 1      | 1     |       |   |    | •  |
| MISCELLANEOUS  |  |   |        |       |       |   |    |    |
| NOP            |  | No operation  | 1      | 1     |       |   |    |    |

6501128 NATL SEMICOND, (UP/UC)

18C 32857

D T-49-19-59

T-49-19-05

## Symbol Definitions

| SYMBOL                        | DESCRIPTION                      |
|-------------------------------|----------------------------------|
| A                             | The Accumulator                  |
| AC                            | The Auxiliary Carry Flag         |
| addr                          | Program Memory Address (12 bits) |
| b                             | Bit Designator (b = 0 - 7)       |
| BS                            | The Bank Switch                  |
| BUS                           | The BUS Port                     |
| C                             | Carry Flag                       |
| CLK                           | Clock Signal                     |
| CNT                           | Event Counter                    |
| D                             | Nibble Designator (4 bits)       |
| data                          | Number or Expression (8 bits)    |
| DBF                           | Memory Bank Flip-Flop            |
| F <sub>0</sub> F <sub>1</sub> | Flags 0, 1                       |
| I                             | Interrupt                        |
| P                             | "In-Page" Operation Designator   |

| SYMBOL                        | DESCRIPTION   |
|-------------------------------|---|
| p                             | Port Designator (p = 1, 2 or 4 - 7)   |
| PSW                           | Program Status Word   |
| r                             | Register Designator (r = 0, 1 or 0 - 7)   |
| SP                            | Stack Pointer   |
| T                             | Timer   |
| TF                            | Timer Flag  |
| T <sub>0</sub> T <sub>1</sub> | Testable Flags 0, 1   |
| X                             | External RAM  |
| #                             | Prefix for Immediate Data   |
| @                             | Prefix for Indirect Address   |
| \$                            | Program Counter's Current Value   |
| (x)                           | Contents of External RAM Location   |
| ((xx))                        | Contents of Memory Location Addressed by the Contents of External RAM Location. |
| ←                             | Replaced By   |

## TYPICAL APPLICATIONS

Figure 6 shows a typical way to use the 48-Series Micro-computers in a stand-alone system.

■ Crystal used is:

- Series resonant
- AT cut
- 1 to 6 MHz or 4 to 11 MHz

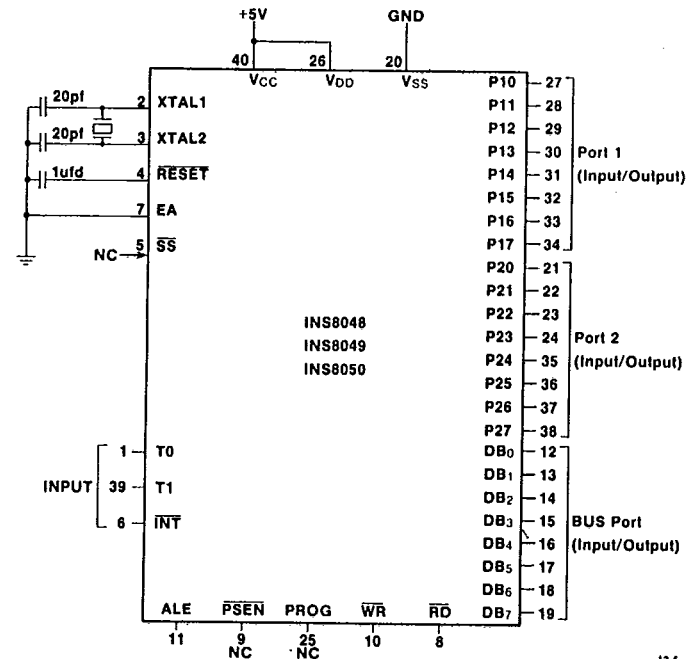


FIGURE 6. Stand-alone INS8048/49/50

6501128 NATL SEMICOND, (UP/UC)

18C 32858

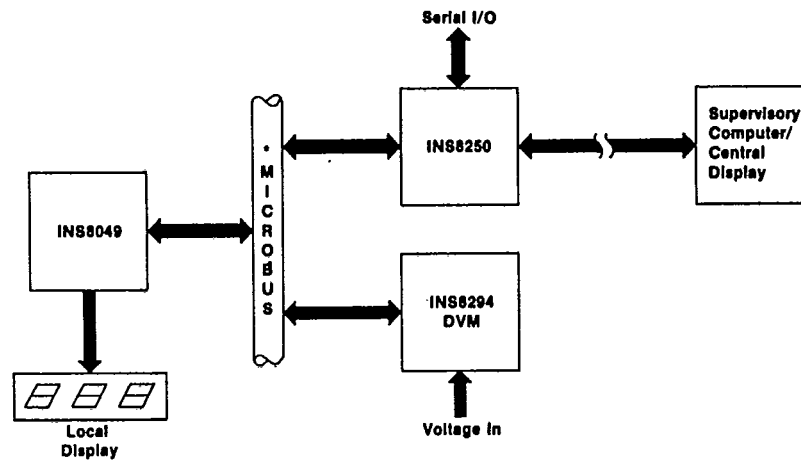
D

T-49-19-59

T-49-19-05

**TYPICAL APPLICATIONS (Cont'd)**

Figure 7 shows a typical remote data acquisition system with an INS8250 Programmable Asynchronous Communication System which can receive commands or update information from a supervisory computer. The figure also shows an INS8294 CMOS DVM that receives data at  $V_{IN}$  and displays the data on the 7-segment local display unit. Data are transferred from the INS8294 to the INS8049 via National's MICROBUS™.

**FIGURE 7. Data Acquisition System**

12-7

**TYPICAL APPLICATIONS (Cont'd)**

Figure 8 shows a typical way to add a Input/Output Expander and Programmable Interval Timer to the 48-Series Microprocessors.



T-49-19.05

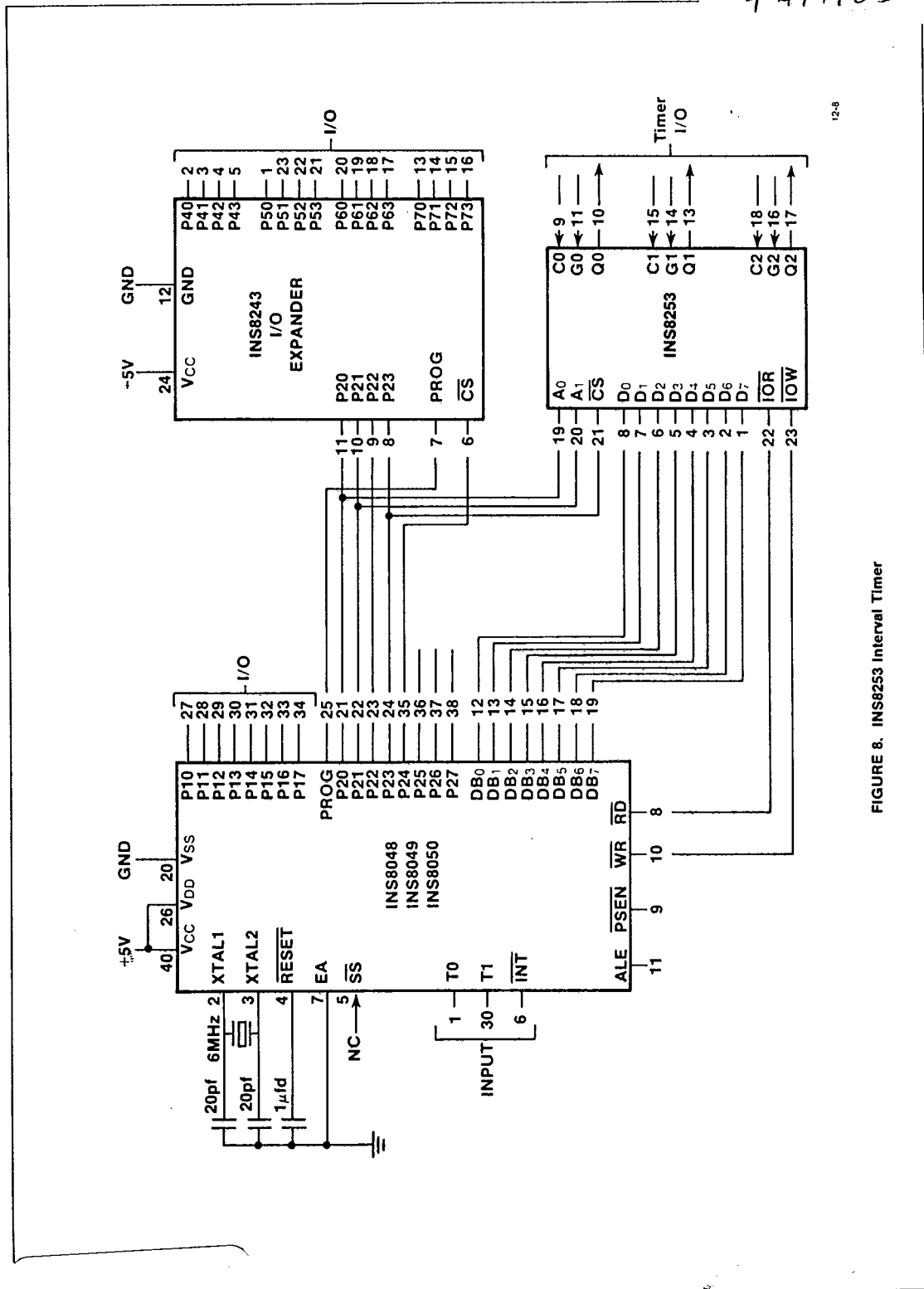


FIGURE 8. INS8253 Interval Timer

6501128 NATL SEMICOND, (UP/UC)

18C 32860

D

T-49-19-59

T-49-19-05

**APPROVED FORMATS FOR CUSTOM PROGRAMMED PARTS****INPUT MEDIUM:**

2716 EPROM  
2708 EPROM  
PAPER TAPE

**IMPORTANT - EPROM LABELLING**

Only one customer program may be included in a single order. The following method must be used to identify the EPROMs comprising a program.

- a. The EPROMs used for storing a custom program are designated as shown:

2716: Block A 0-2047  
2708: Block A 0-1023  
Block B 1024-2047

- b. All EPROMs must be labelled (stickers, paint, etc.) with this block designation plus a customer assigned print or identification number.

**Example:**

- 1) Customer Data
- Custom Program Length - 2K
  - Medium - Two 2708's
  - Customer Print or I.D. No. C123-45

**2) EPROM Labels**

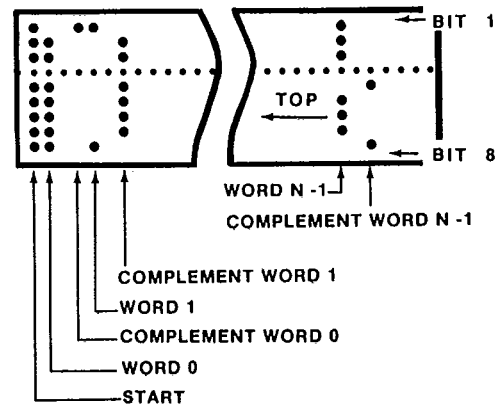
C123-45  
A  
0-1023

C123-45  
B  
1024-2047

**Paper Tape**

Tapes may only be submitted in binary complement format. The following information should be written on the paper tape.

Company Name  
Customer Print or I.D. No.  
NSC Part No.  
A Punch = ("1" or "0")  
This is \_\_\_\_\_ logic (POS or NEG)

**BINARY COMPLEMENT FORMAT**

NOTE 1: Tape must be blank except for the data words.

NOTE 2: Tape must start with a rubout character.

NOTE 3: Data is comprised of two words, the first being the actual data and the second being the complement of the data.

**Verification**

You will receive a listing of the options ordered and the input data. If you also wish to receive EPROMs for verification, please send additional blank EPROMs as necessary for this purpose. You can use software (the listing) or hardware (EPROMs) to verify the program.

You will be asked for a GO/NO GO response within one week after you receive the listing.

**VERIFICATION LISTING**

The verification listing has six sections:

1. A cover sheet with provision for "STOP, DO NOT PROCEED" or "VERIFICATION CERTIFIED" signatures.
2. Description of the options you have chosen.
3. A description of the logic designations and assumptions used to process the data.
4. A listing of the data you have submitted.
5. An error summary.
6. A definition of the standard logic definitions for the ROM and the reduced form of the data. This list shows the output word corresponding to each address coded in binary.

6501128 NATL SEMICOND, (UP/UC)

18C 32861

D

T-49-19-59

T-49-19-05

**Ordering Information for Custom Programmed Parts**

The following information must be submitted with each customer microcomputer program. An order will not be processed unless it is accompanied by this information. This form acts as a Traveler from Customer through Customer Service to ROM programming. Please retain a copy of this form to compare against the verification listing. The form will be sent back to the customer by Customer Service.

|                      |   |
|----------------------|---|
|                      | National Microcomputer Part Number          |
|                      | ROM Letter Code (National Use Only)         |
| Name                 | Date  |
| Address              | Customer Print or I.D. No.                  |
| City State Zip       | Purchase Order No.                          |
| Telephone ( )        | Name of person National can contact (Print) |
| Authorized Signature | Date  |

**OPTIONS****1. Device Type (Circle One)**

8048-6 (6 MHz) 8049-6 8050-6

8048-11 (11 MHz) 8049-11

**B. Verification Medium:** The user will be sent one or more of the following media to verify National's reception of valid date. If any EPROM is selected, blank EPROMs must be submitted with this form.

**Circle One or More****A. Input Medium (Circle One)**48 Series Part: 8048  
8748EPROM: 2708 2716  
2758A 2732  
2758B

Listing: Binary MPS Format EPROM: 2708 2716  
Hexadecimal Format 2758A 2732  
2758B 8748

Total Number of EPROMs: \_\_\_\_\_

Total number of EPROMs: \_\_\_\_\_

6501128 NATL SEMICOND, (UP/UC)

18C 32862

D

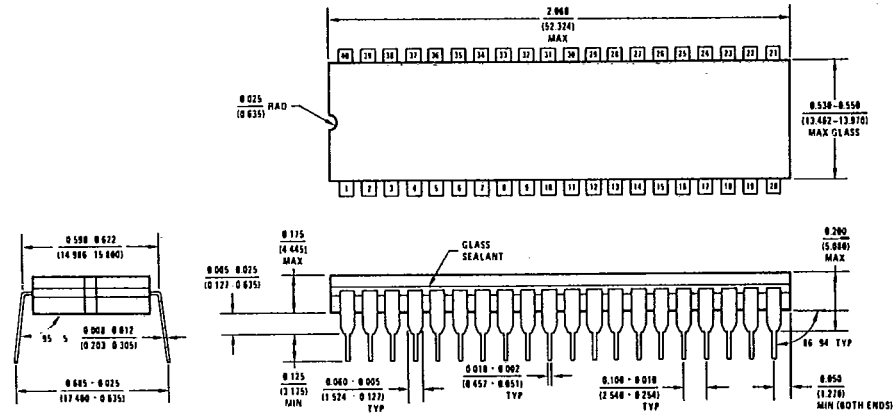
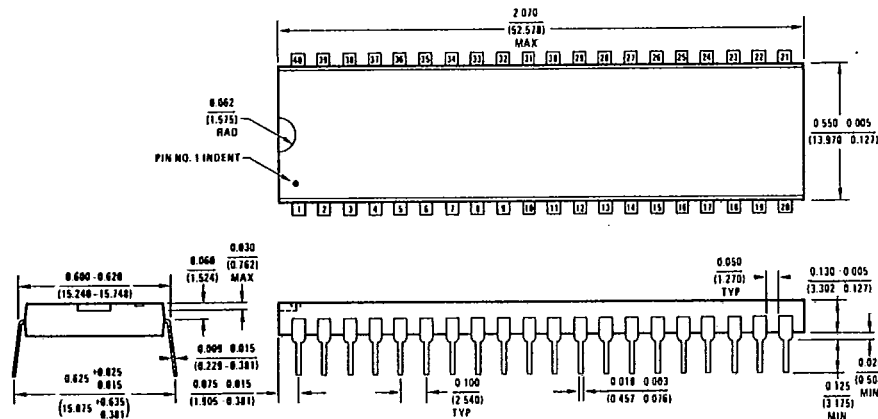
T-49-19-59

T-49-19-05

## INS8048-Series Microcomputer/Microprocessor Family

## Physical Dimensions

inches - millimeters

Ceramic Dual-in-Line Package (J)  
Order Number INS8048JPlastic Dual-in-Line Package (N)  
Order Number INS8048N

National Semiconductor  
Corporation  
2900 Semiconductor Drive  
Santa Clara, California 95051  
Tel (408) 737 5000  
TWX (910) 339 9240

National Semiconductor GmbH  
Lise-Meunier-Strasse 61/11  
8000 München 21  
West Germany  
Tel (089) 576091  
Telex 05 22772

NS International Inc., Japan  
Miyake Building  
1-9 Yotsuya Shinjuku-ku 160  
Tokyo Japan  
Tel (03) 355 3711  
TWX 232 2015 NSCJ J

National Semiconductor  
(Hong Kong) Ltd  
8th Floor  
Cheung Kong Electronic Bldg  
4 Hing Yip Street  
Kwun Tong  
Kowloon Hong Kong  
Tel J 899235  
Telex 73866 NSI HK HX  
Cable NATEL HK

NS Electronics De Brazil  
Avda Brigadier Faria Lima 844  
11 Andar Conjunto 1104  
Jardim Paulistano  
Sao Paulo Brasil  
Telex  
1171008 CABINE SAO PAULO

NS Electronics Pty. Ltd.  
Cnr. Stud Rd. & Min. Highway  
Bayswater Victoria 3153  
Australia  
Tel 03 729 6333  
Telex 37096

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and National reserves the right at any time without notice to change said circuitry.