

International IOR Rectifier

SERIES IRK.170, .230, .250

SCR / SCR and SCR / DIODE

NEW MAGN-A-pak™ Power Modules

INTERNATIONAL RECTIFIER

Features

- High voltage.
- Electrically isolated base plate
- 3000 V_{RMS} isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- Beryllium oxide substrate
- Also available with aluminum nitride substrate

170A
230A
250A

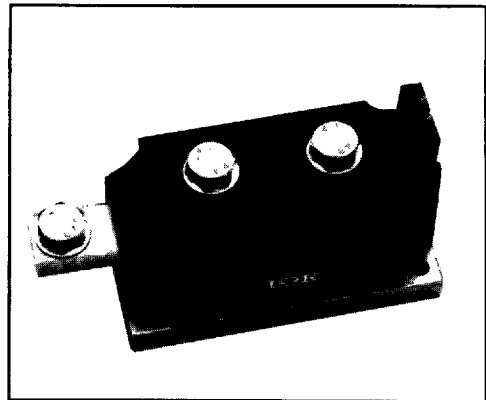
Description

This new IRK serie of MAGN-A-paks modules uses high voltage power thyristor/thyristor and thyristor/diode in seven basic configurations. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel mode.

These modules are intended for general purpose applications such as battery chargers, welders and plating equipment and where high voltage and high current are required (motor drives, U.P.S., etc.).

Major Ratings and Characteristics

Parameters	IRK.170	IRK.230	IRK.250	Units
$I_{T(AV)}$ @ 85°C	170	230	250	A
$I_{T(RMS)}$	377	510	555	A
I_{TSM} @ 50Hz	5100	7500	8500	A
@ 60Hz	5350	7850	8900	A
I^2t @ 50Hz	131	280	361	kA ² s
@ 60Hz	119	256	330	kA ² s
$I^2\sqrt{t}$	1310	2800	3610	kA ² √s
$V_{DRM} - V_{RRM}$	Up to 1600	Up to 2000	Up to 1600	V
T_J	-40 to 130			°C



ELECTRICAL SPECIFICATIONS

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Voltage Ratings

Type number	Voltage Code	V_{RRM} , V_{DRM} , maximum repetitive peak reverse and off-state blocking voltage V	V_{RSM} , maximum non-repetitive peak reverse voltage V	I_{RRM} , I_{DRM} max @ 130°C mA
IRK.170, 230, 250	04	400	500	50
	06	600	700	50
	08	800	900	50
	10	1000	1100	50
	12	1200	1300	50
	14	1400	1500	50
	16	1600	1700	50
IRK.230	18	1800	1900	50
	20	2000	2100	

On-state Conduction

Parameters	IRK.170	IRK.230	IRK.250	Units	Conditions		
$I_{T(AV)}$ Maximum average on-state current @ Case temperature	170	230	250	A	180° conduction, half sine wave		
	85	85	85	°C			
$I_{T(RMS)}$ Maximum RMS on-state current	377	510	555	A	as AC switch		
I_{TSM} Maximum peak, one-cycle on-state, non-repetitive surge current	5100	7500	8500	A	t=10ms	Sinusoidal half wave, Initial $T_J = T_J$ max	
	5350	7850	8900	A	t=8.3ms		No voltage reapplied
	4300	6300	7150	A	t=10ms		100% V_{RRM} reapplied
	4500	6600	7500	A	t=8.3ms		100% V_{RRM} reapplied
I^2t Maximum I^2t for fusing	131	280	361	kA ² s	t=10ms	Sinusoidal half wave, Initial $T_J = T_J$ max	
	119	256	330	kA ² s	t=8.3ms		No voltage reapplied
	92.5	198	255	kA ² s	t=10ms		100% V_{RRM} reapplied
	84.4	181	233	kA ² s	t=8.3ms		100% V_{RRM} reapplied
I^2/t Maximum I^2/t for fusing	1310	2800	3610	kA ² /s	t=0.1 to 10ms, no voltage reapplied		
$V_{T(TO)1}$ Low level value of threshold voltage	0.89	1.03	0.97	V	$(16.7\% \times \pi \times I_{T(AV)}) < I < (\pi \times I_{T(AV)})$	$T_J = T_J$ max.	
$V_{T(TO)2}$ High level value of threshold voltage	1.12	1.07	1.00	V	$(\pi \times I_{T(AV)}) < I < (20 \times \pi \times I_{T(AV)})$	$T_J = T_J$ max.	
$r_{\theta 1}$ Low level on-state slope resistance	1.34	0.77	0.60	mΩ	$(16.7\% \times \pi \times I_{T(AV)}) < I < (\pi \times I_{T(AV)})$	$T_J = T_J$ max.	
$r_{\theta 2}$ High level on-state slope resistance	0.96	0.73	0.57	mΩ	$(\pi \times I_{T(AV)}) < I < (20 \times \pi \times I_{T(AV)})$	$T_J = T_J$ max.	
V_{TM} Maximum on-state voltage drop	1.60	1.59	1.44	V	$I_{TM} = \pi \times I_{T(AV)}$, $T_J = T_J$ max., 180° conduction Av. power = $V_{T(TO)} \times I_{T(AV)} + r_{\theta} \times (I_{T(RMS)})^2$		
I_H Maximum holding current	500	500	500	mA	Anode supply=12V, initial $I_T=30A$, $T_J=25^\circ\text{C}$		
I_L Maximum latching current	1000	1000	1000	mA	Anode supply=12V, resistive load=1Ω gate pulse: 10V, 100μs, $T_J=25^\circ\text{C}$		

Switching

t_d Typical delay time	1.0	1.0	1.0	μs	$T_J = 25^\circ\text{C}$	Gate Current=1A $di_{g}/dt = 1A/\mu\text{s}$
t_r Typical rise time	2.0	2.0	2.0	μs	$T_J = 25^\circ\text{C}$	$V_d = 0.67\% V_{DRM}$
t_q Typical turn-off time	50 - 150			μs	$I_{TM} = 300\text{ A}$; $-di/dt = 15\text{ A}/\mu\text{s}$; $T_J = T_J$ max; $V_r = 50\text{ V}$; $dV/dt = 20\text{ V}/\mu\text{s}$; Gate 0V, 100 ohm	

Blocking

I_{RRM} Max. peak reverse and off-state leakage current	50		mA	$T_J = T_J$ max.
V_{INS} RMS isolation voltage	3000		V	50Hz, circuit to base, all termin. shorted, 25°C, 1s
dv/dt Critical rate of rise of off-state voltage	500		V/μs	$T_J = T_J$ max, linear to 80% rated V_{DRM}
	1000		V/μs	$T_J = T_J$ max, linear to 67% rated V_{DRM}

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Triggering

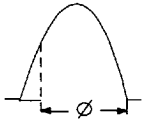
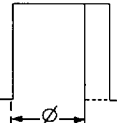
P_{GM}	Maximum peak gate power	10.0	W	$t_p \leq 5ms$, $T_J = T_J \text{ max.}$
$P_{G(AV)}$	Maximum average gate power	2.0	W	$f = 50Hz$, $T_J = T_J \text{ max.}$
$+I_{GM}$	Maximum peak gate current	3.0	A	$t_p \leq 5ms$, $T_J = T_J \text{ max.}$
$-V_{GT}$	Max. peak negative gate voltage	5.0	V	$t_p \leq 5ms$, $T_J = T_J \text{ max.}$
V_{GT}	Maximum required DC gate voltage to trigger	4.0	V	$T_J = -40^\circ C$
		3.0	V	$T_J = 25^\circ C$
		2.0	V	$T_J = T_J \text{ max.}$
I_{GT}	Maximum required DC gate current to trigger	350	mA	$T_J = -40^\circ C$
		200	mA	$T_J = 25^\circ C$
		100	mA	$T_J = T_J \text{ max.}$
V_{GD}	Maximum gate voltage that will not trigger	0.25	V	@ $T_J = T_J \text{ max.}$, rated V_{DRM} applied
I_{GD}	Maximum gate current that will not trigger	10.0	mA	@ $T_J = T_J \text{ max.}$, rated V_{DRM} applied
di/dt	Max rate of rise of turned-on current	500	A/ μs	@ $T_J = T_J \text{ max.}$, $I_{TM} = 400 A$ rated V_{DRM} applied

Thermal and Mechanical Specifications

T_J	Junction operating temperature	-40 to 130			$^\circ C$	
T_{stg}	Storage temperature range	-40 to 150			$^\circ C$	
R_{thJC}	Maximum thermal resistance junction to case	0.17	0.125	0.125	K/W	Per junction, DC operation
R_{thc-s}	Thermal resistance, case to heatsink	0.02	0.02	0.02	K/W	Mounting surface flat, smooth and greased (per module)
T Mounting tourque $\pm 10\%$	MAGN-A-pak to heatsink	4 to 6			Nm	A mounting compound is recommended and the tourque should be rechecked after a period of about 3 hours to allow for the spread of the compound
	Busbar to MAGN-A-pak	8 to 10			Nm	
wt	Approximate weight	500			g	
		17.8			oz	
Case style		MAGN-A-pak				

 ΔR Conduction (per Junction)

(The following table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC)

Conduction angle	IRK.170	IRK.230	IRK.250	Units	Conditions
	180°	0.009	0.009	0.009	K/W $T_J = T_J \text{ max.}$
	120°	0.010	0.010	0.010	
	90°	0.010	0.010	0.014	
	60°	0.020	0.020	0.020	
	30°	0.032	0.032	0.032	
	180°	0.007	0.007	0.007	K/W $T_J = T_J \text{ max.}$
	120°	0.011	0.011	0.011	
	90°	0.015	0.015	0.015	
	60°	0.020	0.020	0.020	
	30°	0.033	0.033	0.033	

MAGN-A-paks Suitable for Current Source Inverters

Thyristor		Diode	$I_{T(AV)} / I_{F(AV)} @ T_C$		
V_{DRM}	V_{RSM}	V_{RRM}	170A	230A	250A
V_{RRM} 1400	1500	V_{RSM} 2000	@ 85°C IRKH170-14D20	@ 85°C IRKH230-14D20	@ 85°C IRKH250-14D20
1400	1500	2000	IRKL170-14D20	IRKL230-14D20	IRKL250-14D20
1600	1700	2500	IRKH170-16D25	IRKH230-16D25	IRKH250-16D25
1600	1700	2500	IRKL170-16D25	IRKL230-16D25	IRKL250-16D25
1800	1900	2800	Not Available	IRKH230-18D28	Not Available
1800	1900	2800	Not Available	IRKL230-18D28	Not Available
2000	2100	3200	Not Available	IRKH230-20D32	Not Available
2000	2100	3200	Not Available	IRKL230-20D32	Not Available

For all other parameters and characteristics refer to standard IRKH... and IRKL... modules.

Application Notes

3 x IRKT...

3 x IRKL...

3 x IRKH...

M

Current Source Inverters

Current-Source Inverters (also known as Sequentially Commutated Inverters) use Phase Control (as opposed to Fast) Thyristors and Diodes.

The advantages of Current Source Inverters lie in their ease control, absence of large commutation inductances and limited fault currents. Their simple construction, illustrated by the circuit on the left, is further enhanced by the use of MAGN-A-paks which allow the power circuit of an Inverter to be realised with 6 capacitors and 9 MAGN-A-paks all mounted on just one heatsink.

The optimal design of Current Source Inverters requires the use of Diodes with blocking voltages greater than those of the thyristors. This departure from conventional half-bridge modules is catered for by MAGN-A-pak range with Thyristors up to 2000V and Diodes up to 3200V.

Current Source Inverter using 9 MAGN-A-paks

Ordering Information Table

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Device Code

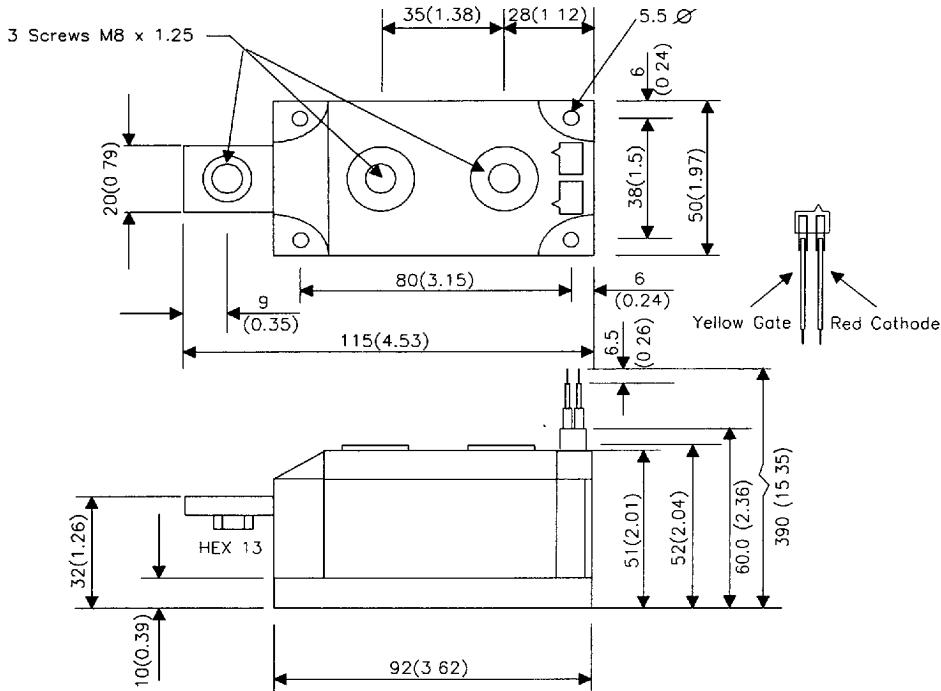
IRK	T	250	-	14	D20	N
①	②	③	④	⑤	⑥	

- 1** - Module type
- 2** - Circuit configuration (See Outline Table)
- 3** - Current rating
- 4** - Voltage code: Code x 100 = V_{RRM} (See Voltage Ratings Table)
- 5** - Current Source Inverters Types
- 6** - None = Standard devices (beryllium oxide)
N = aluminium nitride substrate (Contact factory)

Outline Table

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CONTAINS BERYLLIUM OXIDE CERAMIC

- May contain Beryllium Oxide Ceramic, and under normal circumstances is non hazardous
- Do not open, cut or grind.
- Unserviceable parts must be disposed of as harmful waste.

HARMFUL

- All dimensions in millimeters (inches)
- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94V0

IRKT...

IRKH...

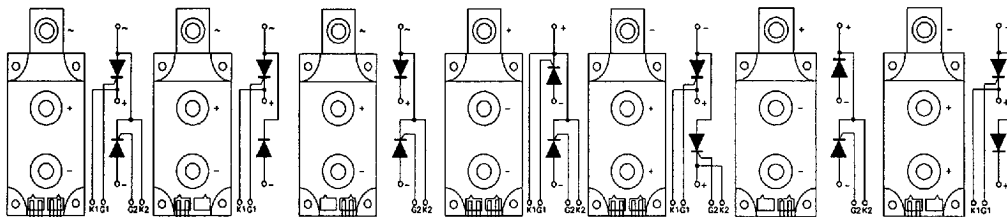
IRKL...

IRKU...

IRKV...

IRKK...

IRKN...



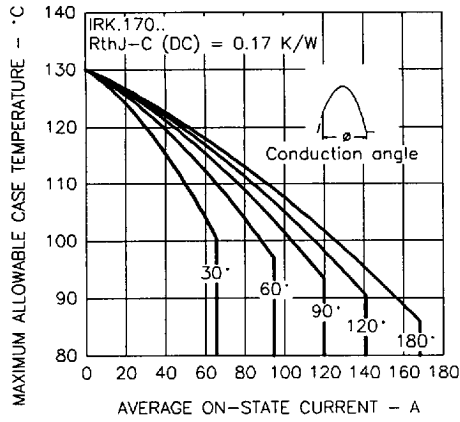


Fig. 1 - Current Ratings Characteristics

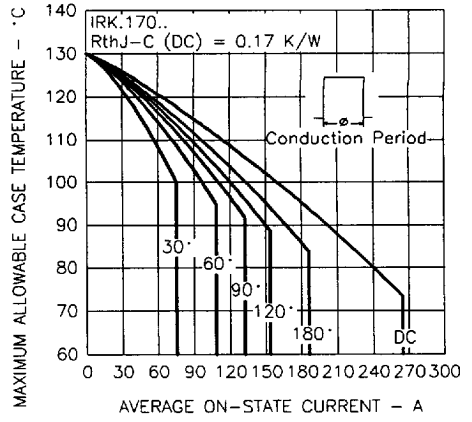


Fig. 2 - Current Ratings Characteristics

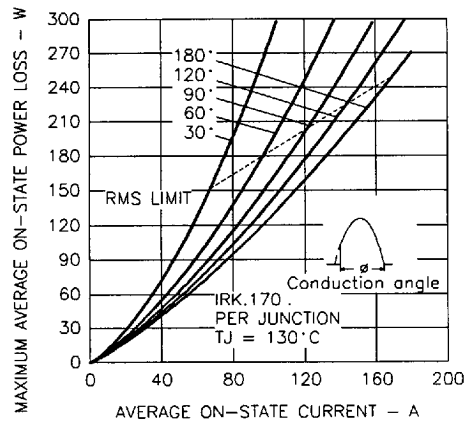


Fig. 3 - On-state Power Loss Characteristics

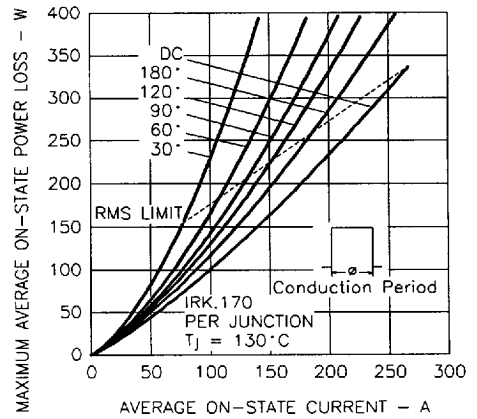


Fig. 4 - On-state Power Loss Characteristics

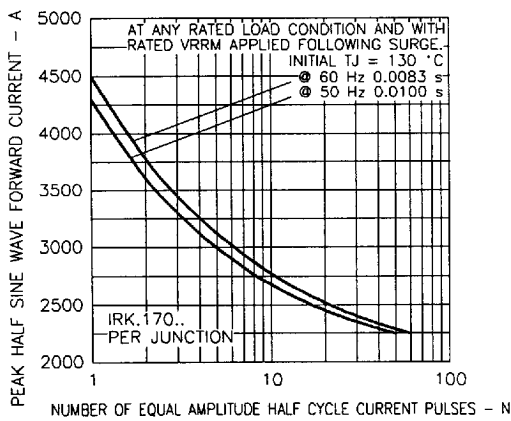


Fig. 5 - Maximum Non-Repulsive Surge Current

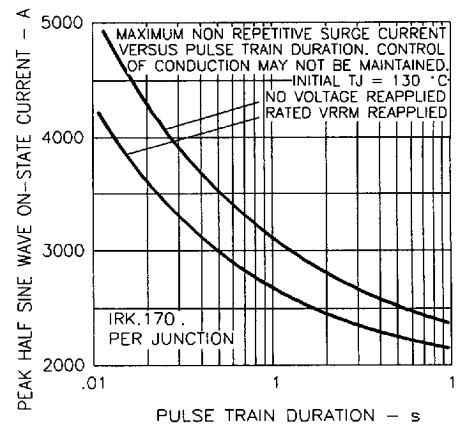


Fig. 6 - Maximum Non-Repulsive Surge Current

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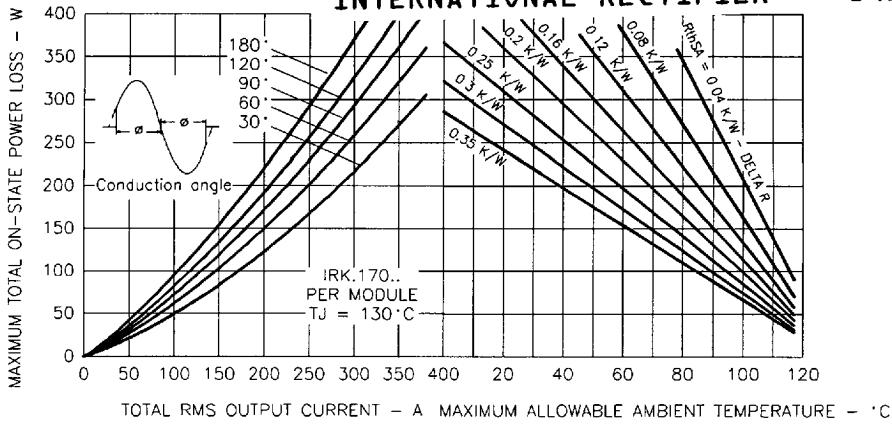


Fig. 7 - On-state Power Loss Characteristics

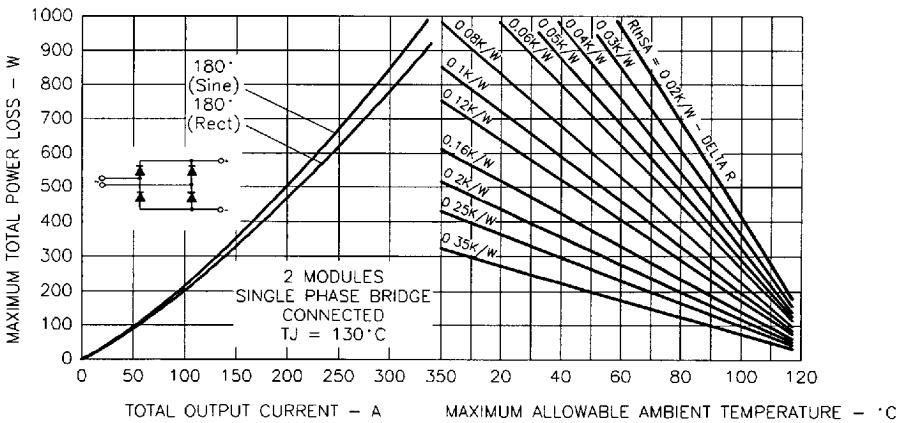


Fig. 8 - On-state Power Loss Characteristics

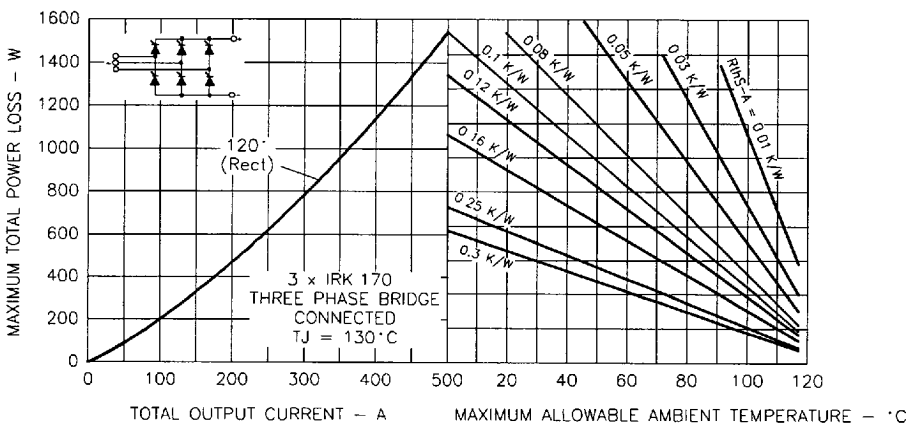


Fig. 9 - On-state Power Loss Characteristics

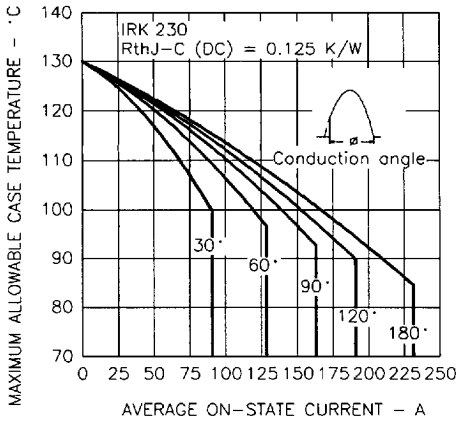


Fig. 10 - Current Ratings Characteristics

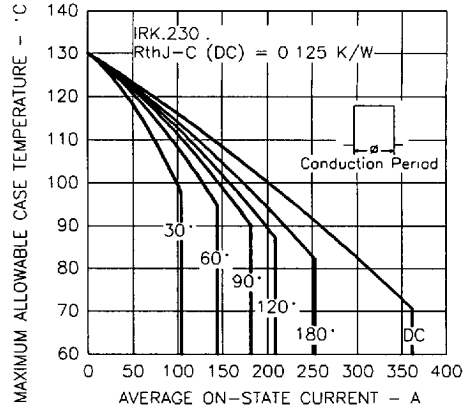


Fig. 11 - Current Ratings Characteristics

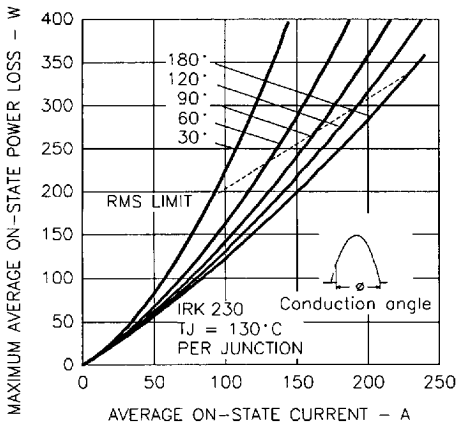


Fig. 12 - On-state Power Loss Characteristics

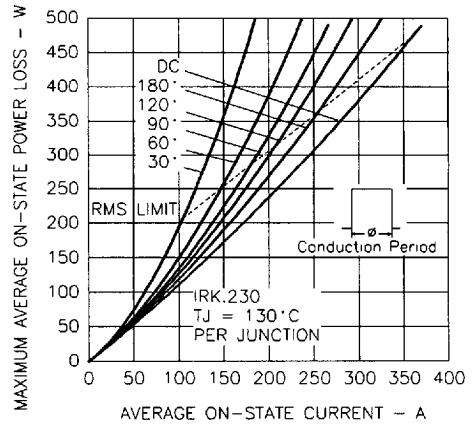


Fig. 13 - On-state Power Loss Characteristics

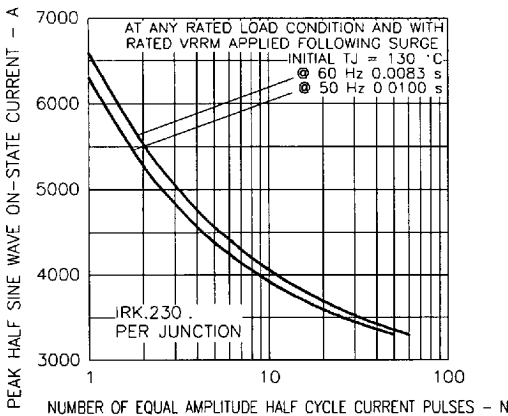


Fig. 14 - Maximum Non-Repetitive Surge Current

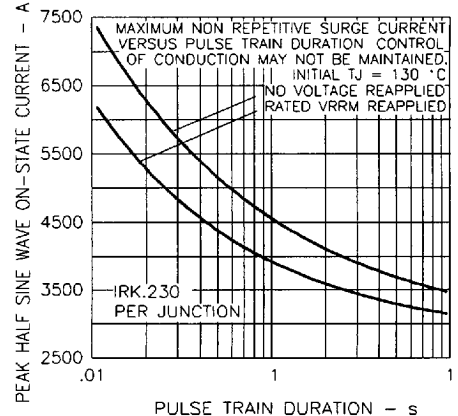


Fig. 15 - Maximum Non-Repetitive Surge Current

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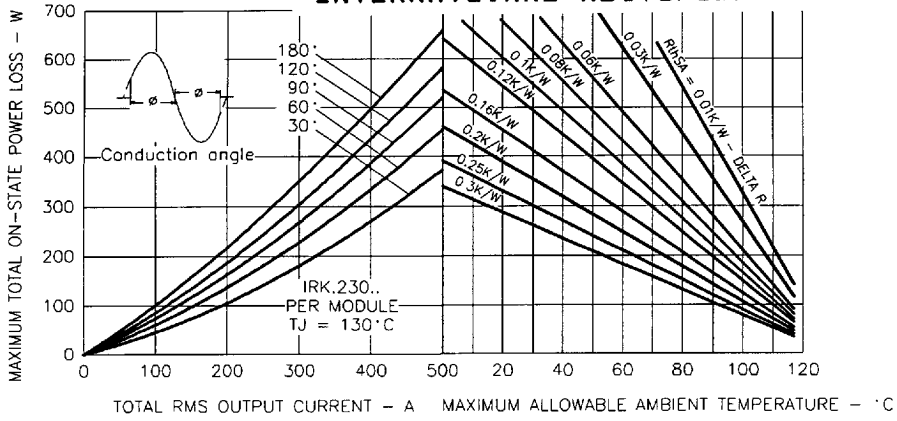


Fig. 16 - On-state Power Loss Characteristics

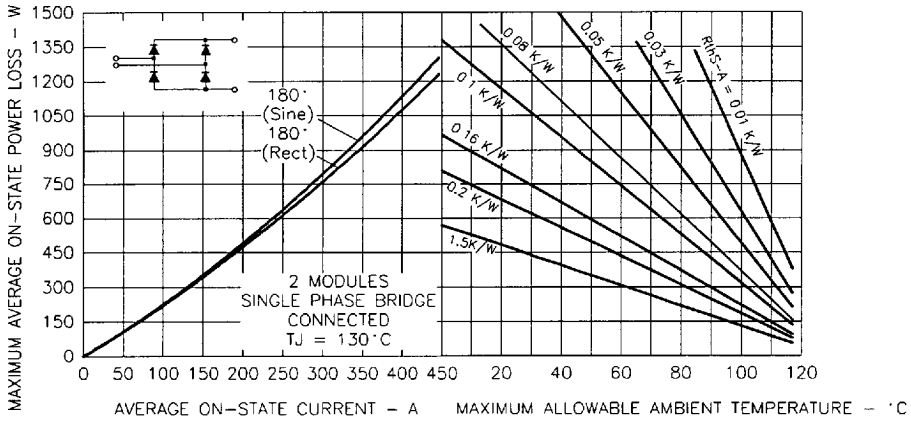


Fig. 17 - On-state Power Loss Characteristics

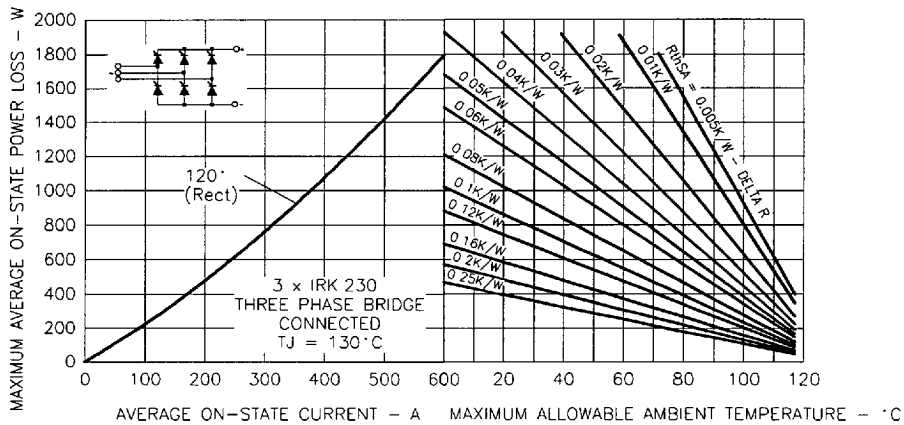


Fig. 18 - On-state Power Loss Characteristics

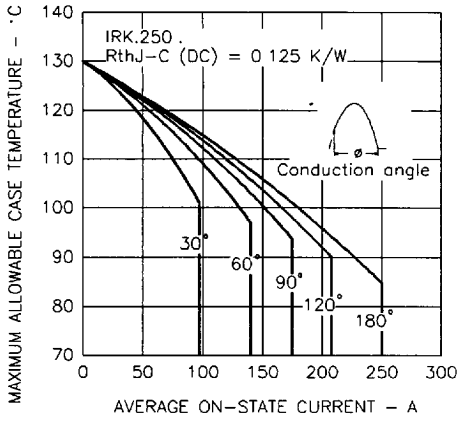


Fig. 19 - Current Ratings Characteristics

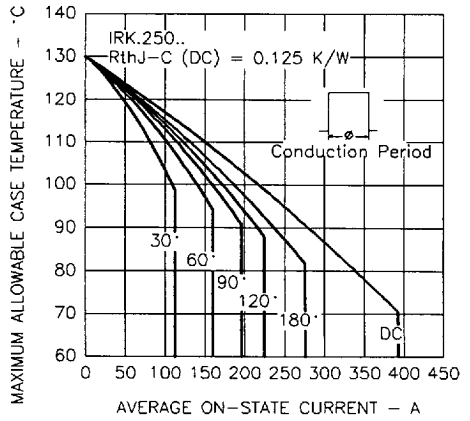


Fig. 20 - Current Ratings Characteristics

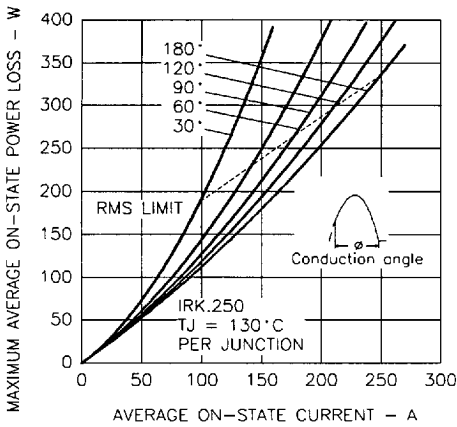


Fig. 21 - On-state Power Loss Characteristics

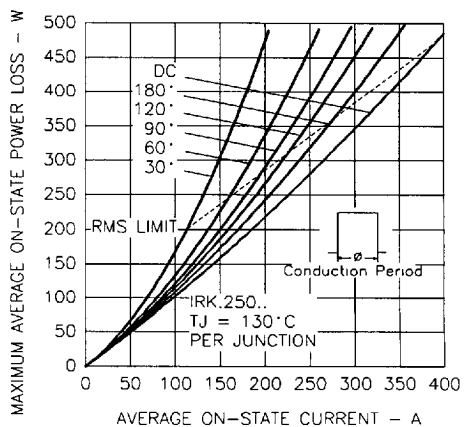


Fig. 22 - On-state Power Loss Characteristics

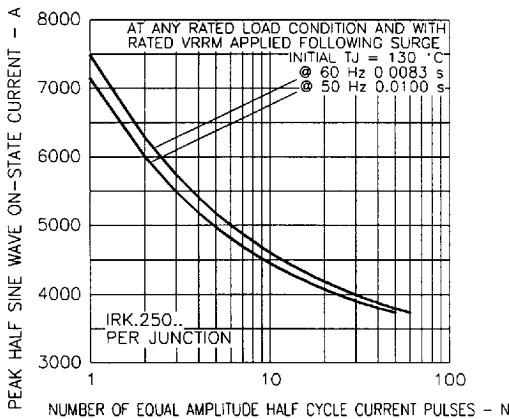


Fig. 23 - Maximum Non-Repetitive Surge Current

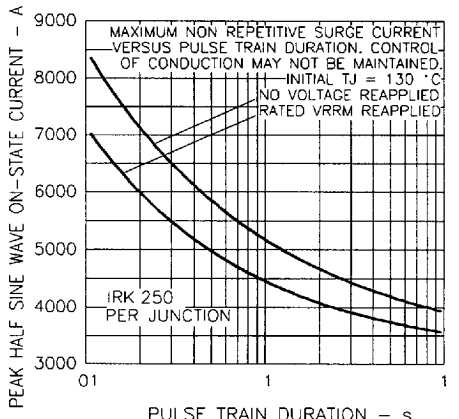


Fig. 24 - Maximum Non-Repetitive Surge Current

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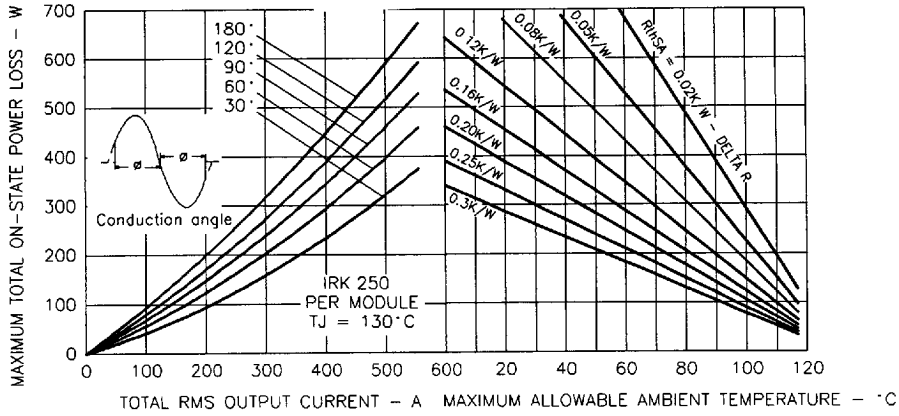


Fig.25 - On-state Power Loss Characteristics

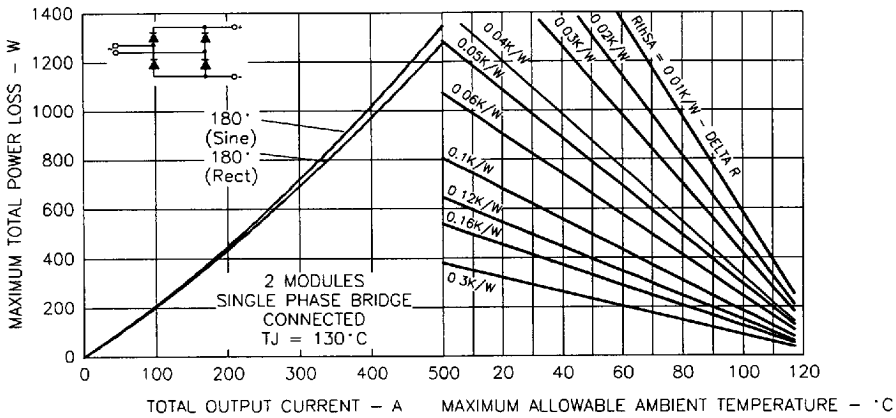


Fig.26 - On-state Power Loss Characteristics

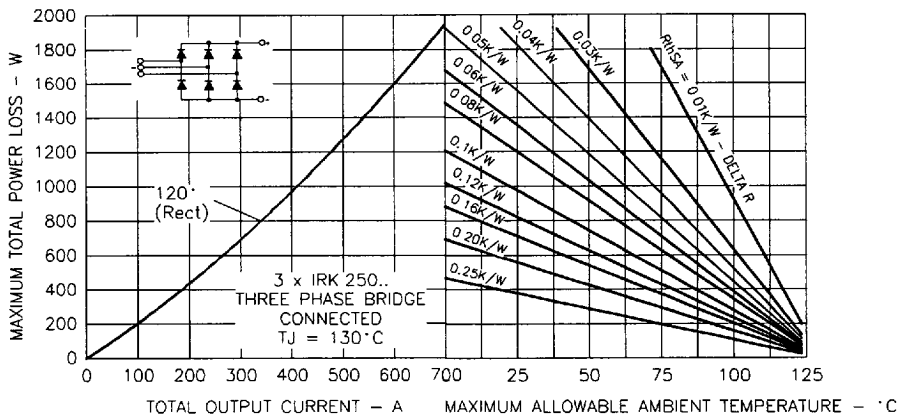


Fig.27 - On-state Power Loss Characteristics

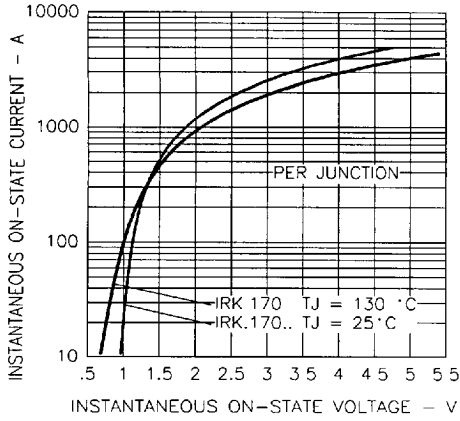


Fig. 28 - On-state Voltage Drop Characteristics

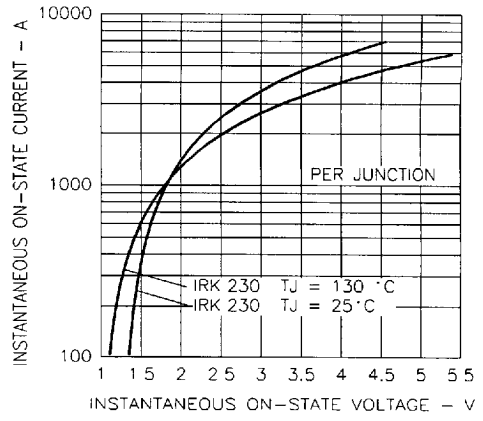


Fig. 29 - On-state Voltage Drop Characteristics

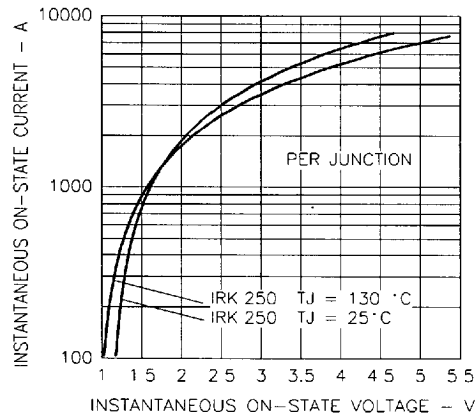


Fig. 30 - On-state Voltage Drop Characteristics

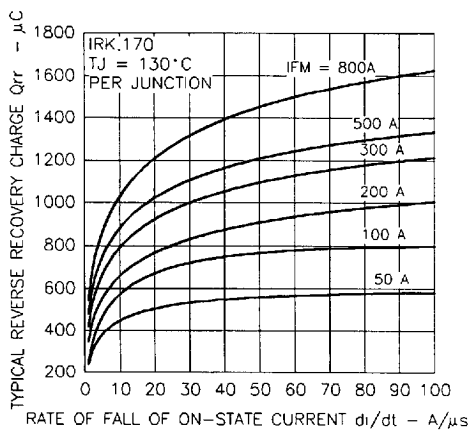


Fig. 31 - Reverse Recovery Charge Characteristics

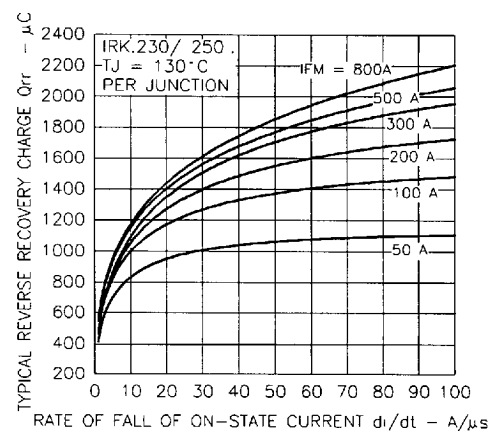


Fig. 30 - Reverse Recovery Charge Characteristics

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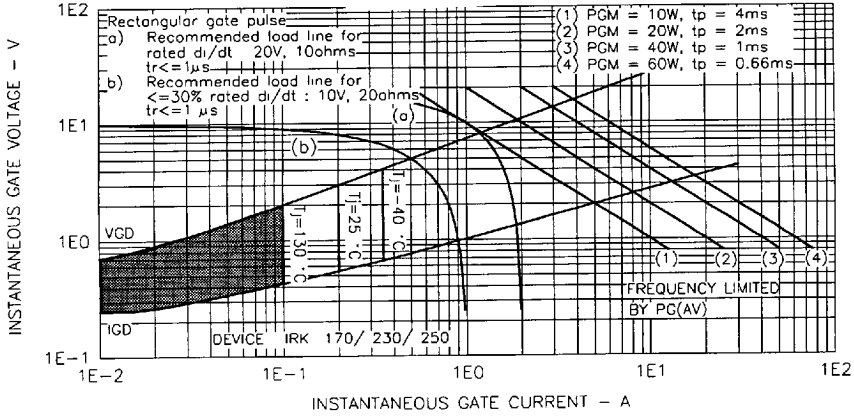


Fig. 33 - Gate Characteristics

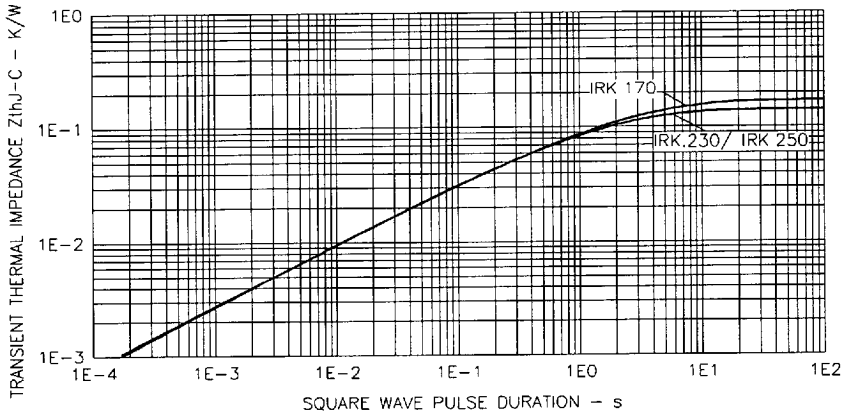


Fig. 34 - Thermal Impedance Z_{thJC} Characteristics