PLESSEY
Semiconductors

T-77-07-13

MV1720

MAC CONTROL CIRCUIT

The main functions of the MV1720 Controller for the Nordic VLSI C/D/D2/MAC/packet receiver are to decode the bit-stream from the demodulator, and to serve as an interface between the receiver microcomputer and the chip set.

The MV1720 synchronises on the frame structure by recognising line and frame sync, and generates timing signals which control the operation of other modules. Data is spectrum descrambled, and data in the selected bursts is de-interleaved and formed into full packets. Packet headers and optionally the data part are corrected and routed to a common output for sound and data.

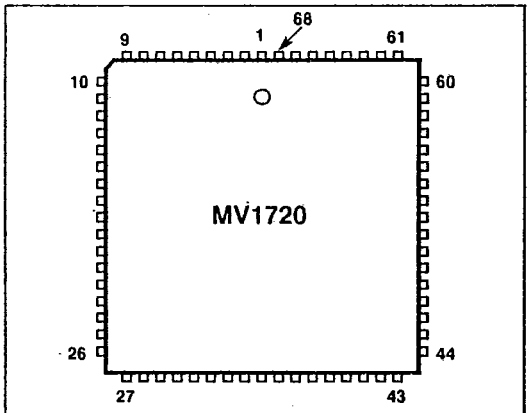
SI-packets (addr 0), SMM, CMM or AUX packets can also be routed to a separate packet buffer which can be read from the receiver microcomputer. CMM address recognition is supported. Golay encoded packets are decoded, corrected and optionally compressed before they are stored in the packet buffer.

The MV1720 has a general purpose microprocessor interface that is compatible with most microprocessors or microcomputers. The data rate is controlled by the microcomputer and can be up to 2 Mbyte/sec.

Line 625 is decoded and majority voted for repeated and static data fields. The resultant data is output as a special 'packet' with separate strobe signals. This packet can also be read via the packet buffer.

FEATURES

- Programmable Sync Acquisition and Generation
- De-interleaving of Two Independent Subframes
- Hardware Golay Decoding and Correction for CMM, SMM and SI-Packets (Programmable)
- Programmable Packet Address Selection
- Programmable SMM Packet Selection
- Programmable CMM Packets Selection with Unique Customer Address and Shared Address (according to the EBU Spec) (ref.1)
- Programmable CMM Packet Selection with Collective Address and Entire Audience (Proposed EBU Spec Extension)
- High-Speed Microprocessor Interface supporting most Microprocessors or Microcomputers



LC68

Pin	Function	Pin	Function
1	V_{SS}	35	CE
2	V_{DD}	36	V_{SS}
3	FS2	37	MCD4
4	FS1	38	MCD5
5	RESET	39	V_{DD}
6	DATAIN	40	MCD6
7	CLK1	41	MCD7
8	V_{SS}	42	NC
9	CDATAOUT	43	NC
10	NC	44	NC
11	TEST	45	TEST
12	CSTRB	46	RS
13	V_{DD}	47	MCLK
14	CLKPLL	48	IRQ
15	CLAMP	49	VAL
16	CDATAIN	50	PDATA
17	L	51	V_{SS}
18	F	52	SPINF
19	TEST 1	53	SFRQ
20	LSYNC	54	V_{DD}
21	V_{SS}	55	PACKST
22	CLKD 2	56	PACKDT
23	RD	57	V_{SS}
24	WR	58	SIV
25	TEST	59	TEST
26	NC	60	NC
27	NC	61	NC
28	TEST	62	SB2
29	V_{SS}	63	SB1
30	MCD0	64	TTV
31	MCD1	65	DISD
32	MCD2	66	DATAOUT
33	V_{DD}	67	ML625
34	MCD3	68	EFCNT

Fig.1 Pin connections - top view

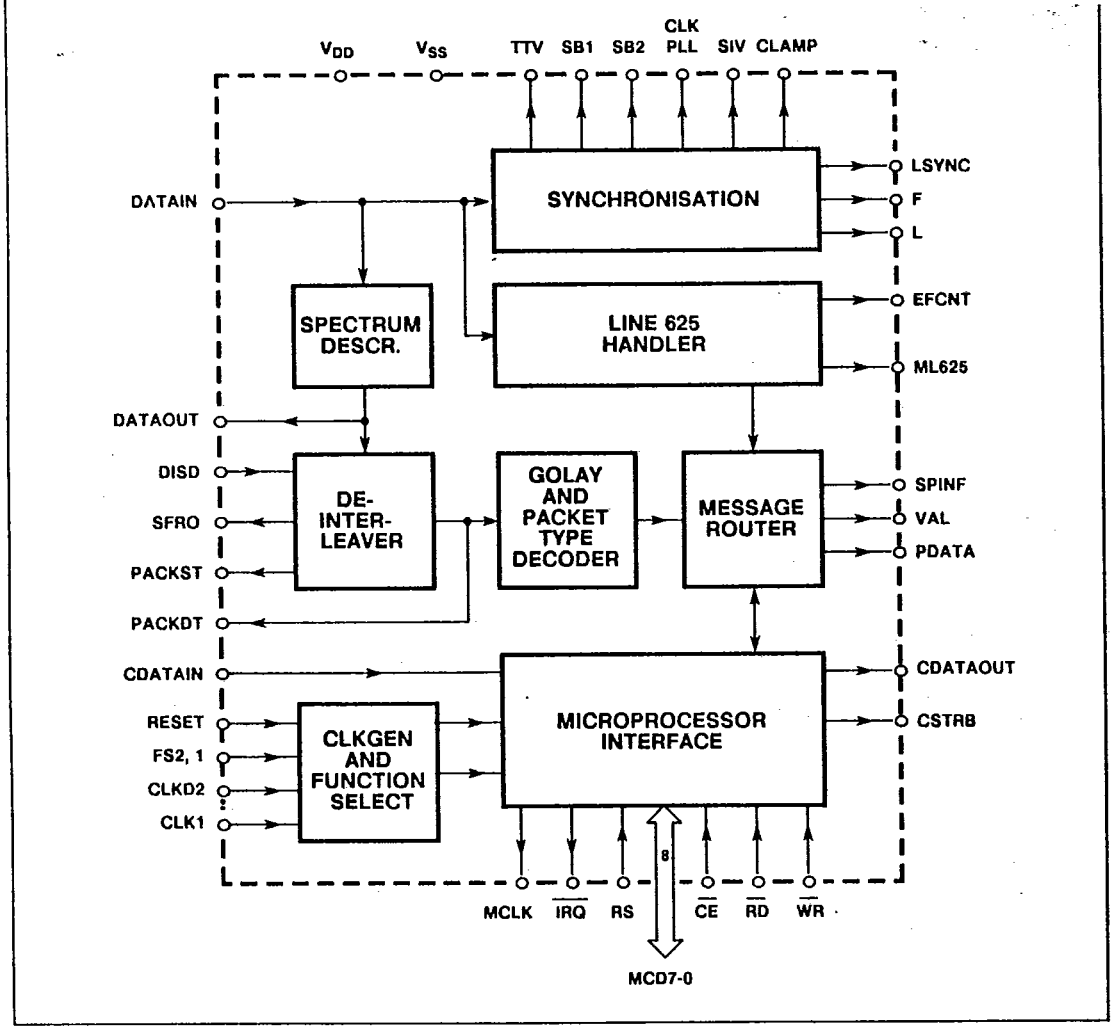


Fig.2 Simplified block diagram for MV1720 MAC/packet control chip

DESCRIPTION OF THE SIMPLIFIED BLOCK DIAGRAM

Synchronisation

This module monitors the input data from the receiver, looking for the line sync words (LSW) appearing in the beginning of each line. There are two such alternating words named W1 and W2. The module first looks for 3 consecutive alternating LSWs, and enters 'local sync' when this occurs. Afterwards it expects to find the boundary between an even- and odd-numbered frame within 1250 lines, i.e. two frame periods.

When searching for the LSW, it will accept 1 bit error before local sync is obtained, after which it switches to accepting 2 bit errors. After entering local sync it may loose 15 consecutive LSWs before sync is assumed to be lost.

When detecting the frame boundary the F and L output signals both change from low to high, and continue to toggle according to the specification. The position where these signals change can be programmed via the microcomputer interface.

This module also generates the signals SB1 and SB2 (flagging two selectable data bursts (subframes) on DATAOUT), SIV (service identification in line 625 on DATAOUT), CLAMP (clamp period for video), TTV (lines containing Teletext), and LSYNC (active after each LSW detected).

Spectrum Descrambler

The descrambler contains a 15-bit pseudo-random generator. It starts after LSW is detected in line 1 and runs continuously until line 625 when it is initialised (set to ones).

The DATAIN signal is XOR'ed with the output from the generator. The output from the descrambler is available on the DATAOUT pin of the MV1720.

De-Interleaver

This module consists of four 751 bit buffers and a sequencer handling input and output. Each buffer is a 751 x 1 bit static RAM. Incoming data arrives in bursts (99 x 2 bits/line for the standard sub frames); outgoing data is transmitted as complete packets.

Four buffers enable the MV1720 to de-interleave a continuous stream of data from two independent subframes. It is possible to de interleave data that only occurs in certain lines, i.e. field blanking by using the DISD input. Output from the de-interleaver is available as PACKDT (packet data), PACKST (packet strobe) and SFRO (subframe origin).

Golay and Packet Type Decoder

This module uses a Meggitt decoder for error correcting the Golay encoded packet header and optionally the data part for selected packets.

To achieve real time operation, a pipelined syndrome register is included. The correctable error patterns are permanently stored in an on-chip ROM.

The module removes the 11-bit checksum in the packet header and inserts a bit indicating which of the two selected sub-frames is the origin of the packet. The module corrects the Hamming (8,2) PT byte as well.

The resulting error corrected packets are immediately passed on to the Message router.

Messager Router T-77-07-13

The Message Router handles all incoming packets, and compares packet addresses and address fields in CMM packets. The microcomputer can select which packets should be transmitted to a buffer in the processor interface.

The selection is done by storing the different addresses in a table in the Message Router and comparing them to appropriate packet fields. This table is updated via the configuration chain. The table contains:

Packet 0 address (permanently stored)
CMM packet address (10 bits)
CMM packet Unique Customer address (36 bits)
CMM packet Shared address (24 bits)
CMM packet Collective address (12 bits)
SMM packet address (10 bits)
AUX packet address (10 bits)
Line 625 data packet (permanently stored)

The processor interface can control the priority between the different packets. All packets will be transmitted to the PDATA pin at 20.25 M bits. Data in line 625 is converted to a packet with the decimal address 1023 (inserted by the Line 625 Handler).

A strobe signal for the packet-headers is provided on a separate pin of the MV1720. This signal (VAL) is high during the first 13 bits (PA, CI, SFRI) of every packet.

The line 625 message is not strobed by the VAL signal. A strobe signal (SPINF) is enabled during output of this message. SPINF is also enabled during output of packets with packet address 0, CMM and SMM messages.

Line 625 Handler

This module handles parts of the special data burst in line 625 of each frame; i.e.

UDT - Unified Date Time
SDF - Static Data Frame
RDF - Repeated Data Frame

The first bit of UDT (sequence bit) is checked and any sequence error is flagged in the special line 625 packet. The next four bits of UDT are not processed in any way, just included in the line 625 packet.

In every fifth line 625 packet, a majority vote of the five last SDFs is included. In the other four packets, the SDF part is not valid. A flag (SDFV) indicates whether SDF is valid or not. The majority voted SDF's are also BCH error checked but not corrected. If the BCH check fails then SDFV is not set.

The five TDMCTLs in line 625 are also majority voted and BCH checked. The result (RDF) is included in the line 625 packet together with an error flag for the BCH check.

The module also contains a flywheel counter for FCNT. This counter is incremented every line 625. The most significant bit of FCNT is available externally as EFCNT. If a valid RDF is received, the received FCNT is loaded into the counter. Loading FCNT will not change EFCNT before next line 625.

Clock Generator and Function Select

CLK1 is used to generate all internal timing and must always be available. CLKD2 is only for D2/MAC reception.

RESET is used to reset MV1720 to a known state after power up.

FS1 and FS2 are function select inputs used during test and should always be tied to V_{SS}.

Processor Interface

The processor interface is for an external microcomputer. This microcomputer initialises and configures the complete MAC/packet chipset, and receives selected information from the packet multiplex together with status information.

This interface is designed to be compatible with a large number of different microprocessors or single chip microcomputers. The interface is shown in Fig.3.

ABSOLUTE MAXIMUM RATINGS (Referenced to V_{SS})

T-77-07-13

DC Supply voltage V_{DD}	-0.3V to +7V
Input voltage	-0.3V to V_{DD} +0.3V
Storage temperature range	-55°C to +125°C
Ambient operating temperature	0°C to +70°C

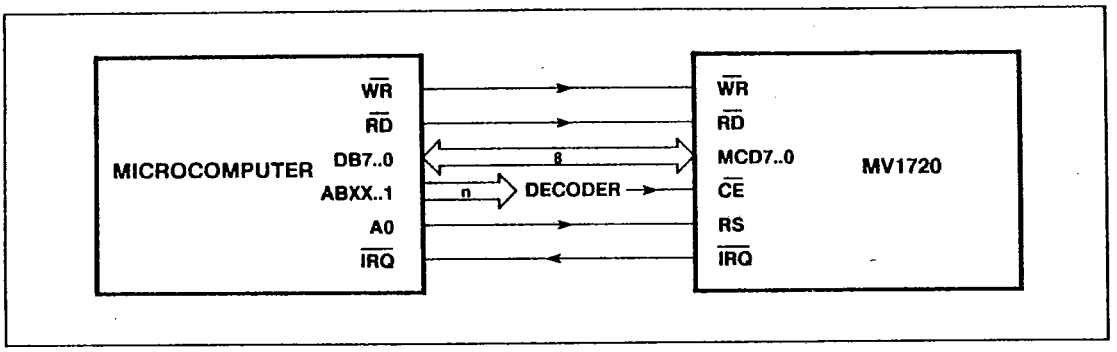


Fig.3 Interface between the MV1720 and a microcomputer

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 0°C to +70°C, V_{DD} = +4.75V to +5.25V

Characteristic	Value		Units	Conditions
	Min.	Max.		
Low input voltage	V_{SS}	1.2	V	
High input voltage	3.4	V_{DD}	V	
Low output voltage		0.4	V	I_{OL} = 10mA
High output voltage	V_{DD} -0.4		V	I_{OH} = -10mA
Clock 1 frequency	1	21	MHz	
Setup time (all inputs) See note 1		0	ns	

NOTE

1. This figure is valid for all data inputs relative to the positive edge of CLK1.

(ref.1) MAC packet family specifications EBU No. TECH 3258-E.