MX•COM, INC. MX939

Advance Information

LOW VOLTAGE DUAL MODE CDPD/AMPS-WBD FULL-DUPLEX DATA MODEM

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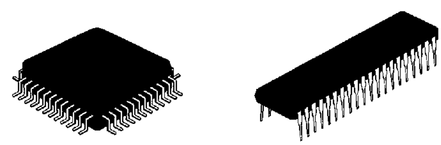
FEATURES

- MX•COM MiXed SIGNAL CMOS
- FULL-DUPLEX GMSK MODEM
- SAT TONE DETECTION & REGENERATION
- WIDE BAND DATA (WBD) MODEM
- LOW VOLTAGE OPERATION
  3 TO 5.5 V
- POWERSAVING MANAGEMENT MODES
- DIGITALLY CONTROLLED I/O SIGNAL LEVELS
- 180° TWO-POINT TX OUTPUT
- SERIAL PORT COMPATIBLE WITH DSP INTERFACE
- PARALLEL μP CONTROL INTERFACE
- COMPLIES WITH CDPD 1.0 STANDARD

APPLICATIONS

- CDPD FULL-DUPLEX DATA MODEM
- AMPS WIDE BAND FULL-DUPLEX DATA MODEM WITH SAT CONTROL
- TQFP PACKAGE FITS PCMCIA



MX939TG
48-pin TQFP

MX939P
40-pin PDIP

Description

The MX939 is a synchronous Modem IC designed for wireless data applications. Employing Gaussian Minimum Shift Keying (GMSK) baseband modulation, the MX939 provides a BT of 0.5 and data rates at 19.2 kbps for Cellular Digital Packet Data (CDPD) and 10 kbps for Wide Band Data (WBD).

The MX939 is programmable via an 8-bit parallel bus to support packet switched CDPD full-duplex GMSK operation. Optionally, the MX939 may be programmed for AMPS circuit switched WBD operation including SAT tone detection and regeneration. In this mode an interrupt occurs whenever the SAT tone is detected.

In its AMPS WBD capacity, the MX939 accepts NRZ data and converts it to Manchester encoded data for transmission. It also receives Manchester encoded data and outputs sliced data directly at 10kbps.

Input and output signal levels can be adjusted using the digitally controlled gain blocks. 180° out of phase outputs are possible using the additional inverting digitally controlled gain block, allowing two-point modulation.

The TX and RX data interfaces are bit serial, synchronized to TX and RX data clocks generated by the modem.

A programmable Powersave mode ensures minimum power consumption. The MX939 is available in DIP and TQFP (Thin Quad Flat Pack) packages.

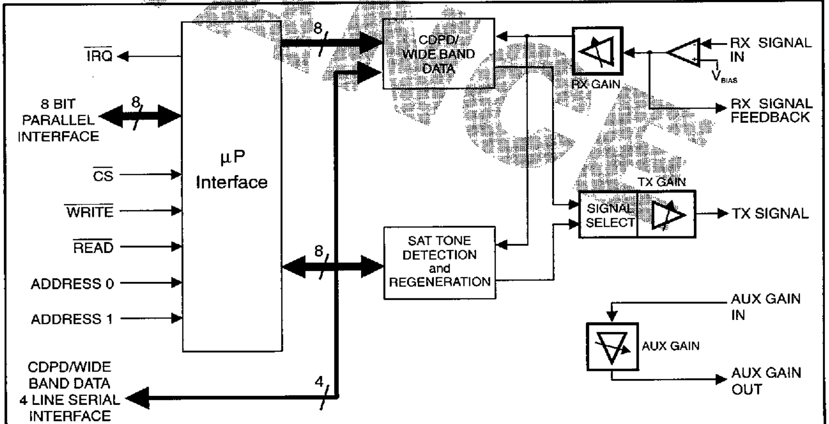


Figure 1 - Block Diagram

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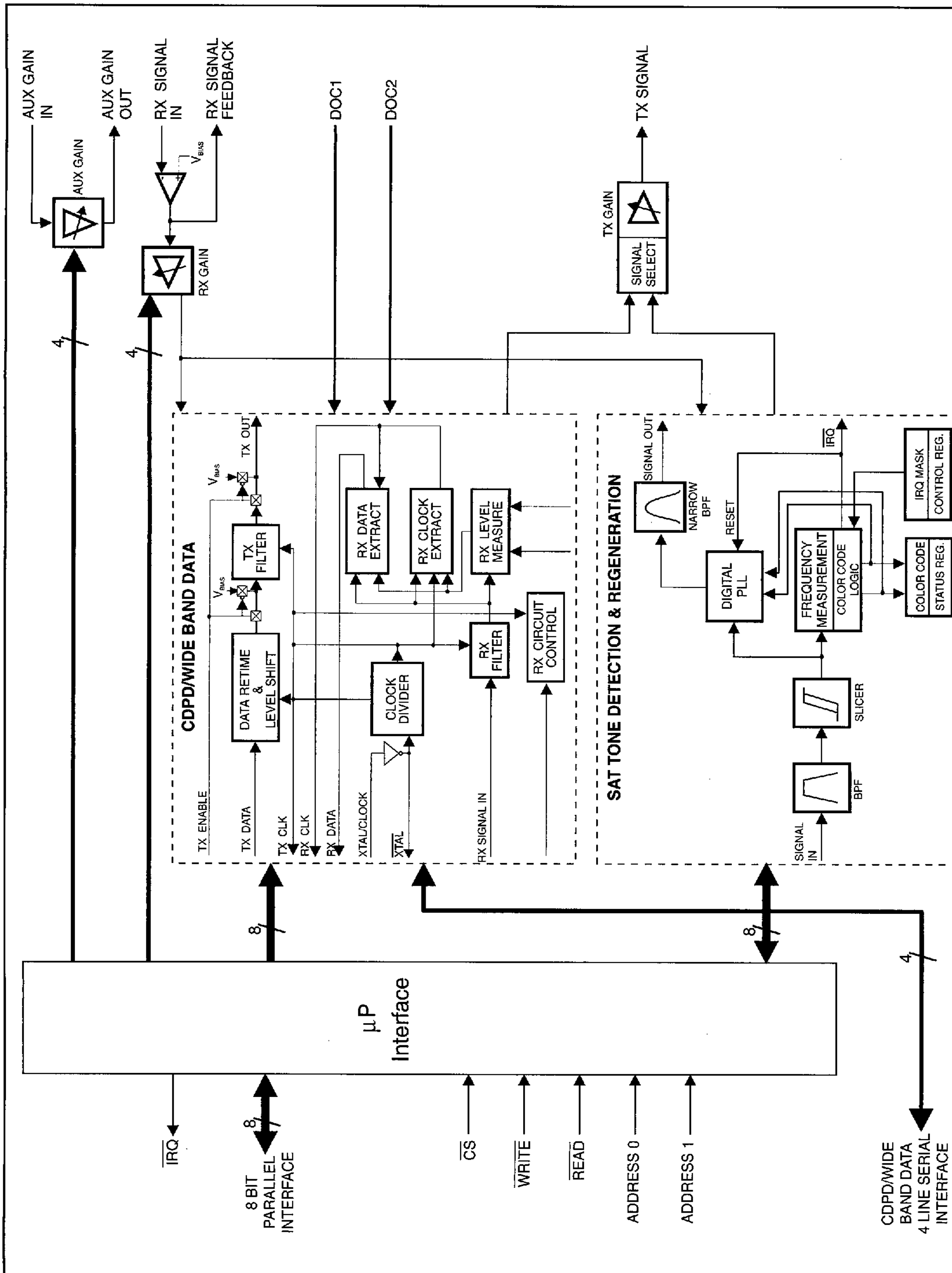

Figure 2 - Detailed Block Diagram

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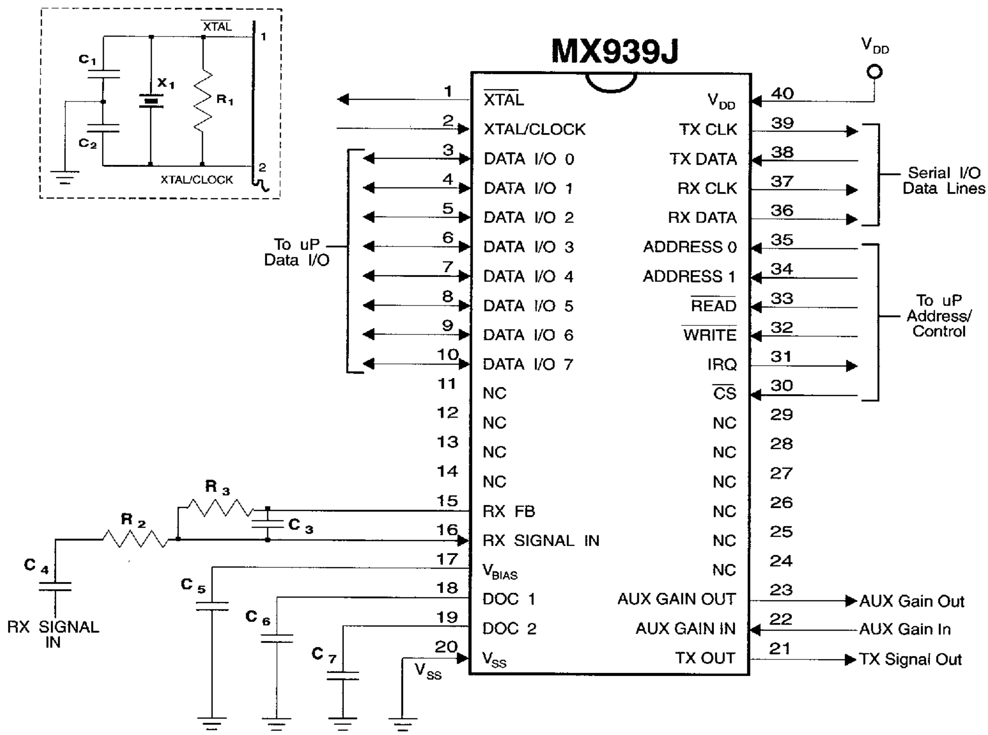
Pin	Function
1	**$\overline{\text{Xtal}}$:** The output of the on-chip clock oscillator.
2	**Xtal/Clock:** The input to the on-chip Xtal oscillator. A Xtal, or externally derived clock (f_{XTAL}) pulse input should be connected here. If an externally generated clock is to be used, it should be connected to this pin and the "$\overline{\text{Xtal}}$" pin left unconnected. Note that operation of the MX939 without a suitable Xtal or clock input may cause device damage.
3-10	**DATA I/O 0-7:** 8 bi-directional 3-state µP interface data lines.
15	**RX FB:** The output of the RX Input Amplifier and the input to the RX Filter.
16	**RX Signal In:** The input to RX input amplifier.
17	**V_{BIAS}:** The internal circuitry bias line, held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by a capacitor mounted close to the pin.
18 19	**Doc1:** **Doc2:** Connections to the RX Level Measurement Circuitry. A capacitor should be connected from each pin to V_{SS}.
20	**V_{SS}:** Negative supply rail. Signal ground.
21	**TX Out:** The TX signal output from the MX939 GMSK Modem.
22 23	**AUX Gain In:** **AUX Gain Out:** These pins form the input and output of the auxiliary inverting digitally controlled variable gain amplifier.
30	**$\overline{\text{CS}}$ (Chip Select):** This is an active low logic level input to the MX939 used to enable a data read or write operation.
31	**$\overline{\text{IRQ}}$:** This is a "wire-ORable" output for connection to the controlling µP's Interrupt Request input. It has a low impedance pull-down to V_{SS} when active, and has a high impedance when inactive.
32	**$\overline{\text{WRITE}}$:** This active low logic level input is used to control the writing of data to the MX939 from the controlling µP.
33	**$\overline{\text{READ}}$:** This active low logic level input is used to control the reading of data from the MX939 into the controlling µP.
34 35	**ADDRESS 1:** These are logic level register select inputs. **ADDRESS 0:**
36	**RX Data:** A logic level output carrying the received data, synchronous with RX CLK.
37	**RX CLK:** A logic level clock output at the received data bit-rate.
38	**TX Data:** The logic level input for the data to be transmitted. This data should be synchronous with TX CLK.
39	**TX CLK:** A logic level clock output at the transmit-data rate.

TX & RX Data, and TX & RX Clk form the serial I/O interface for the CDPD or wide band data modems with the bit rate frequencies listed below:

Modem Type	RX Data	RX Clk	TX Data	TX Clk
CDPD	9.6kHz max.	19.2kHz	9.6kHz max.	19.2kHz
AMPS WBD	10kHz max.	20kHz	5kHz max.	10kHz

Pin	Function
40	**V_{DD}:** Positive supply rail. A single +5 volt power supply is required. Levels and voltages within this modem are dependent upon this supply. This pin should be decoupled to V_{SS} by a capacitor mounted close to the pin.

Note: Pin-out for the 48-pin TQFP is T.B.D.



Component	Value
R_1	1.0MΩ
R_2	Note 1
R_3	100kΩ
C_1	T.B.D.
C_2	T.B.D.

Component	Value
C_3	33pF
C_4	Note 1
C_5	1.0µF
C_6	15pF
C_7	15pF
X_1	1.44MHz

Notes

1. R_2, R_3, C_3 and C_4 form the gain components for the RX Input signal. They should be chosen as required by the signal input level.

Figure 3 - External Components

Actual Pin-out T.B.D.

Application Information for CDPD/Wide Band Data

RX Signal Path Description

The function of the RX circuitry is to:

1. Set the incoming signal to a usable level.
2. Clean the signal by filtering.
3. Provide d.c. level thresholds for clock and data extraction.
4. Provide clock timing information for data extraction and external circuits.
5. Provide RX data in a binary form.

The output of the radio receiver's Frequency Discriminator should be fed to the MX939's RX Filter via a suitable gain and d.c. level adjusting circuit. This gain circuit can be built, with external components, around the on-chip RX Input Amplifier.

Positive going signal excursions at RX Feedback pin will produce a logic "0" at the RX Data Output. Negative going excursions will produce a logic "1."

The received signal is fed through the lowpass RX Filter, which has a -3dB corner frequency of 0.56 times the data bit-rate, before being applied to the Level Measure and Clock and Data extraction blocks.

The Level Measuring block consists of two voltage detectors, one of which measures the amplitude of the 'positive' parts of the received signal. The other measures the amplitude of the 'negative' portions. External capacitors are used by these detectors, via the Doc 1/2 pins, to form voltage 'hold' or 'integrator' circuits. Results of the two measurements are then processed to establish the optimum d.c. level decision-thresholds for the Clock and Data extraction, depending upon the RX signal amplitude and any d.c. offset present.

RX Circuit Control Modes

The operating characteristics of the RX Level Measurement and Clock Extraction circuits are controlled, as shown in Table 1, by logic level inputs applied to the 'PLLacq,' 'RX Hold' and 'RXDCacq.'

As shown in Figure 4, a data transmission generally begins with a preamble such as "1010101010," to allow the receiving modem to establish timing- and level-lock as quickly as possible. During the time that the preamble is expected, the 'RXDCacq' and 'PLLacq' inputs should be switched from a logic "0 to 1" so that the Level Measuring and Clock Extraction modes are operated and sequenced as shown.

The 'RX Hold' input should normally be held at a logic "1" while data is being received, but may be driven to a logic "0" to freeze the Level Measuring and Clock Extraction circuits during a fade. If the fade lasts for less than 200 bit periods, normal operation can be resumed by returning the 'RX Hold' input to a logic "1" at the end of the fade. For longer fades, it may be better to reset the Level Measuring circuits by placing the 'RXDCacq' to a logic "1" for 10 to 20 bit periods.

'RX Hold' has no effect on the Level Measuring circuits while 'RXDCacq' is at a logic "1," and has no effect on the PLL while 'PLLacq' is at a logic "1."

A logic "0" on 'RX Hold' does not disable the 'RX Clock' output, and the RX Data Extraction and S/N Detection circuits will continue to operate.

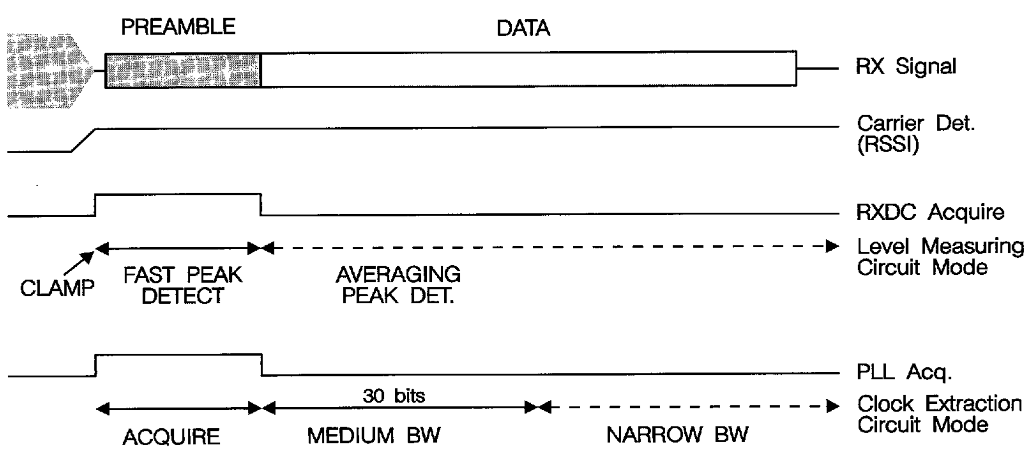


Figure 4 - RX Mode Control Diagram

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Application Information ......

PLLacq	RX Hold	PLL Action
"1"	X	**Acquire:** Sets the PLL bandwidth wide enough to allow a lock to the received signal in less than 8 zero crossings. The Acquire mode will operate as long as PLLacq is a logic "1".
"1" to "0"	"1"	**Medium Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±T.B.D. bit-periods for every two received zero-crossings. The PLL operates in this mode for a period of about 30 bits immediately following a "1" to "0" transition of the PLLacq input, provided that the RX Hold input is a logic "1".
"0"	"1"	**Narrow Bandwidth:** The correction applied to the extracted clock is limited to a maximum of ±T.B.D. bit-periods for every two received zero-crossings. The PLL operates in this mode whenever the RX Hold Input is a logic "1" and PLLacq has been a logic "0" for at least 30 bit periods (after Medium Bandwidth operation, for instance).
"0"	"0"	**Hold:** The PLL feedback loop is broken, allowing the RX Clock to freewheel during signal fade periods.
RXDCacq	**RX Hold**	**RX Level Measure Action**
"0" to "1"	X	**ClGain:** Operates for one bit-time after a "0" to "1" transition of the RXDCacq input. The external capacitors are rapidly charged toward a voltage halfway between the received signal input level and V_{BIAS}, with the charge time-constant being approximately 0.5bit-time.
"1"	X	**Fast Peak Detect:** The voltage detectors act as peak-detectors. One capacitor is used to capture the 'positive'-going signal peaks of the RX Filter output signal; the other captures the 'negative'-going peaks. The detectors operate in this mode whenever the RXDCacq input is at a logic "1," except for the initial 1-bit ClGain-mode time.
"0"	"1"	**Averaging Peak Detect:** Provides a slower but more accurate measurement of the signal peak amplitudes.
"0"	"0"	**Hold:** The capacitor charging circuits are disabled so that the outputs of the voltage detectors remain substantially at the last readings (discharging very slowly [time-constant approx. 2,000 bits] towards V_{BIAS}).

Table 1 - PLL and RX Level Measurement Operational Modes

RX Clock Extraction

Synchronized by a phased locked loop (PLL) circuit to zero-crossings of the incoming data, the 'RX Clock Extraction' circuitry controls the 'RX CLK' output. The RX Clock is also used internally by the Data Extraction circuitry. The PLL parameters can be varied by the 'RX Circuit Control' inputs PLLacq and RX Hold to operate in one of four PLL modes as described in Table 1.

RX Data Extraction

The 'RX Data Extraction' circuit decides whether each received bit is a "1" or "0" by sampling the output of the RX Filter in the middle of each bit-period, and comparing the sampled voltage against a threshold derived from the 'Level Measuring' circuit. This threshold is varied on a bit-by-bit basis to compensate for intersymbol interference. The extracted data is output from the 'RX Data' pin, and should be sampled externally on the rising edge of the 'RX CLK.'

TX Signal Path Description

The binary data applied to the 'TX Data' input is retimed within the chip on each rising edge of the 'TX Clock' and then converted to a binary signal centered about V_{BIAS}.

The TX Filter has a lowpass frequency response, which is designed to minimize amplitude and phase distortion of the binary signal while providing sufficient attenuation of the high frequency-components which would otherwise cause interference into adjacent radio channels.

The signal at 'TX Out' is centered around V_{BIAS}, going positive for logic "1" (high) level inputs to the 'TX Data' input and negative for logic "0" (low) inputs.

Application Information ......

FM Modulator, Demodulator and IF

For optimum performance, the 'eye' pattern of the received signal (when receiving random data) applied to the MX939 should be as close as possible to the Transmit 'eye' pattern example shown in Figure 5. Of particular importance are general symmetry and cleanliness of the zero-crossings.

To achieve this, attention must be paid to:

- Linearity and frequency/phase response of the TX frequency modulator. Unless the transmit data is encoded to remove low frequency components, the modulator frequency response should extend down to a few Hz. This is because two-point modulation is necessary for synthesized radios.
- Bandwidth and phase response of the RX IF filters.
- Accuracy of the TX and RX carrier frequencies -any difference will shift the received signal towards one of the skirts of the IF filter response.

Ideally, the RX demodulator should be d.c. coupled to the MX939 'RX Signal In' pin (with a d.c. bias added to center the signal at the RX Feedback pin around $V_{DD}/2$ [V_{BIAS}]), however a.c. coupling can be used provided that:

- The 3 dB cut-off frequency is 20Hz or below (i.e. a 0.1µF capacitor in series with 100kΩ).
- The data does not contain long sequences of consecutive ones or zeroes.
- Sufficient time is allowed after a step change at the discriminator output (resulting from channel changing or the appearance of an RF carrier) for the voltage into the MX939 to settle before the 'RXDCacq' line is strobed.

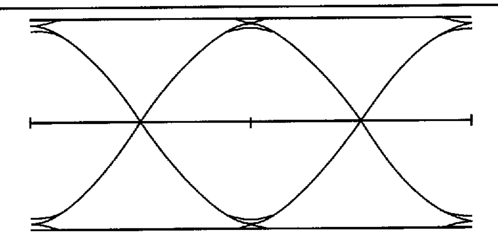

Figure 5 - Typical Transmit Eye Pattern

Data Formats

The receive section of the MX939 works best with data which has a reasonably 'random' structure --the data should contain approximately the same number of 'ones' as 'zeroes' with no long sequences of consecutive 'ones' or 'zeroes'. Also, long sequences (>100 bits) of '10101010 ...' patterns should be avoided.

For this reason, it is recommended that data is randomized in some manner before transmission, for example by 'exclusive-ORing' it with the output of a binary pseudo-random pattern generator.

Where data is transmitted in bursts, each burst should be preceded by a preamble designed to allow the receive modem to establish timing and level lock as quickly as possible. This preamble should be at least 16 bits long, and should preferably consist of alternating pairs of '1's and '0's i.e. '110011001100 .....'; the pattern '10101010 ....' should not be used.

'Acquisition' and 'Hold' Modes

The 'RXDCacq' and 'PLLacq' inputs must be pulsed 'High' for about 16 bits at the start of reception to ensure that the d.c. measurement and timing extraction circuits lock-on to the received signal correctly. Once lock has been achieved, then the above inputs should be taken 'Low' again.

In most applications, there will be a d.c. step in the output voltage from the receiver FM discriminator due to carrier frequency offsets as channels are changed or when the distant transmitter is turned on.

The MX939 can tolerate d.c. offsets in the received signal of at much as ±0.5V with respect to V_{BIAS}, (measured at the RX Feedback pin). However, to ensure that the d.c. offset compensation circuit operates correctly and with minimum delay, the 'Low' to 'High' transition of the 'RXDCacq' and 'PLLacq' inputs should occur after the mean input voltage to the MX939 has settled to within about 0.1V of its final value. (Note that this can place restrictions on the value of any series signal coupling capacitor.)

As well as using the 'RX Hold' input to freeze the Level Measuring and Clock Extraction circuits during a signal 'fade,' RX Hold may also be used in systems which employ a continuously transmitting control channel to freeze the receive circuitry during transmission of a data packet, allowing reception to resume afterwards without losing bit synchronization. To achieve this, the MX939 'Xtal' clock needs to be accurate enough that the derived 'RXClock' output does not drift by more that about 0.1 bit time from the actual received data-rate during the time that the 'RXHold' input is 'Low'.

The 'RXDCacq' input, however, may need to be pulsed 'High' to re-establish the level measurements if the 'RXHold' input is 'Low' for more that a few hundred bit-times.

The voltages on the Doc1 and Doc2 pins reflect the average peak positive and negative excursions of the (filtered) receive signal, and could therefore be used to derive a measure of the data signal amplitude. Note however, that these pins are driven from very high-impedance circuits, so that the d.c. load presented by any external circuitry should exceed 10MΩ to V_{BIAS}.

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Read and Write Registers - Memory Map

	HEX	READ	WRITE	CS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read Only Status Register	$0	0	1	0	0	0	0	0	0	0	COLOR CODE	
Write Only GAIN 1 Register	$0	1	0	0	— — — AUX GAIN — — —				— — — — TX GAIN — — — —			
GAIN 2 Register	$1	1	0	0	x	x	x	x	— — — — RX GAIN — — — —			
Control Register	$2	1	0	0	x	x	IRQ Mask	Hold	PLLacq	DCacq	MODE	

x = don't care

Read Only Register

STATUS Register (HEX address $0)

This read only register contains the status of the color code as described below:

COLOR CODE (Bits 0 and 1)

Bits 0 and 1 indicate the SAT tone frequency or "COLOR CODE" of the incoming signal according to the table below. Whenever the COLOR CODE changes an interrupt may occur, depending on the state of the IRQ mask (Bit 5) in the control register.

Measured Frequency of Incoming Signal	Measured SAT Determination	Where	COLOR CODE Bit 1	Bit 0
$f \leq f_1$	No valid SAT	f_1 = 5955 ± 5Hz	1	1
$f_1 \leq f < f_2$	SAT = 5970	f_2 = 5985 ± 5Hz	0	0
$f_2 \leq f < f_3$	SAT = 6000	f_3 = 6015 ± 5Hz	0	1
$f_3 \leq f < f_4$	SAT = 6030	f_4 = 6045 ± 5Hz	1	0
$f_4 \leq f$	No valid SAT		1	1
No SAT Received	No valid SAT		1	1

Table 2 - Color Code Frequencies

Write Only Register

GAIN 1 Register (HEX address $0)

This write only register controls the MX939's gain functions as described below:

AUX GAIN (Bits 7, 6, 5 and 4)

This 4-bit number specifies the gain of the auxiliary amplifier. The desired gain is selected according to Table 3. In the OFF state the amplifier is in a powersave mode, and the output is taken to bias via a 500kΩ resistor.

TX GAIN (Bits 3, 2, 1 and 0)

This 4-bit number specifies the TX gain. The desired gain is selected according to Table 4. In the OFF state the amplifier is in a powersave mode, and the output is taken to bias via a 500kΩ resistor.

Bit 7	Bit 6	Bit 5	Bit 4	Gain dB
0	0	0	0	OFF
0	0	0	1	-3.0
0	0	1	0	-2.571
0	0	1	1	-2.143
0	1	0	0	-1.714
0	1	0	1	-1.286
0	1	1	0	-0.857
0	1	1	1	-0.428
1	0	0	0	0
1	0	0	1	0.428
1	0	1	0	0.857
1	0	1	1	1.286
1	1	0	0	1.714
1	1	0	1	2.143
1	1	1	0	2.573
1	1	1	1	3.0

Table 3 - AUX Gain Register

Bit 3	Bit 2	Bit 1	Bit 0	Gain dB
0	0	0	0	OFF
0	0	0	1	-3.0
0	0	1	0	-2.571
0	0	1	1	-2.143
0	1	0	0	-1.714
0	1	0	1	-1.286
0	1	1	0	-0.857
0	1	1	1	-0.428
1	0	0	0	0
1	0	0	1	0.428
1	0	1	0	0.857
1	0	1	1	1.286
1	1	0	0	1.714
1	1	0	1	2.143
1	1	1	0	2.573
1	1	1	1	3.0

Table 4 - TX Gain Register

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GAIN 2 Register (HEX address $1)

This write only register controls the MX939's gain functions as described below:

RX GAIN (Bits 3, 2, 1 and 0)

This 4-bit number specifies the RX gain. The desired gain is selected according to Table 5 below.

Bit 3	Bit 2	Bit 1	Bit 0	Gain dB
0	0	0	0	OFF
0	0	0	1	-3.0
0	0	1	0	-2.571
0	0	1	1	-2.143
0	1	0	0	-1.714
0	1	0	1	-1.286
0	1	1	0	-0.857
0	1	1	1	-0.428
1	0	0	0	0
1	0	0	1	0.428
1	0	1	0	0.857
1	0	1	1	1.286
1	1	0	0	1.714
1	1	0	1	2.143
1	1	1	0	2.573
1	1	1	1	3.0

Table 5 - RX Gain Register

CONTROL Register (HEX address $2)

This register controls the MX939's functions as described below:

MODE (Bits 1 and 0)

This 2-bit number configures the MX939 to function as a CDPD, SAT Tone or Wide Band Data Modem described in Table 6 below.

Bit 1	Bit 0	CDPD	SAT Tone	Wide Band Data
0	0	Powersaved	Powersaved	Powersaved
0	1	Enabled	Powersaved	Powersaved
1	0	Powersaved	Enabled	Powersaved
1	1	Powersaved	Powersaved	Enabled

Table 6 - Mode Control Register

RXDCAcq (Bit 2)

A logic "1" applied to this bit will set the RX Level Measurement circuitry to the acquire mode. This applies to both the CDPD and the Wide Band Data Modem functions.

PLLAcq (Bit 3)

A logic "1" applied to this bit will set the RX Clock Extraction circuitry to the acquire mode. This applies to both the CDPD and the Wide Band Data Modem functions.

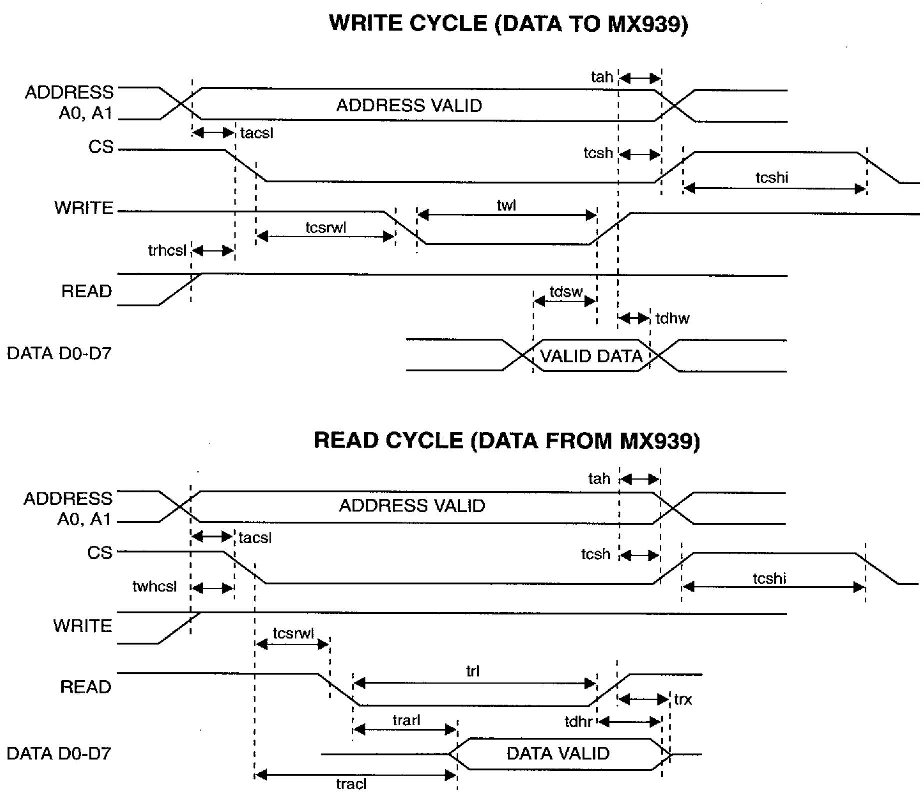
Hold (Bit 4)

A logic "0" applied to this bit will "freeze" the Clock Extraction and Level Measurement circuits unless they are in the acquire mode. This applies to both the CDPD and the Wide Band Data Modem functions.

IRQ Mask (Bit 5)

When this bit is set to "1" the COLOR CODE interrupt will be gated out to the IRQ pin. When this bit is set to "0" the COLOR CODE interrupt will be inhibited.

Timing Information



Period		Note	Min.	Typ.	Max.	Units
tacsl:	Address valid to CS low time		0	-	-	ns
tah:	Address hold time		0	-	-	ns
tcsh:	CS hold time		0	-	-	ns
tcshi:	CS high time		6	-	-	xtal cycles
tcsrwl:	CS to WRITE or READ low time		0	-	-	ns
tdhr:	Read data hold time		0	-	-	ms
tdhw:	Write data hold time		0	-	-	ns
tdsw:	Write data setup time		90	-	-	ns
trhcsl:	READ high to CS low time (write)		0	-	-	ns
tracl:	Read access time from CS low	1	-	-	175	ns
trarl:	Read access time from READ low	1	-	-	145	ns
trl:	READ low time		200	-	-	ns
trx:	READ high to D0-D7 3-state time		-	-	50	ns
twhcsl:	WRITE high to CS low time (read)		0	-	-	ns
twl:	WRITE low time		200	-	-	ns

Note 1: With 30pF max. to V_{SS} on D0-D7 pins.

Figure 6 - Parallel µP Interface Timing

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0V
Input Voltage at any pin (ref V_{SS}=0V)	-0.3 to (V_{DD}+ 0.3V)
Sink/Source Current	
(supply pins)	±30mA
(other pins)	±20mA
Total Device Dissipation (@ T_{AMB}=25°C)	800mW max.
Derating	10 mW/°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

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Operating Characteristics

All devices were measured under the following conditions unless otherwise noted.

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 1.44 MHz

Noise bandwidth = bit rate

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})		3.0	-	5.5	V
Static Values					
Supply Current					
Powersaved	1	-	1.0	TBD	mA
Enabled	1	-	8	TBD	mA
Transmit Parameters					
TX Output Impedance					
Enabled	2	-	1.0	TBD	kΩ
Powersaved	2	TBD	500	TBD	kΩ
TX Signal Level					
CDPD	3,5	TBD	1.0	TBD	V p-p
AMPS WBD	3,5	TBD	1.7	TBD	V p-p
SAT	3,5	TBD	0.4	TBD	V p-p
Receive Parameters					
RX Input Impedance		TBD	-	-	MΩ
RX In Amp Voltage Gain		-	500	-	V/V
RX Input Signal Level					
CDPD	4,5	TBD	1.0	TBD	V p-p
AMPS WBD	4,5	TBD	1.7	TBD	V p-p
SAT	4,5	TBD	0.4	TBD	V p-p
Xtal/Clock Input					
High Pulse Width	6	TBD	-	-	ns
Low Pulse Width	6	TBD	-	-	ns
Input Impedance		TBD	-	-	MΩ
Voltage Gain (i/p = 1mVrms @ 1kHz)		TBD	-	-	dB

Characteristics	See Note	Min.	Typ.	Max.	Unit
µP Interface					
Input Logic "1" Level	17,18	V_{DD}-1.15	-	-	V
Input Logic "0" Level	17,18	-	-	1.5	V
Input Leakage Current	17,18	TBD	-	TBD	µA
Input Capacitance	17,18	-	10.0	-	pF
Logic "1"Output Level at IOH = 120µA	18	V_{DD}-0.4	-	-	V
Logic "0"Output Level at IOL = 360µA	18,19	-	-	0.4	V
"Off" State Leakage Current (V = V_{DD})	19	-	-	TBD	µA
AUX Gain					
Input Impedance		TBD	-	-	kΩ
Output Impedance Enabled		-	1	-	kΩ
Powersave		-	500	-	kΩ
Bandwidth (-3dB)		TBD	-	-	kΩ
Total Harmonic Distortion	7	-	0.35	TBD	%
Output Noise Level	8	-	180	TBD	mVrms
Onset of Clipping	9	TBD	-	-	V p-p
RX Gain, TX Gain, AUX Gain					
Gain	10	TBD	-	TBD	dB
Gain per Step	10	-	0.43	-	dB
Step Error	10	-	-	TBD	dB
SAT Characteristics					
SAT RX Decode Response	16	-	200	TBD	ms
SAT RX Not Decode Level			TBD		
SAT TX Phase Step Response	11	-	-	TBD	ms
SAT TX Phase Jitter		TBD	-	TBD	degrees
SAT TX S/N		-	-	TBD	%
CDPD Characteristics					
CDPD RX Bit Rate		-	19.2	-	kbps
CDPD RX Data Delay	13	-	-	TBD	bit periods
CDPD RX BER			TBD		
CDPD TX Bit Rate		-	19.2	-	kbps
CDPD TX BT		-	0.5	-	
CDPD TX Data Delay	12	-	1.5	TBD	bit periods
AMPS WIDE BAND DATA (WBD) Characteristics					
WBD RX Bit Rate	15	-	20	-	kbps
WBD RX Data Delay	13	-	-	TBD	bit periods
WBD RX BER			TBD		
WBD TX Bit Rate	14	-	10	-	kbps
WBD TX Data Delay	12	-	1.5	TBD	bit periods

Notes

1. Not including current drawn from the MX939 pins by external circuitry.
2. Small signal impedance.
3. Measured with a 5V supply and the TX gain amplifier set to 0dB.
4. Measured with a 5V supply, the RX gain amplifier set to 0dB, and 0dB gain in the input amplifier.
5. Typical levels equate to carrier deviations of ±8kHz for WBD, ±4.8kHz for CDPD, and ±2kHz for SAT. The levels are directly proportional to the supply voltage.
6. Timing for an external clock input to the Xtal/clock pin.
7. Gain set to 0dB, input level of 549mVrms at 1kHz.
8. With an A.C. short-circuit input, measured in a 30kHz bandwidth.
9. With a 5 volt supply.
10. With reference to a 1kHz signal.
11. Time to settle to within 10° of final steady state phase.
12. Measured between the rising edge of 'TX Clock' and the center of the corresponding bit at 'TX Out.'
13. Measured between the center of bit at 'RX Signal In' and corresponding rising edge of the 'RX Clock'.
14. Input as NRZ data and converted on chip to Manchester encoded data.
15. Output as Manchester encoded data at a frequency of twice the NRZ data rate.
16. S/N T.B.D.
17. $\overline{WRITE}$, $\overline{READ}$, $\overline{CS}$, A0 and A1 pins.
18. D0-D7 pins.
19. $\overline{IRQ}$ pin.