

# CMOS single-chip 8-bit microcontroller with on-chip EEPROM

80C851/83C851

T-49-19-08

## DESCRIPTION

The Philips 80C851/83C851 is a high-performance microcontroller fabricated with Philips high-density CMOS technology. The 80C851/83C851 has the same instruction set as the 80C51. The Philips CMOS technology combines the high speed and density characteristics of HMOS with the low power attributes of CMOS. The Philips epitaxial substrate minimizes latch-up sensitivity.

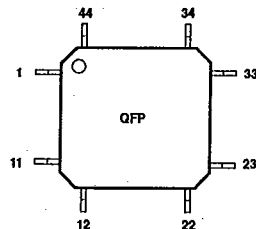
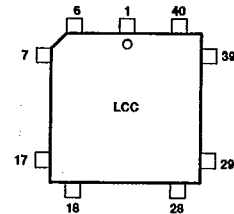
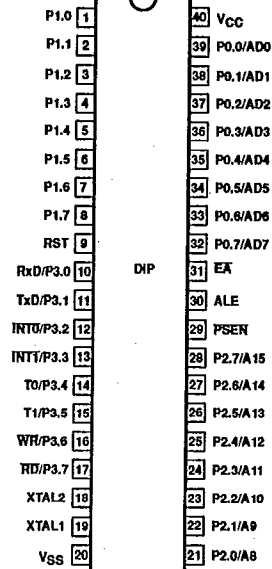
The 80C851/83C851 contains a  $4k \times 8$  ROM with mask-programmable ROM code protection, a  $128 \times 8$  RAM,  $256 \times 8$  EEPROM, 32 I/O lines, two 16-bit counter/timers, a seven-source, five vector, two-priority level nested interrupt structure, a serial I/O port for either multi-processor communications, I/O expansion or full duplex UART, and on-chip oscillator and clock circuits.

In addition, the 80C851/83C851 has two software selectable modes of power reduction — idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM and EEPROM contents but freezes the oscillator, causing all other chip functions to be inoperative.

## FEATURES

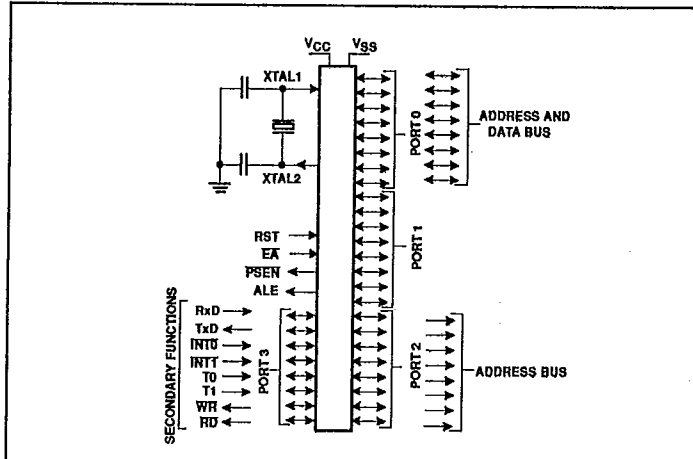
- 80C51 based architecture
  - $4k \times 8$  ROM
  - $128 \times 8$  RAM
  - Two 16-bit counter/timers
  - Full duplex serial channel
  - Boolean processor
- Non-volatile  $256 \times 8$ -bit EEPROM (electrically erasable programmable read only memory)
  - On-chip voltage multiplier for erase/write
  - 50,000 erase/write cycles per byte
  - 10 years non-volatile data retention
  - Infinite number of read cycles
  - User selectable security mode
  - Block erase capability
- Mask-programmable ROM code protection
- Memory addressing capability
  - 64k ROM and 64k RAM
- Power control modes:
  - Idle mode
  - Power-down mode
- CMOS and TTL compatible
- 1.2 to 16MHz
- Three package styles
- Three temperature ranges

## PIN CONFIGURATIONS



SEE PAGE 612 FOR QFP AND LCC PIN FUNCTIONS.

## LOGIC SYMBOL



# CMOS single-chip 8-bit microcontroller with on-chip EEPROM

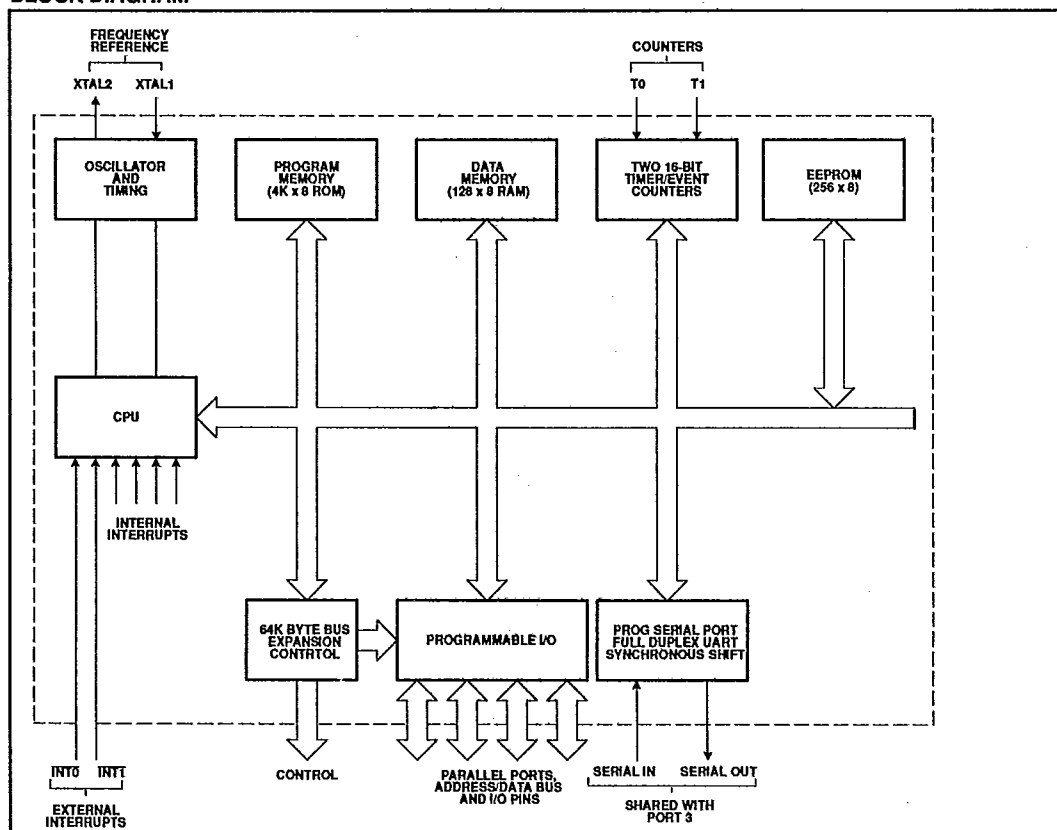
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## PART NUMBER SELECTION

PHILIPS PART ORDER NUMBER PART MARKING		SIGNETICS PART ORDER NUMBER		TEMPERATURE AND PACKAGE	FREQUENCY (MHz)
ROMless Version	ROM Version	ROMless Version	ROM Version		
PCB80C851-2-16P	PCB83C851-2P	S80C851-4N40	S83C851-4N40	0 to +70°C, plastic DIP	1.2 to 16
PCB80C851-2-16WP	PCB83C851-2WP	S80C851-4A44	S83C851-4A44	0 to +70°C, plastic PLCC	1.2 to 16
PCB80C851-2-16H	PCB83C851-2H	S80C851-4B44	S83C851-4B44	0 to +70°C, plastic QFP	1.2 to 16
PCF80C851-2-16P	PCF83C851-2P	S80C851-5N40	S83C851-5N40	-40 to +85°C, plastic DIP	1.2 to 16
PCF80C851-2-16WP	PCF83C851-2WP	S80C851-5A44	S83C851-5A44	-40 to +85°C, plastic PLCC	1.2 to 16
PCF80C851-2-16H	PCF83C851-2H	S80C851-5B44	S83C851-5B44	-40 to +85°C, plastic QFP	1.2 to 16
PCA80C851-2-16P	PCA83C851-2P	S80C851-6N40	S83C851-6N40	-40 to +125°C, plastic DIP	1.2 to 16
PCA80C851-2-16WP	PCA83C851-2WP	S80C851-6A44	S83C851-6A44	-40 to +125°C, plastic PLCC	1.2 to 16
PCA80C851-2-16H	PCA83C851-2H	S80C851-6B44	S83C851-6B44	-40 to +125°C, plastic QFP	1.2 to 16

## BLOCK DIAGRAM

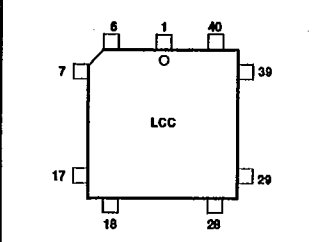


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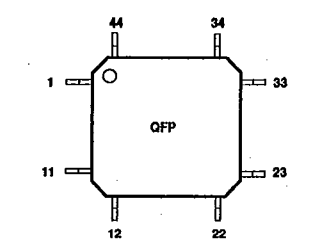
T-49-19-08

## LCC PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6	30	P2.6/A14
9	P1.7	31	P2.7/A15
10	RST	32	PSEN
11	P3.0/RxD	33	ALE
12	NC	34	NC
13	P3.1/TxD	35	E $\bar{A}$
14	P3.2/INT0	36	P0.7/AD7
15	P3.3/INTT	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/WR	40	P0.3/AD3
19	P3.7/RD	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	VSS	44	VCC

## QFP PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6	24	P2.6/A14
3	P1.7	25	P2.7/A15
4	RST	26	PSEN
5	P3.0/RxD	27	ALE
6	NC	28	NC
7	P3.1/TxD	29	E $\bar{A}$
8	P3.2/INT0	30	P0.7/AD7
9	P3.3/INTT	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/WR	34	P0.3/AD3
13	P3.7/RD	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	VSS	38	VCC
17	NC	39	VSS
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

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## PIN DESCRIPTION

MNEMONIC	PIN NO.			TYPE	NAME AND FUNCTION
	DIP	LCC	QFP		
V <sub>SS</sub>	20	22	16, 39	I	<b>Ground:</b> 0V reference.
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ).
P2.0–P2.7	21–28	24–31	18–25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I <sub>IL</sub> ). Port 3 also serves the special features of the 80C851 family, as listed below:
				I	<b>RxD (P3.0):</b> Serial input port
				O	<b>TxD (P3.1):</b> Serial output port
				I	<b>INT0 (P3.2):</b> External interrupt
				I	<b>INT1 (P3.3):</b> External interrupt
				I	<b>T0 (P3.4):</b> Timer 0 external input
				I	<b>T1 (P3.5):</b> Timer 1 external input
				O	<b>WR (P3.6):</b> External data memory write strobe
				O	<b>RD (P3.7):</b> External data memory read strobe
RST	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V <sub>SS</sub> permits a power-on reset using only an external capacitor to V <sub>CC</sub> .
ALE	30	33	27	I/O	<b>Address Latch Enable:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory.
PSEN	29	32	26	O	<b>Program Store Enable:</b> The read strobe to external program memory. When the device is executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
EA	31	35	29	I	<b>External Access Enable:</b> EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 0FFFH. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 0FFFH.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier.

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## EEPROM

Communications between the CPU and the EEPROM is accomplished via 5 special function registers; 2 address registers (high and low byte), 1 data register for read and write operations, 1 control register, and 1 timer register to adapt the erase/write time to the clock frequency. All registers can be read and written. Figure 1 shows a block diagram of the CPU, the EEPROM and the interface.

## Register and Functional Description

### Address Register (EADRH, EADRL)

The lower byte contains the address of one of the 256 bytes. The higher byte (EADRH) is for future extensions and for addressing the security bits (see Security Facilities). The

EADRH register address is F3H. The EADRL register address is F2H.

### Data Register (EDAT)

This register is required for read and write operations and also for row/block erase. In write mode, its contents are written to the addressed byte (for "row erase" and "block erase" the contents are don't care). The write pulse starts all operations, except read. In read mode, EDAT contains the data of the addressed byte. The EDAT register address is F4H.

### Timer Register (ETIM)

The timer register is required to adapt the erase/write time to the oscillator frequency. The user has to ensure that the erase or write (program) time is neither too short or too long.

The ETIM register address is F5H. Table 1 contains the values which must be written to the ETIM register by software for various oscillator frequencies (the default value is 08H after RESET).

The general formula is:

5ms Write time:

$$\text{Value (decimal, to be rounded up)} = \frac{f_{\text{XTAL1}} [\text{kHz}]}{204.8} - 2$$

10ms Write time:

$$\text{Value (decimal)} = \frac{f_{\text{XTAL1}} [\text{kHz}]}{96} - 2$$

### Control Register (ECNTRL)

See Figure 2 for a description of this register. The ECNTRL register address is F6H.

Table 1. Values for the Timer Register (ETIM)

f <sub>XTAL1</sub>	VALUES FOR ETIM			
	5ms WRITE TIME		10ms WRITE TIME	
	HEX	DEC	HEX	DEC
1.0MHz	03	3	08	8
2.0MHz	08	8	13	19
3.0MHz	0D	13	1D	29
4.0MHz	12	18	28	40
5.0MHz	17	23	32	50
6.0MHz	1C	28	3C	60
7.0MHz	21	33	47	71
8.0MHz	26	38	51	81
9.0MHz	2A	42	5C	92
10.0MHz	2F	47	66	102
11.0MHz	34	52	71	113
12.0MHz	39	57	7B	123
13.0MHz	3E	62		
14.0MHz	43	67		
15.0MHz	48	72		
16.0MHz	4D	77		

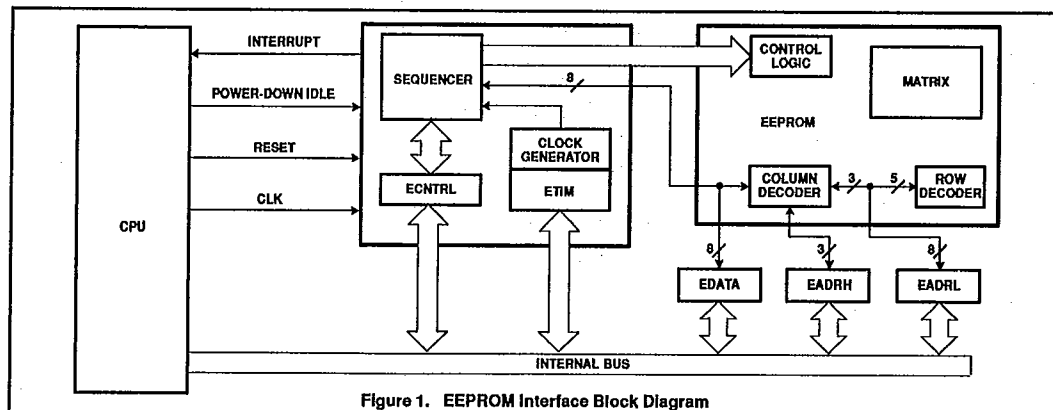


Figure 1. EEPROM Interface Block Diagram

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7	6	5	4	3	2	1	0
IFE	EEINT	EWP	--	ECNTRL3	ECNTRL2	ECNTRL1	ECNTRL0

Bit	Symbol	Function
ECNTRL7	IFE	Active high EEPROM interrupt flag: set by the sequencer or by software; reset by software. When set and enabled, this flag forces an interrupt to the same vector as the serial port interrupt (see Interrupt section).
ECNTRL6	EEINT	EEPROM interrupt enable: set and reset by software (active high).
ECNTRL5	EWP	Erase/write in progress flag: set and reset by the sequencer (active high). When EWP is set, access to the EEPROM is not possible. EWP cannot be set or reset by software.
ECNTRL4		Reserved.
ECNTRL3-ECNTRL0		See table below.

Operation	ECNTRL3	ECNTRL2	ECNTRL1	ECNTRL0
Byte mode	0	0	0	0
Row erase	1	1	0	0
Page write*	--	--	--	--
Page erase/write* block erase	1	0	1	0

\*Future products.

**Byte mode:** Normal EEPROM mode, default mode after reset. In this mode, data can be read and written to one byte at a time.

**Read mode:** This is the default mode when byte mode is selected. This means that the contents of the addressed byte are available in the data register.

**Write mode:** This mode is activated by writing to the data register. The address register must be loaded first. Since the old contents are read first (by default), this allows the sequencer to decide whether an erase/write or write cycle only (data = 00H) is required.

**Row erase:** In this mode, the addressed row is cleared. The three LSBs of EADRL are not significant, i.e. the 8 bytes addressed by EADRL are cleared in the same time normally needed to clear one byte ( $t_{\text{CERASE}} = t_c = t_w$ ). For the following write modes, only the write and not the erase/write cycle is required. For example, using the row erase mode, programming 8 bytes takes  $t_{\text{TOTAL}} = t_c + 8 \times t_w$  compared to  $t_{\text{TOTAL}} = 8 \times t_c + 8 \times t_w$  ( $t_c = t_{\text{CERASE}} \cdot t_w = t_{\text{WRITE}}$ ).

**Page write:** For future products.

**Page erase/write:** For future products

**Block erase:** In this mode all 256 bytes are cleared. The byte containing the security bits is also cleared.  $t_{\text{BLOCKERASE}} = t_c$ . The contents of EADRH, EADRL and EDAT are insignificant.

## Program Sequences and Register Contents after Reset

The contents of the EEPROM registers after a Reset are the default values:

EADRH	= 1xxxxxxB	(security bit address)
EADRL	= 00H	(security bit address)
ETIM	= 08H	(minimum erase time with the lowest permissible oscillator frequency)
ECNTRL	= 00H	(Byte mode, read)
EDAT	= xxH	(security bit)

**Initialize:** MOV ETIM, ..  
MOV EADRH, ..

**Read:** MOV EADRL, ..  
MOV ..., EDAT

**Write:** MOV EADRL, ..  
MOV EDAT, ..

**Erase row:** MOV EADRL, .. Row address, 3LSBs don't care  
MOV ECNTRL, #0CH Erase row mode  
MOV EDAT, .. (EDAT) don't care

**Erase block:** MOV ECNTRL, 0AH Erase block mode  
MOV EDAT, .. (EDAT) don't care

If the security bit is to be altered, the program generally starts as follows:

MOV EADRH, #80H  
MOV EADRL, #00H

Figure 2. Control Register (ECNTRL)

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## Security Facilities

### EEPROM Protection

The EEPROM is protected using four security bits which are contained in an extra EEPROM byte at address 8000H (EADRH/EADRL). They can be set or cleared by software. To activate the EEPROM protection, the program sequence in byte mode must be as follows:

```
MOV EADRH, #80H
MOV EADRL, #00H
MOV EDAT, #FFH
```

If two or more of these bits are reset, SB = 0, the security mode is disabled and the EEPROM is not protected. If three or four bits are set, SB = 1 and the EA mode differs from the internal access mode.

In this case, access to the EEPROM is only possible in one mode regardless of how the external access mode is reached (by pulling

the EA pin low or by passing the 4K boundary). For SB = 1 and "external access" only, the "block erase" mode is enabled. The program sequence has to be as follows:

```
MOV EADRH, #80H (security byte address)
MOV EADRL, #00H (security byte address)
MOV ECNTRL, #0AH (block erase mode)
MOV EDAT, #xxH (start block erase)
```

All 256 data bytes, the security bits, and SB will be cleared after completing this mode (EWP = 0). SB will also be affected in byte mode when writing to the security byte (not for SB = 1 and "external access"). Figure 3 illustrates the access to SB.

### ROM Code Protection

Since the external access mode can only be selected by pulling the EA pin low during reset, it is not possible to read the internal program memory using the MOVC instruction while executing external program memory. Furthermore, it is not possible to change this

mode to internal access within the MOVC cycle.

Additionally, a mask-programmable ROM code protection facility is available. When the program memory passes the 4K boundary using both the internal and external ROMs, it is not possible to access the internal ROM from the external program memory if the mask-programmable ROM security bit is set. An access to the lower 4K bytes of program memory using the MOVC instruction is only possible while executing internal program memory.

Also the verification mode (test-mode which writes the ROM contents to a port for comparison with a reference code) is not implemented for security reasons. A different test-mode is implemented for test purposes. This mode allows every bit to be tested. However, the internal code cannot be accessed via a port.

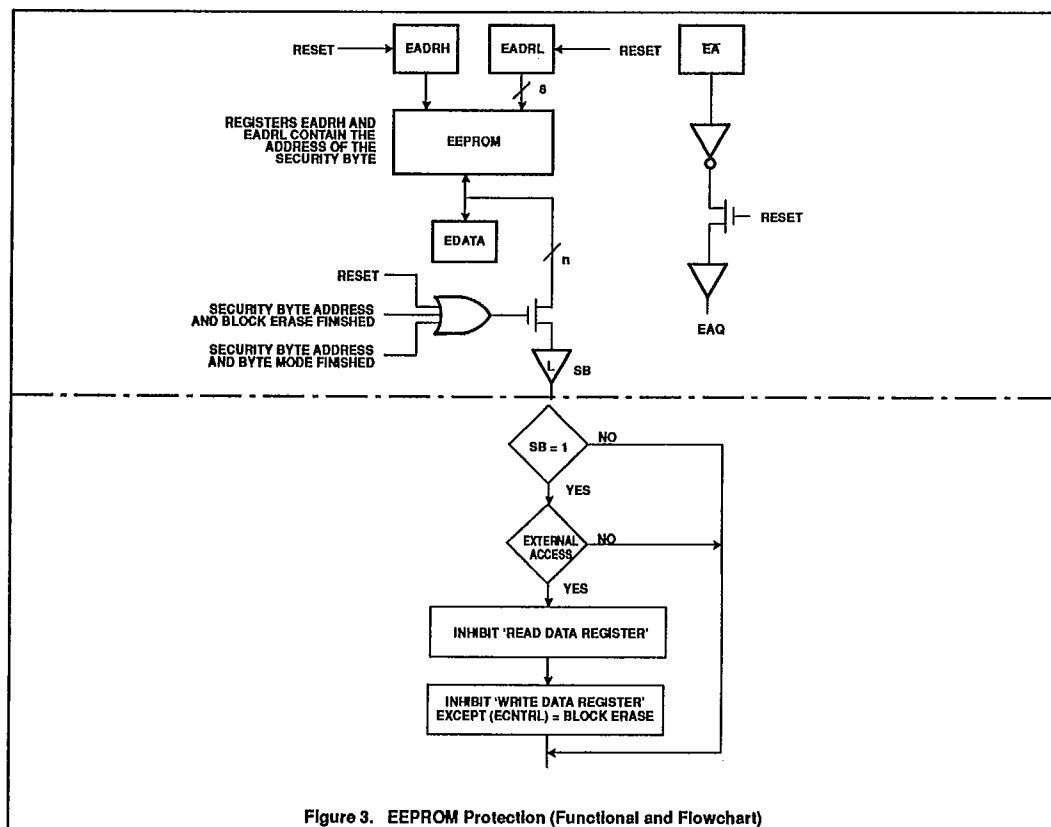


Figure 3. EEPROM Protection (Functional and Flowchart)

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## OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 610.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

## RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-up reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-up, the voltage on  $V_{CC}$  and RST must come up at the same time for a proper start-up.

**Note:** Before entering the idle or power-down modes, the user has to ensure that there is no EEPROM erase/write cycle in progress

(i.e., the EWP bit has to be reset before activating the idle or power-down modes; otherwise EEPROM accesses will be aborted).

## IDLE MODE

In idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

## POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM and EEPROM are preserved. A hardware reset is the only way to terminate the power-down mode. The control bits for the reduced power modes are in the special function register PCON. Table 2 shows the state of the I/O ports during low current operating modes.

## INTERRUPT SYSTEM

External events and the real-time-driven on-chip peripherals require service by the CPU asynchronous to the execution of any particular section of code. To tie the asynchronous activities of these functions to normal program execution, a multiple-source, two-priority-level, nested interrupt system is provided. Interrupt response latency is from 3µs to 7µs when using a 12MHz crystal. The S83C851 acknowledges interrupt requests from 7 sources as follows:

- INT0 and INT1: externally via pins 12 and 13, respectively,
- Timer 0 and timer 1: from the two internal counters,
- Serial port: from the internal serial I/O port or EEPROM (1 vector).

Each interrupt vectors to a separate location in program memory for its service program. Each source can be individually enabled (the EEPROM interrupt can only be enabled when the serial port interrupt is enabled) or disabled and can be programmed to a high or low priority level. All enabled sources can also be globally disabled or enabled. Both external interrupts can be programmed to be level-activated and are active low to allow "wire-ORing" of several interrupt sources to one input pin.

**Note:** The serial port and EEPROM interrupt flags must be cleared by software; all other flags are cleared by hardware.

Table 2. External Pin Status During Idle and Power-Down Modes

MODE	PROGRAM MEMORY	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2, 3</sup>

PARAMETER	RATING	UNIT
Storage temperature range	-65 to +150	°C
Voltage on any other pin to $V_{SS}$	-0.5 to +6.5	V
Input or output DC current on any single I/O pin	±5	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1.0	W

### NOTES:

- Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
- Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to  $V_{SS}$  unless otherwise noted.



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## DC ELECTRICAL CHARACTERISTICS

 $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$  ( $V_{CC} = 5\text{V} \pm 20\%$ ),  $-40^{\circ}\text{C to } +85^{\circ}\text{C}$  ( $V_{CC} = 5\text{V} \pm 20\%$ ), or  $-40^{\circ}\text{C to } +125^{\circ}\text{C}$  ( $V_{CC} = 5\text{V} \pm 10\%$ ),  $V_{SS} = 0\text{V}$ 

SYMBOL	PARAMETER	PART TYPE	TEST CONDITIONS	LIMITS		UNIT
				MIN	MAX	
$V_{IL}$	Input low voltage, except $\overline{EA}$	0 to $+70^{\circ}\text{C}$ $-40$ to $+85^{\circ}\text{C}$ $-40$ to $+125^{\circ}\text{C}$		-0.5 -0.5 -0.5	$0.2V_{CC}-0.1$ $0.2V_{CC}-0.15$ $0.2V_{CC}-0.25$	V V V
$V_{IL1}$	Input low voltage to $\overline{EA}$	0 to $+70^{\circ}\text{C}$ $-40$ to $+85^{\circ}\text{C}$ $-40$ to $+125^{\circ}\text{C}$		-0.5 -0.5 -0.5	$0.2V_{CC}-0.3$ $0.2V_{CC}-0.35$ $0.2V_{CC}-0.45$	V V V
$V_{IH}$	Input high voltage, except XTAL1, RST	0 to $+70^{\circ}\text{C}$ $-40$ to $+85^{\circ}\text{C}$ $-40$ to $+125^{\circ}\text{C}$		$0.2V_{CC}+0.9$ $0.2V_{CC}+1.0$ $0.2V_{CC}+1.0$	$V_{CC}+0.5$ $V_{CC}+0.5$ $V_{CC}+0.5$	V V V
$V_{IH1}$	Input high voltage, XTAL1, RST	0 to $+70^{\circ}\text{C}$ $-40$ to $+85^{\circ}\text{C}$ $-40$ to $+125^{\circ}\text{C}$		$0.7V_{CC}$ $0.7V_{CC}+0.1$ $0.7V_{CC}+0.1$	$V_{CC}+0.5$ $V_{CC}+0.5$ $V_{CC}+0.5$	V V V
$V_{OL}$	Output low voltage, ports 1, 2, 3 <sup>6</sup>		$I_{OL} = 1.6\text{mA}^4$		0.45	V
$V_{OL1}$	Output low voltage, port 0, ALE, $\overline{PSEN}$ <sup>6</sup>		$I_{OL} = 3.2\text{mA}^4$		0.45	V
$V_{OH}$	Output high voltage, ports 1, 2, 3, ALE, $\overline{PSEN}$		$I_{OH} = -60\mu\text{A}$ $I_{OH} = -25\mu\text{A}$ $I_{OH} = -10\mu\text{A}$	2.4 $0.75V_{CC}$ $0.9V_{CC}$		V V V
$V_{OH1}$	Output high voltage, port 0 in external bus mode <sup>6</sup>		$I_{OH} = -800\mu\text{A}$ $I_{OH} = -300\mu\text{A}$ $I_{OH} = -80\mu\text{A}$	2.4 $0.75V_{CC}$ $0.9V_{CC}$		V V V
$I_{IL}$	Logical 0 input current, ports 1, 2, 3	0 to $+70^{\circ}\text{C}$ $-40$ to $+85^{\circ}\text{C}$ $-40$ to $+125^{\circ}\text{C}$	$V_{IN} = 0.45\text{V}$		-50 -75 -75	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$I_{TL}$	Logical 1-to-0 transition current, ports 1, 2, 3	0 to $+70^{\circ}\text{C}$ $-40$ to $+85^{\circ}\text{C}$ $-40$ to $+125^{\circ}\text{C}$	$V_{IN} = 2.0\text{V}$		-650 -750 -750	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$I_{L1}$	Input leakage current, port 0, $\overline{EA}$		$0.45\text{V} < V_I < V_{CC}$		$\pm 10$	$\mu\text{A}$
$I_{CC}$	Power supply current: Active mode @ 16MHz <sup>1</sup> Idle mode @ 16MHz <sup>2</sup> Power down mode <sup>3</sup>		See note 7		32 6.5 100	$\text{mA}$ $\text{mA}$ $\mu\text{A}$
$R_{RST}$	Internal reset pull-down resistor			50	150	k $\Omega$
$C_{IO}$	Pin capacitance		$f = 1\text{MHz}$		10	pF

### NOTES:

- The operating supply current is measured with all output pins disconnected; XTAL1 driven with  $t_r = t_f = 5\text{ns}$ ;  $V_{IL} = V_{SS} + 0.5\text{V}$ ;  $V_{IH} = V_{CC} - 0.5\text{V}$ ; XTAL2 not connected;  $\overline{EA} = \text{RST} = \text{Port 0} = V_{CC}$ .
- The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with  $t_r = t_f = 5\text{ns}$ ;  $V_{IL} = V_{SS} + 0.5\text{V}$ ;  $V_{IH} = V_{CC} - 0.5\text{V}$ ; XTAL2 not connected;  $\overline{EA} = \text{Port 0} = V_{CC}$ ; RST =  $V_{SS}$ .
- The power-down current is measured with all output pins disconnected; XTAL2 not connected;  $\overline{EA} = \text{Port 0} = V_{CC}$ ; RST = XTAL1 =  $V_{SS}$ .
- Capacitive loading on Port 0 and Port 2 may cause spurious noise pulses to be superimposed on the LOW level output voltage of ALE, Port 1 and Port 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make a 1-to-0 transition during bus operations. In the worst cases (capacitive loading  $> 100\text{pF}$ ), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
- Capacitive loading on Port 0 and Port 2 may cause the HIGH level output voltage on ALE and  $\overline{PSEN}$  to momentarily fall below the  $0.9V_{CC}$  specification when the address bits are stabilizing.
- Under steady state (non-transient) conditions,  $I_{OL}$  must be externally limited as follows:  
Maximum  $I_{OL}$  per Port pin: 10mA  
Maximum  $I_{OL}$  per 8-bit port —  
Port 0: 26mA  
Ports 1, 2, and 3: 15mA  
Maximum total  $I_{OL}$  for all output pins: 71mA.  
If  $I_{OL}$  exceeds the test condition,  $V_{OL}$  may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
- See Figures 11 through 14 for  $I_{CC}$  test conditions.

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## AC ELECTRICAL CHARACTERISTICS<sup>1, 2</sup>

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$t_{\text{OCLCL}}$	4	Oscillator frequency			1.2	16	MHz
$t_{\text{HLL}}$	4	ALE pulse width	85		$2t_{\text{OCLCL}}-40$		ns
$t_{\text{AVLL}}$	4	Address valid to ALE low	8		$t_{\text{OCLCL}}-55$		ns
$t_{\text{LLAX}}$	4	Address hold after ALE low	28		$t_{\text{OCLCL}}-35$		ns
$t_{\text{LLIV}}$	4	ALE low to valid instruction in		150		$4t_{\text{OCLCL}}-100$	ns
$t_{\text{LLPL}}$	4	ALE low to PSEN low	23		$t_{\text{OCLCL}}-40$		ns
$t_{\text{PLPH}}$	4	PSEN pulse width	143		$3t_{\text{OCLCL}}-45$		ns
$t_{\text{PLIV}}$	4	PSEN low to valid instruction in		83		$3t_{\text{OCLCL}}-105$	ns
$t_{\text{PIXX}}$	4	Input instruction hold after PSEN	0		0		ns
$t_{\text{PIXZ}}$	4	Input instruction float after PSEN		38		$t_{\text{OCLCL}}-25$	ns
$t_{\text{AVIV}}$	4	Address to valid instruction in		208		$5t_{\text{OCLCL}}-105$	ns
$t_{\text{PLAZ}}$	4	PSEN low to address float		10		10	ns
<b>Data Memory</b>							
$t_{\text{RLRH}}$	5, 6	RD pulse width	275		$6t_{\text{OCLCL}}-100$		ns
$t_{\text{WLWH}}$	5, 6	WR pulse width	275		$6t_{\text{OCLCL}}-100$		ns
$t_{\text{RLDV}}$	5, 6	RD low to valid data in		148		$5t_{\text{OCLCL}}-165$	ns
$t_{\text{RHDX}}$	5, 6	Data hold after RD	0		0		ns
$t_{\text{RHDX}}$	5, 6	Data float after RD		55		$2t_{\text{OCLCL}}-70$	ns
$t_{\text{LLDV}}$	5, 6	ALE low to valid data in		350		$8t_{\text{OCLCL}}-150$	ns
$t_{\text{AVDV}}$	5, 6	Address to valid data in		398		$9t_{\text{OCLCL}}-165$	ns
$t_{\text{LLWL}}$	5, 6	ALE low to RD or WR low	138	238	$3t_{\text{OCLCL}}-50$	$3t_{\text{OCLCL}}+50$	ns
$t_{\text{AW}}$	5, 6	Address to RD or WR	120		$4t_{\text{OCLCL}}-130$		ns
$t_{\text{OW}}$	5, 6	Data setup time before WR	288		$7t_{\text{OCLCL}}-150$		ns
$t_{\text{QVWX}}$	5, 6	Data valid to WR transition	3		$t_{\text{OCLCL}}-60$		ns
$t_{\text{WHOX}}$	5, 6	Data hold after WR	13		$t_{\text{OCLCL}}-50$		ns
$t_{\text{RLAZ}}$	5, 6	RD low to address float		0		0	ns
$t_{\text{WHLH}}$	5, 6	RD or WR high to ALE high	23	103	$t_{\text{OCLCL}}-40$	$t_{\text{OCLCL}}+40$	ns
<b>External Clock</b>							
$t_{\text{CHCX}}$	8	High time	20		20		ns
$t_{\text{CLCX}}$	8	Low time	20		20		ns
$t_{\text{CLCH}}$	8	Rise time		20		20	ns
$t_{\text{CHCL}}$	8	Fall time		20		20	ns
<b>Erase/write timer constant<sup>3</sup></b>							
$t_{\text{EW}}$		Erase/write cycle time	10	40	10	40	ms
$t_{\text{E}}$		Erase time	5	40	5	40	ms
$t_{\text{W}}$		Write time	5	40	5	40	ms
$t_{\text{S}}$		Data retention time <sup>4</sup>	10		10		years
NE/W		Erase/write cycles <sup>5</sup>	50,000		50,000		cycles

### NOTES:

- Parameters are valid over operating temperature range unless otherwise specified.
- Load capacitance for port 0, ALE, and PSEN = 100pF, load capacitance for all other outputs = 80pF.
- The power-off fall-time of  $V_{\text{CC}}$  must be less than 1ms to prevent an overwrite pulse from being generated in the EEPROM which can cause spurious parasitic writing to EEPROM cells. If the  $V_{\text{CC}}$  power-off full-time is greater than 1ms, a power-off reset signal should be generated to prevent this condition from occurring.
- Test condition:  $T_{\text{amb}} = +55^{\circ}\text{C}$ .
- Number of erase/write cycles for each EEPROM byte.

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## EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

**A – Address**

**C — Clock**

D – Input data

H – Logic level high

1 - Instruction (program memory contents)

L --- Logic level low, or ALE

P – PSEN

Q – Output data

R –  $\overline{RD}$  signal

**t** – Time

V - Valid

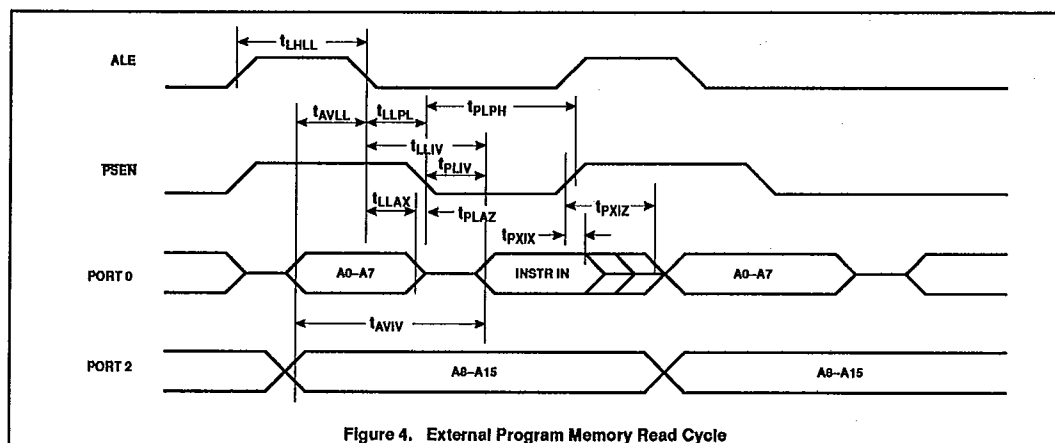
W- WR signal

X – No longer a valid logic level

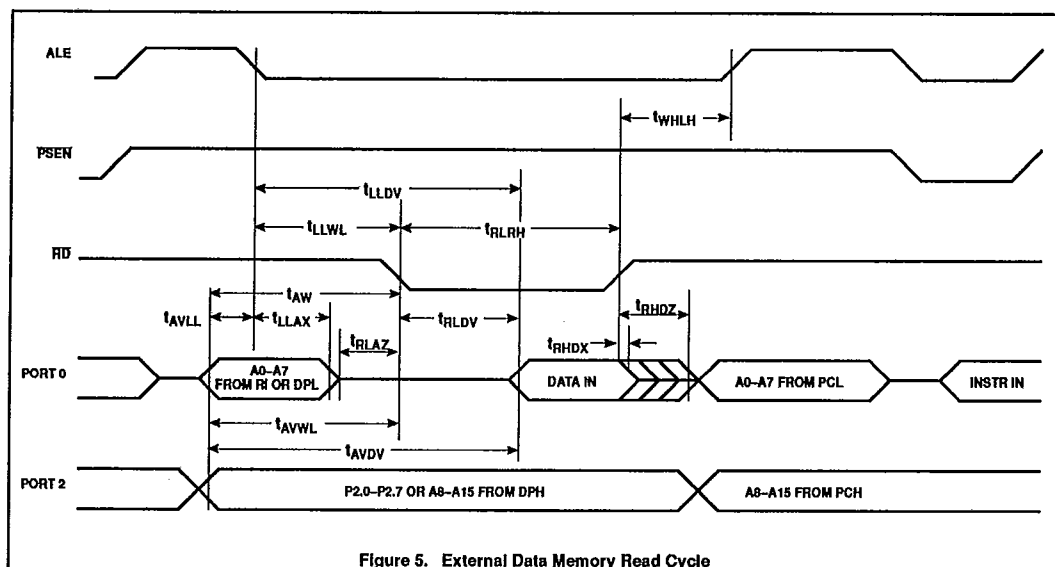
Z - Float

**Examples:**  $t_{AVLL}$  = Time for address valid to ALE low.

$t_{LLPL}$  = Time for ALE low to  $\overline{PSEN}$  low.



#### Figure 4. External Program Memory Read Cycle

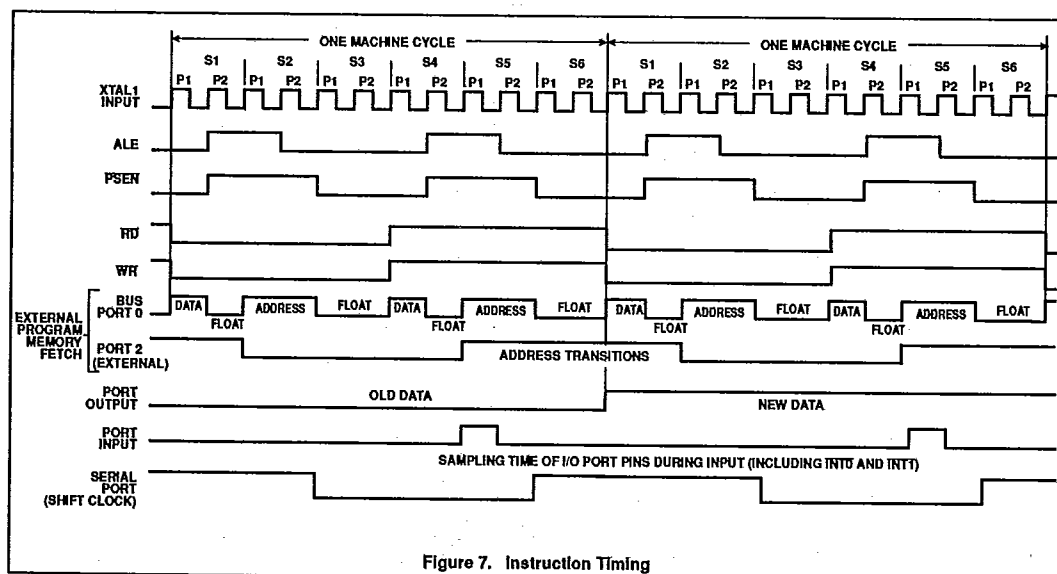
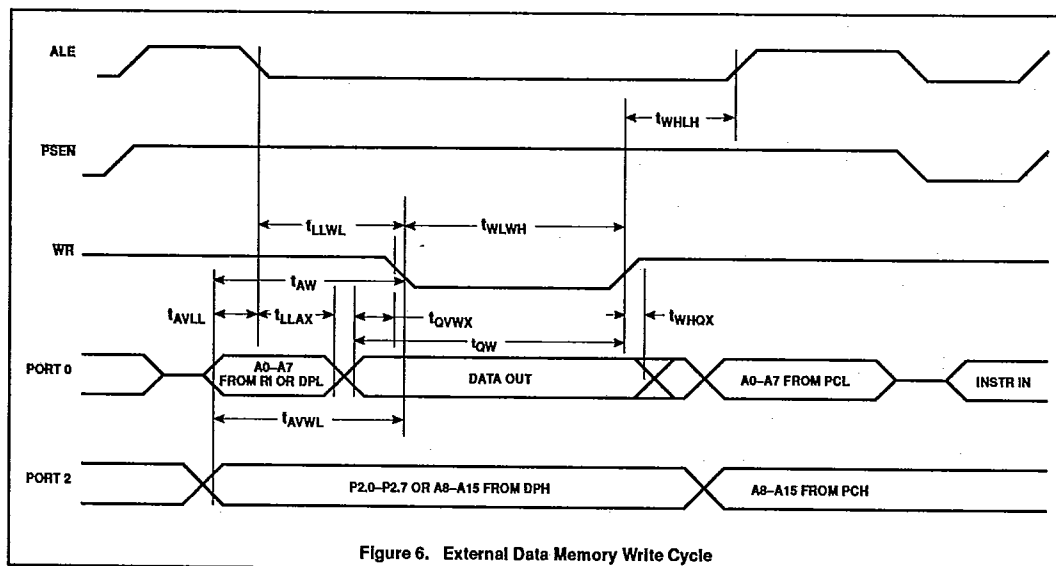


**Figure 5. External Data Memory Read Cycle**

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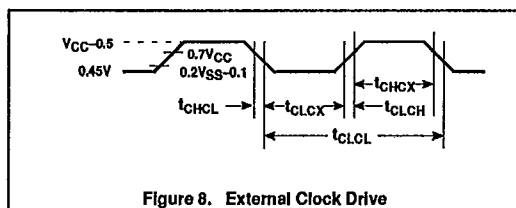
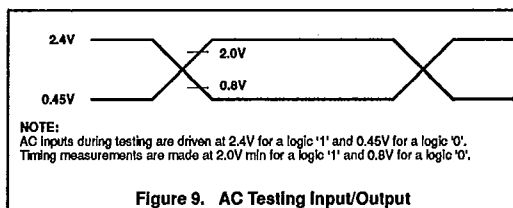
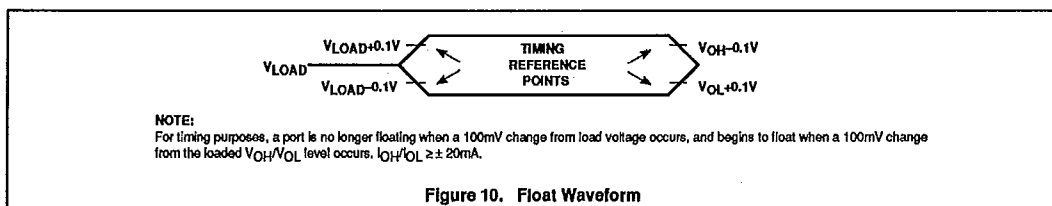
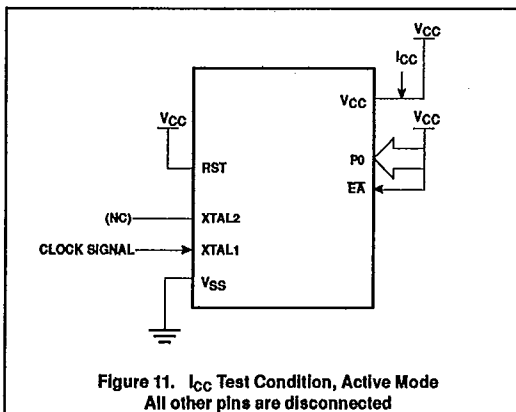
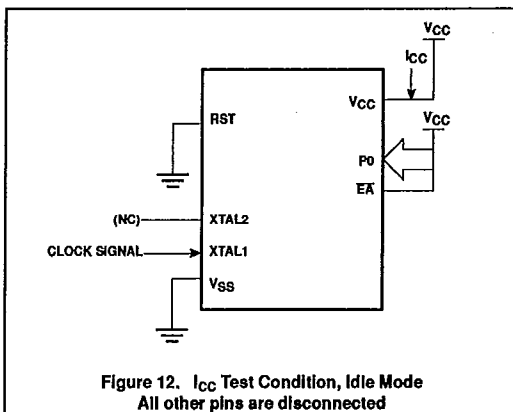
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**Table 3. External Clock Drive XTAL1**Oscillator circuitry: The capacities connected to the crystal should be:  $C1 = C2 = \text{tbf.}$ 

SYMBOL	PARAMETER	VARIABLE CLOCK $f = 1.2 - 16\text{MHz}$		UNIT
		MIN	MAX	
$t_{\text{CLCL}}$	Oscillator clock period	63	833	ns
$t_{\text{HIGH}}$	HIGH time	20	$t_{\text{CLCL}} - t_{\text{LOW}}$	ns
$t_{\text{LOW}}$	LOW time	20	$t_{\text{CLCL}} - t_{\text{HIGH}}$	ns
$t_r$	Rise time	—	20	ns
$t_f$	Fall time	—	20	ns
$t_{\text{CY}}$	Cycle time <sup>1</sup>	0.75	10	ns

**NOTE:**1.  $t_{\text{CY}} = 12 t_{\text{CLCL}}$ .**Figure 8. External Clock Drive****Figure 9. AC Testing Input/Output****Figure 10. Float Waveform****Figure 11.  $I_{\text{CC}}$  Test Condition, Active Mode**  
All other pins are disconnected**Figure 12.  $I_{\text{CC}}$  Test Condition, Idle Mode**  
All other pins are disconnected

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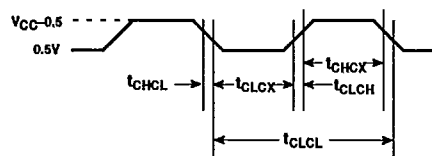


Figure 13. Clock Signal Waveform for  $I_{CC}$  Tests  
In Active and Idle Modes  
 $t_{CLCH} = t_{CHCL} = 5\text{ns}$

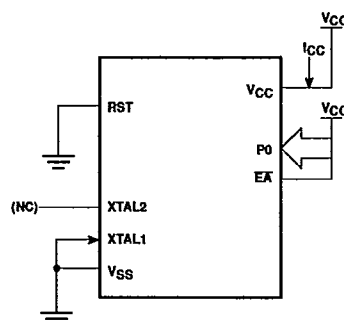


Figure 14.  $I_{CC}$  Test Condition, Power Down Mode  
All other pins are disconnected.  
 $V_{CC} = 2\text{V to } 5.5\text{V}$