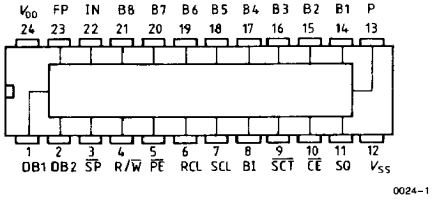
SIEMENS

PEB 2030
Frame Aligner Circuit (FRAC)

- Detection of Frame Alignment Signals for PCM 30 Highways in Accordance with CCITT Recommendations G 737, 738, 739
- Delay Compensation and Clock Alignment between Transmission Line and Exchange
- Compensation of Phase Jitter up to 60 μs
- Detection and Initiation of Route Alarms (AIS, Service Word)
- Loss of Frame Alignment Indicator
- Slip Detection
- Error Simulation for Test Purposes
- Digital Interface, TTL-Compatible
- NMOS

Pin Configuration

(Top View)



Pin Definitions

Pin	Symbol	Function
1	DB 1	} Data Interfaces (DBi)
2	DB 2	
3	$\overline{SP}$	Synchronous Pulse
4	R/$\overline{W}$	Direction of Data Transfer
5	$\overline{PE}$	Alarm Port Enable
6	RCL	Route Clock
7	SCL	Station Clock
8	$\overline{BI}$	Buffer Inactive
9	$\overline{SCT}$	Station Counter Trigger Pulse
10	$\overline{CE}$	Chip Enable
11	SO	Serial Output
23	FP	Fault Pulse
22	IN	PCM Input
14	B 1	} Parallel Outputs (Bi)
.	.	
.	.	
.	.	
21	B 8	
13	P	Parity Bit
12	V_{SS}	Ground (0V)
24	V_{DD}	Supply Voltage (+5V)

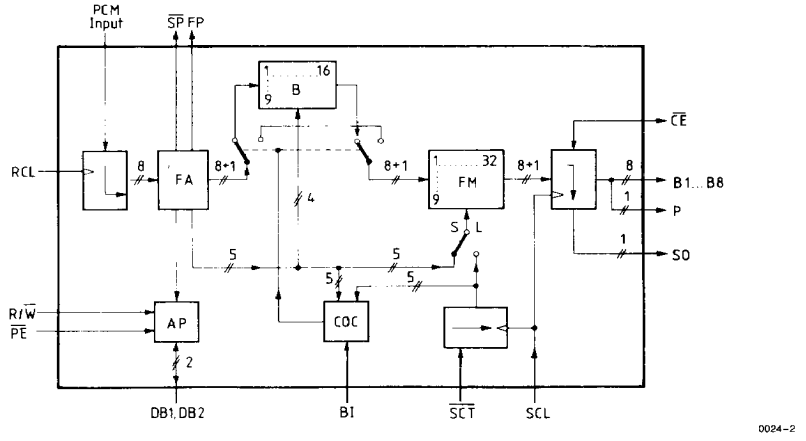
The PEB 2030 frame aligner circuit is used for interfacing PCM 30 routes with PCM switching networks.

Its main applications are as follows:
- In multiplex units for PCM transmission routes
- In concentrators and subscriber multiplexers at one end of PCM routes
- As interface between PCM routes and public and private PCM switches (DIU)
- For delay compensation between switching stages

The Siemens frame aligner circuit PEB 2030 is a monolithic NMOS circuit. Its main application is detection of frame alignment signals of PCM 30 routes according to CCITT Recommendations G 737, 738, 739 and clock adjustment with delay compensation between PCM routes and PCM switches.

An incorporated buffer enables the PEB 2030 to compensate phase jitter up to 60 μs. Route alarms can be challenged by a bidirectional data interface.

Block Diagram



FA Frame Alignment
AP Alarm Port
B Buffer
COC Coincidence Circuit
FM Frame Memory

Functional Description

The PEB 2030 IC is fabricated using N-channel depletion technology.

The circuit, connected to a PCM 30 line, and the associated input clock (route clock RCL), are synchronized with the PCM frame in accordance with CCITT Recommendation G 732. In the stable condition the circuit supplies 488 ns synchronous pulses ($\overline{SP}$) at a bit rate of 4 Kbits/s which identify the beginning of the PCM frames containing the bunched frame alignment signal (FAS). During the synchronizing phase and in the event of frame alignment signal (FAS), the synchronizing pulses are suppressed and a 2 μs fault pulse FP is delivered every 250 μs. When a synchronized state exists, such a fault pulse appears only if a FAS is not recognized.

On the output side the PCM information can be read out in serial or parallel form. For this purpose, a reading clock (SCL) and a 488 ns reading synchronizing pulse ($\overline{SCT}$) must be applied at 250 μs intervals to fix the beginning of the frame. The circuit supplies a parity check bit (even parity) to each PCM word via a tristate output which is activated by a chip enable ($\overline{CE}$) in the same way as the tristate outputs for the parallel information.

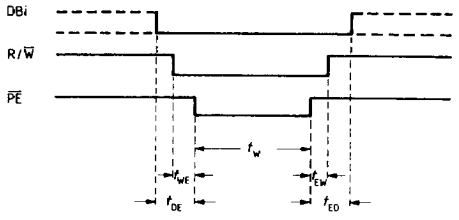
An alarm flipflop (FA alarm) in the circuit is set in the event of frame alignment loss, route timing loss or loss of the $\overline{CE}$ or $\overline{SCT}$ signals. The alarm bit is recorded in another flipflop in the service word (bit 3), whereas a third flipflop stage is set when logic "1" signals are received by the PCM route for the duration of two frames (Alarm Indication Signal AIS). A further flipflop is set when a slip of the frame occurs. The alarms are polled via a bidirectional data interface. The alarm circuits can be triggered and reset for test purposes via the data interface.

Description of Individual Pins

Symbol	Features	Description
1. Supply		
V_{DD}	+5V ±5%	Typical Power Consumption 300 mW.
V_{SS}	0V	
2. PCM Interfaces		
IN		PCM Input. Information Bit from One Negative RCL Edge to the Next.
RCL	2.048 MHz ±50 ppm	Route Clock.
B1...B8	256 Kbit/s	Parallel PCM Output Information. B1 = Most Significant Information Bit.
P	256 Kbit/s	Parity Bit (Even Parity).
SO	2.048 Mbit	Serial PCM Output. Bit Sequence with Decreasing Significance.
SCL	2.048 MHz	Station Clock. Information Bits from One Negative SCL Edge to the Next.
3. Control Signals		
$\overline{SCT}$	4 Kbit/s Width 488 ns	From One Negative SCL Edge to the Next. Frame Begins at Positive $\overline{SCT}$ edge.
$\overline{SP}$	4 Kbit/s Width 488 ns	From One Negative RCL Edge to the Next. Frame Begins with FAS at Positive $\overline{SP}$ Edge.
BI		Continuous Signal. BI = 1 or Not Connected: Buffer Inactive.
FP	Width: 4 × 488 ns = 1.95 µs	Fault Pulse Delivered for Every Undetected FAS or Every 250 µs is the Event of Frame Alignment Loss.
$\overline{CE}$	256 Kbit, with 488 ns or Continuous Level	Chip Enable Controls Outputs B1 to B8, P Low-Impedance. The $\overline{CE}$ Must be Active During the $\overline{SCT}$, so that the $\overline{SCT}$ Supervision by Station Counter is Not Impaired.

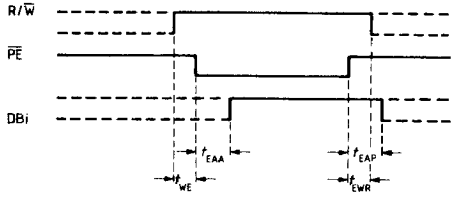
4.0 Data Interface

Write



DBi Input Timing (Write
$t_W > 1\ \mu s$
$t_{WE} > 100$ ns
$t_{DE} > 100$ ns
$t_{EW} > 50$ ns
$t_{ED} > 150$ ns

Read



DBi Output Timing (Read)
$t_{EWR} > 100$ ns
$0.8 < t_{EAA} < 1.2\ \mu s$
$C_L = 300$ pF
$t_{EAP} > 160$ ns
$t_{WE} > 100$ ns

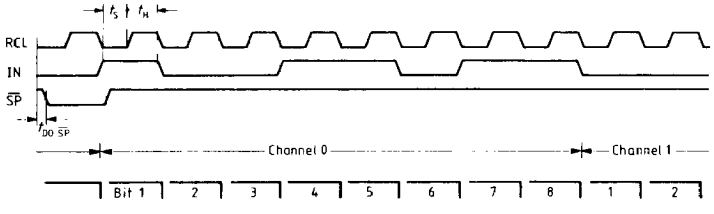
Data Transfer Direction
R/$\overline{W}$ = 1 Read Alarm Port
R/$\overline{W}$ = 0 Write Alarm Port
Alarm Port Enable
Bidirectional Data Interface for Command Acceptance or Alarm Signaling:

DB2	DB1	
0	0	Command: Poll FA, Alarm, AIS Alarm
0	1	Command: Poll B3 of the Service Word Slip Alarm
1	0	Command: Reset Alarm Flipflop
1	1	Command: Alarm Simulation

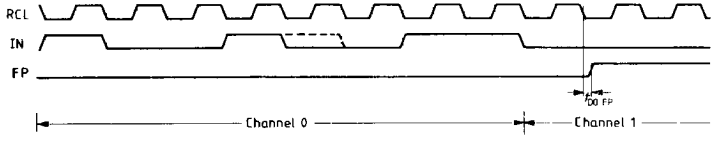
Note:
Alarms are Signalled as Log. "1"

Pulse Diagram

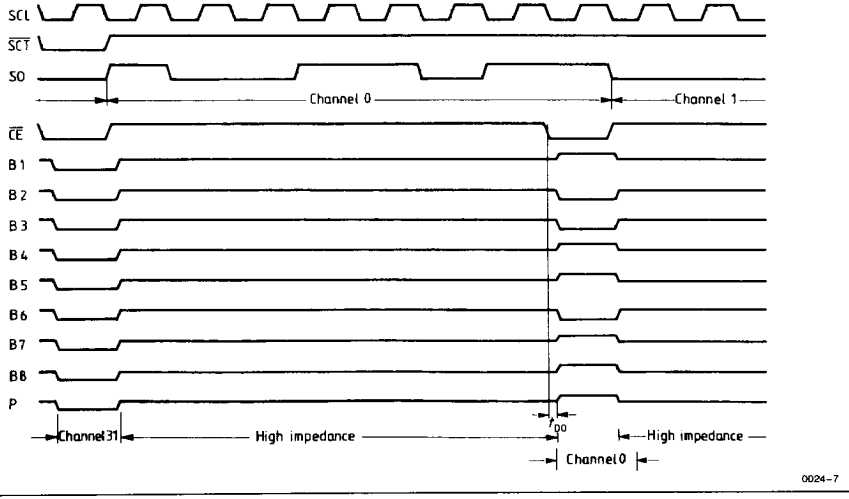
Delivery of Synchronous Pulse $\overline{SP}$ in Synchronized State



Delivery of Fault Pulse FP in the Event of Erroneous Frame Alignment Signal



Output Signals (B1 to B8, P) as Functions of the Station Trigger Pulse $\overline{SCT}$ and Chip Enable $\overline{CE}$



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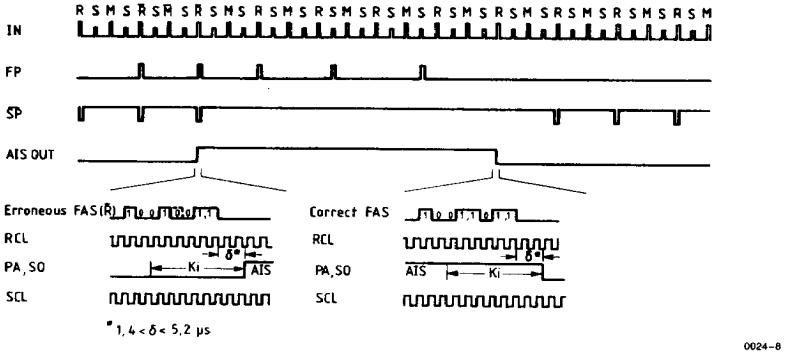
Pulse Diagram (Continued)

Loss of Frame Alignment Due to Bit Falsification on the PCM Route



R	Frame Alignment Signal (FAS)
M	Service Word
S	Simulated FAS (Random FAS)
$\overline{R}$	Erroneous FAS
$\overline{M}$	Erroneous Service Word

Absolute Maximum Ratings*

Input Voltage (V_I) . . . . . −0.3V to +7.0V
Supply Voltage (V_{DD}) . . . . . −0.3V to +7.0V
Operating Temperature (T_A) . . . . . 0°C to +70°C
Storage Temperature (T_{stg}) . . . . . −55°C to +125°C
Total Power Consumption (P_{tot}) . . . . . 400 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (T_A = 25°C)

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Supply Voltage	V_{DD}	4.75	5	5.25	V
Supply Current	I_S		50	70	mA
Input Current	I_{IL}	50		200	µA
H Input Voltage	V_{IH}	2.4			V
L Input Voltage	V_{IL}			0.7	V
L Output Voltage	V_{OL}			0.4	V
H Output Voltage	V_{OH}	2.7			V
H Output Current (FP, SO, SP)	I_{OH}			−0.02	mA
H Output Current (Bi, P)	I_{OH}			−0.05	mA
L Output Current (FP, SO, SP, 1 Bi, P)	I_{OL}			0.46	mA
H Output Current (DBi)	I_{OH}			−0.04	mA
L Output Current (DBi)	I_{OL}			0.9	mA

Timing Specification

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Input H–L Transfer Time	t_{HL}			20	ns
Input L–H Transfer Time	t_{LH}			20	ns
Clock Frequency (Pulse-Pause Ratio 1:1) t_{WH}:t_{WL}	f_{CL}	0.2	2.048	2.1	MHz
Setup Time	t_S	150			ns
Hold Time	t_H	40			ns

Switching Times (V_{DD} = +5V, T_A = +25°C)

Parameter		Symbol	Conditions	Limits			Units
From (Input)	To (Output)			Min	Typ	Max	
$\overline{CE}$	B1...B8, P	t_{DO}	50 pF, 10 kΩ			200	ns
SCL	DB 2, DB 1	t_{DO}	50 pF, 5 kΩ			350	ns
RCL	FP, SP	t_{DO}	15 pF, 10 kΩ			200	ns
SCL	SO	t_{DO}	15 pF, 10 kΩ			200	ns

Ordering Information

Type	Package
PEB 2030	DIC 24