

S6C1104

6 BIT 384 CHANNEL RSDS TFT-LCD SOURCE DRIVER

Nov. 2002.

Ver. 0.3

INTRODUCTION

The S6C1104 is a Source Driver suitable for Reduced Swing Differential Signaling(RSDS) digital interface. It converts 18-bit digital data into the analog voltage for 384 channels, charging each sub-pixel to the correct gray level corresponding to the digital value.

The RSDS path to the panel timing controller contributes toward lowering radiated EMI, reducing system power consumption and eliminates one of the two pixel busses used in typical XGA, SXGA TFT LCD panels. This single 9-bit differential bus conveys the 18-bit color data for XGA, SXGA panels.

FEATURES

- TFT active matrix LCD source driver LSI
- 64G/S is possible through 10 (5 by 2) external power supply and D/A converter
- Both dot inversion display and N-line inversion display are possible
- Compatible with gamma-correction
- Charge sharing function
- Logic supply voltage[VDD1] : 2.7 to 3.6 V
- LCD driver supply voltage[VDD2] : 7.0 to 12.0 V
- Output dynamic range: VSS2+0.2V to VDD2-0.2V
- Maximum operating frequency: fmax=85 MHz (internal data transmission rate at 2.7 V operation)
- Output: 384 outputs
- Reduced Swing Differential Signaling(RSDS) interface for low power consumption and low EMI.
- Minimum RSDS input swing level(CLKP, CLKN, DATAP, DATAN): 100mV
- Data bus interface control pin (DATPOL)
- TCP or COF supported

BLOCK DIAGRAM

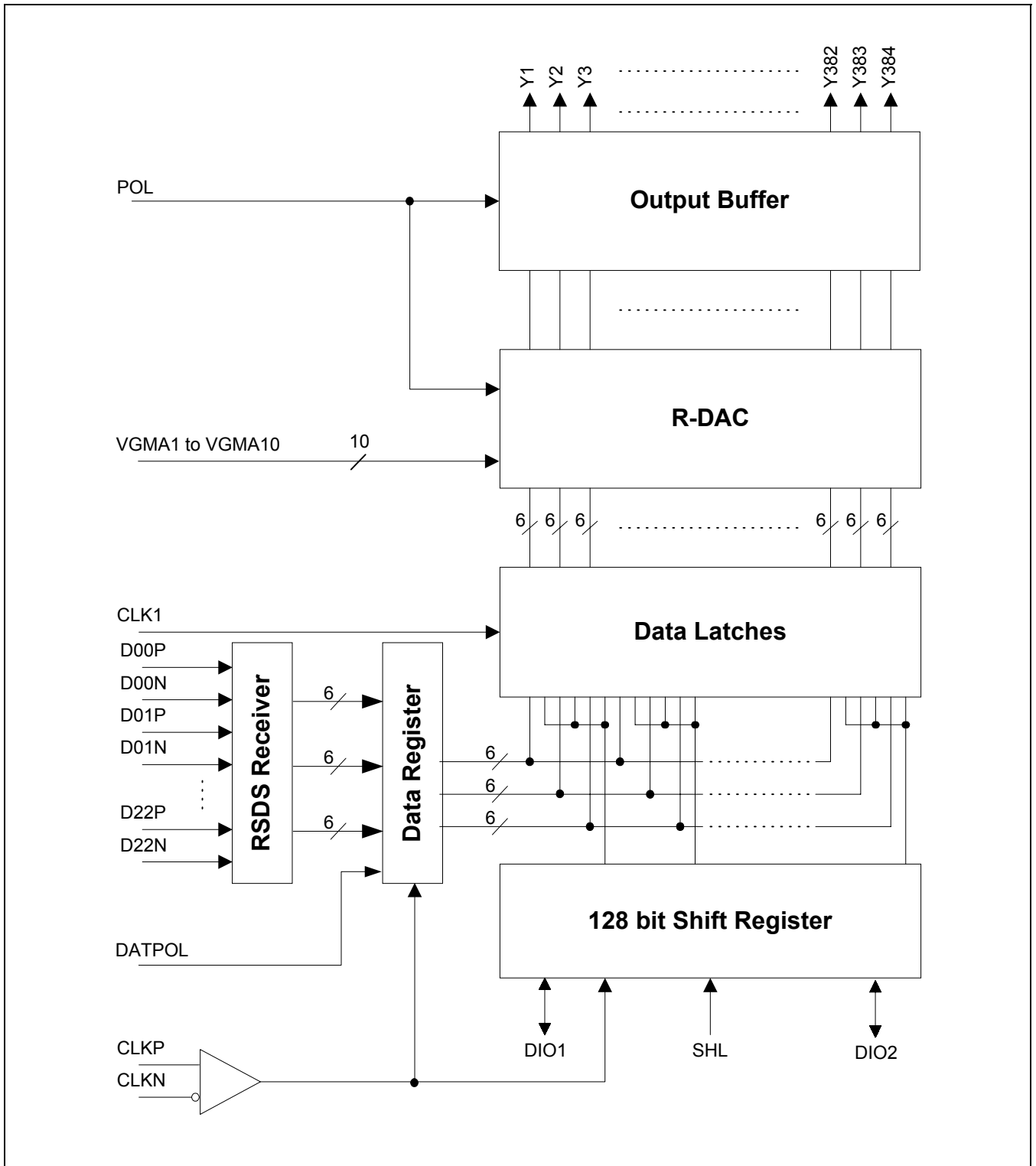


Figure 1. S6C1104 Block Diagram

PIN ASSIGNMENTS

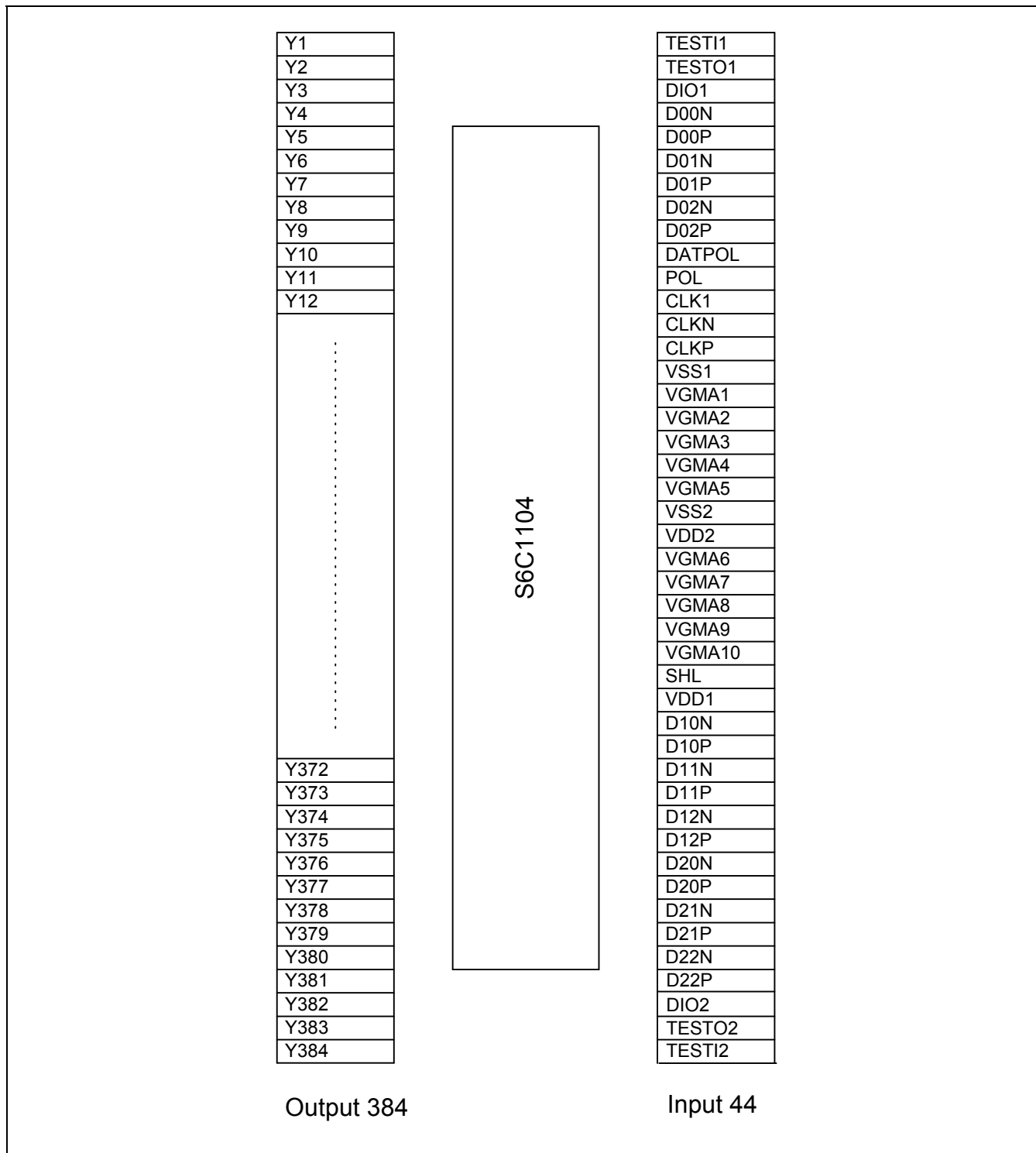


Figure 2. S6C1104 Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	2.7 to 3.6 V
VDD2	Driver power supply	7.0 to 12.0 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 to Y384	Driver outputs	The D/A converted 64 gray-scale analog voltage is output.
D0P<0:2> D0N<0:2> D1P<0:2> D1N<0:2> D2P<0:2> D2N<0:2>	RSDS data input	Total data lines consist of 18 data bus. (6-bit digital, 3 colors(R, G, B) and 2 differential input pairs) The 3-bit differential input pairs generate the internal 6-bit data through the comparison between DxxP and DxxN.
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. When SHL=H: DIO1 input, Y1→Y384, DIO2 output When SHL=L: DIO2 input, Y384→Y1, DIO1 output
DIO1	Start pulse input/output	SHL=H: Used as the start pulse input pin. SHL=L: Used as the start pulse output pin.
DIO2	Start pulse input/output	SHL=H: Used as the start pulse output pin. SHL=L: Used as the start pulse input pin.
DATPOL	Data inversion input	DATPOL= L: No inversion DATPOL= H: Data polarity inversion (DATPOL must be fixed VSS1 or VDD1.)
POL	Polarity input	POL=H: The reference voltage for odd number outputs are VGMA1 to VGMA5 and those for even number outputs are VGMA6 to VGMA10. POL=L: The reference voltage for odd number outputs are VGMA6 to VGMA10 and those for even number outputs are VGMA1 to VGMA5.
CLKP CLKN	RSDS shift clock input	The RSDS clock input pairs generate the internal shift clock, CLK2, through the comparison between CLKP and CLKN.
CLK1	Latch input	S6C1104 clears 128 shift registers at the rising edge of CLK1 and outputs the analog data to the each channel at the falling edge.
VGMA1 to VGMA10	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2>VGMA1>VGMA2>.....>VGMA9>VGMA10>VSS2 Keep power supplies unchanged during the gray-scale voltage output.
TESTI1/O1, TESTI2/O2	Amp test input/output	These pins are used for Amp test. TESTI1(=TESTI2)=L : Normal operation mode

OPERATION DESCRIPTION

RSDS RECEIVER AND DEMUX

The S6C1104 adapts the RSDS interface for EMI solution. The internal RSDS receiver block operates the comparison between the transmitted differential input pair data. The input data lines from the timing controller to the RSDS receiver consist of 6-bit digital, 3 colors, 1 port, 2 differential pairs(DxxP/DxxN).

The input common mode voltage range at the RSDS receiver is 1.2V. The differential data and clock signals from the panel timing controller arrive at the S6C1104 as multiplexed, even and odd data fields. (i.e., the data is 2:1 multiplexed). The nominal peak to peak swing of this data is 200mV across a termination resistor.

RSDS DATA BUS INTERFACE CONTROL

DATPOL controls the internal data inversion. When DATPOL="H", the internal data is inverted. The inverted data is the same that the RSDS receiver operates the comparison between the cross-transmitted differential input pair data. Using the data inversion input pin, DATPOL, the RSDS data bus interface can be changed.

DISPLAY DATA TRANSFER

When DIO1 (or DIO2) pulse is loaded into the internal latch on the falling edge of CLKP, DIO1 (or DIO2) pulse enables the operation of data transfer, so display data is valid on the 2nd falling edge of CLKP. Once all the data of 384 channels is loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLKP is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd falling edge of CLKP after the rising edge of DIO1 (or DIO2).

EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

When SHL="L", Connect DIO1 pin of the previous stage to the DIO2 pin of the next stage and all the input pins except DIO1 and DIO2 are connected together in each device.

When SHL="H", Connect DIO2 pin of the previous stage to the DIO1 pin of the next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 10 (5 by 2) gamma corrected power supplies (VGMA1 to VGMA10). Besides, to be able to deal with dot line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 5-by-2 gamma corrected voltages, input gray-scale voltages of the same polarity with respect to the common voltage, for the respective 5 gamma corrected voltages of VGMA1 to VGMA5 and VGMA6 to VGMA10.

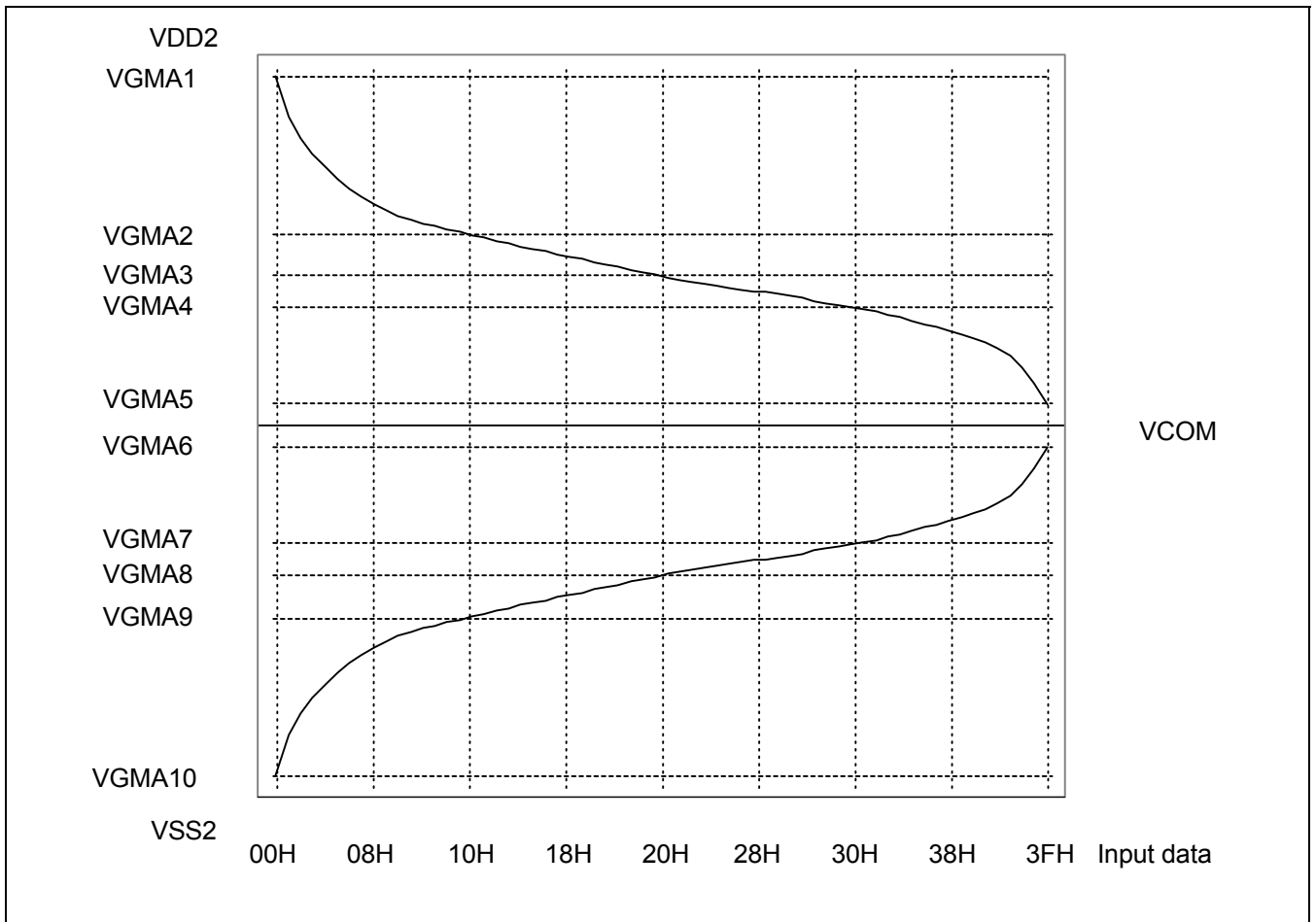
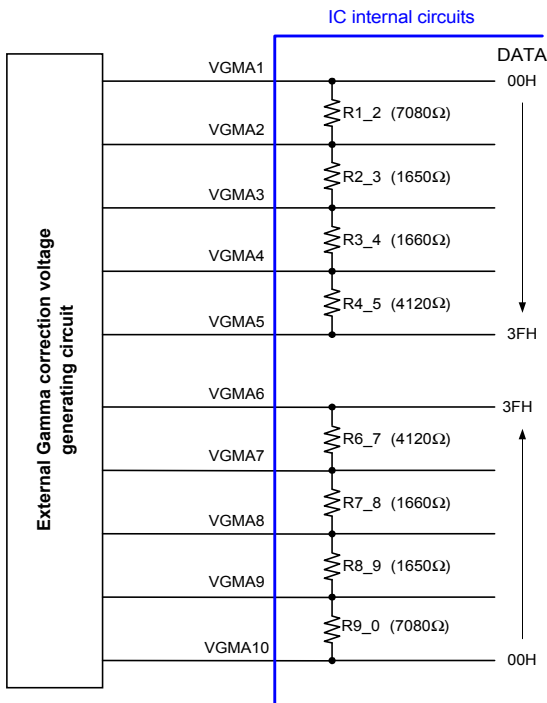


Figure 3. Gamma Correction Curve

Table 1. Resistor Strings (R0 to R62, unit: Ω)

Name	Value	Name	Value	Name	Value	Name	Value
R0	1800	R16	120	R32	100	R48	120
R1	1000	R17	110	R33	100	R49	120
R2	700	R18	110	R34	100	R50	130
R3	600	R19	110	R35	100	R51	130
R4	500	R20	100	R36	100	R52	140
R5	400	R21	100	R37	100	R53	140
R6	400	R22	100	R38	100	R54	150
R7	300	R23	100	R39	100	R55	150
R8	300	R24	100	R40	100	R56	180
R9	200	R25	100	R41	100	R57	210
R10	200	R26	100	R42	100	R58	250
R11	150	R27	100	R43	110	R59	300
R12	150	R28	100	R44	110	R60	500
R13	130	R29	100	R45	110	R61	700
R14	130	R30	100	R46	110	R62	900
R15	120	R31	100	R47	120		

Total R : 14510 Ω



The S6C1104 has on-chip dividing resistors.

The gamma correction voltage input pins are divided into two parts. Each part is connected in series with resistors. Each of these resistor series has a total typical value of 14510Ω.

Note that since these voltages are resistor divided internally, the voltages applied to the VGMA_n pins should be applied through a low-impedance circuit.

If the voltages are directly applied by the resistor divider, the desired output voltages may not result (Recommend you to use operational amplifier).

Table 2. Relationship between Input Data and Output Voltage Value

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
00H	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	1	VH1	$VGMA1+(VGMA2-VGMA1) \times 1800/7080$
02H	0	0	0	0	1	0	VH2	$VGMA1+(VGMA2-VGMA1) \times 2800/7080$
03H	0	0	0	0	1	1	VH3	$VGMA1+(VGMA2-VGMA1) \times 3500/7080$
04H	0	0	0	1	0	0	VH4	$VGMA1+(VGMA2-VGMA1) \times 4100/7080$
05H	0	0	0	1	0	1	VH5	$VGMA1+(VGMA2-VGMA1) \times 4600/7080$
06H	0	0	0	1	1	0	VH6	$VGMA1+(VGMA2-VGMA1) \times 5000/7080$
07H	0	0	0	1	1	1	VH7	$VGMA1+(VGMA2-VGMA1) \times 5400/7080$
08H	0	0	1	0	0	0	VH8	$VGMA1+(VGMA2-VGMA1) \times 5700/7080$
09H	0	0	1	0	0	1	VH9	$VGMA1+(VGMA2-VGMA1) \times 6000/7080$
0AH	0	0	1	0	1	0	VH10	$VGMA1+(VGMA2-VGMA1) \times 6200/7080$
0BH	0	0	1	0	1	1	VH11	$VGMA1+(VGMA2-VGMA1) \times 6400/7080$
0CH	0	0	1	1	0	0	VH12	$VGMA1+(VGMA2-VGMA1) \times 6550/7080$
0DH	0	0	1	1	0	1	VH13	$VGMA1+(VGMA2-VGMA1) \times 6700/7080$
0EH	0	0	1	1	1	0	VH14	$VGMA1+(VGMA2-VGMA1) \times 6830/7080$
0FH	0	0	1	1	1	1	VH15	$VGMA1+(VGMA2-VGMA1) \times 6960/7080$
10H	0	1	0	0	0	0	VH16	VGMA2
11H	0	1	0	0	0	1	VH17	$VGMA2+(VGMA3-VGMA2) \times 120/1650$
12H	0	1	0	0	1	0	VH18	$VGMA2+(VGMA3-VGMA2) \times 230/1650$
13H	0	1	0	0	1	1	VH19	$VGMA2+(VGMA3-VGMA2) \times 340/1650$
14H	0	1	0	1	0	0	VH20	$VGMA2+(VGMA3-VGMA2) \times 450/1650$
15H	0	1	0	1	0	1	VH21	$VGMA2+(VGMA3-VGMA2) \times 550/1650$
16H	0	1	0	1	1	0	VH22	$VGMA2+(VGMA3-VGMA2) \times 650/1650$
17H	0	1	0	1	1	1	VH23	$VGMA2+(VGMA3-VGMA2) \times 750/1650$
18H	0	1	1	0	0	0	VH24	$VGMA2+(VGMA3-VGMA2) \times 850/1650$
19H	0	1	1	0	0	1	VH25	$VGMA2+(VGMA3-VGMA2) \times 950/1650$
1AH	0	1	1	0	1	0	VH26	$VGMA2+(VGMA3-VGMA2) \times 1050/1650$
1BH	0	1	1	0	1	1	VH27	$VGMA2+(VGMA3-VGMA2) \times 1150/1650$
1CH	0	1	1	1	0	0	VH28	$VGMA2+(VGMA3-VGMA2) \times 1250/1650$
1DH	0	1	1	1	0	1	VH29	$VGMA2+(VGMA3-VGMA2) \times 1350/1650$
1EH	0	1	1	1	1	0	VH30	$VGMA2+(VGMA3-VGMA2) \times 1450/1650$
1FH	0	1	1	1	1	1	VH31	$VGMA2+(VGMA3-VGMA2) \times 1550/1650$

NOTE: VDD2>VGMA1>VGMA2>VGMA3>VGMA4>VGMA5

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
20H	1	0	0	0	0	0	VH32	VGMA3
21H	1	0	0	0	0	1	VH33	$VGMA3+(VGMA4-VGMA3) \times 100/1660$
22H	1	0	0	0	1	0	VH34	$VGMA3+(VGMA4-VGMA3) \times 200/1660$
23H	1	0	0	0	1	1	VH35	$VGMA3+(VGMA4-VGMA3) \times 300/1660$
24H	1	0	0	1	0	0	VH36	$VGMA3+(VGMA4-VGMA3) \times 400/1660$
25H	1	0	0	1	0	1	VH37	$VGMA3+(VGMA4-VGMA3) \times 500/1660$
26H	1	0	0	1	1	0	VH38	$VGMA3+(VGMA4-VGMA3) \times 600/1660$
27H	1	0	0	1	1	1	VH39	$VGMA3+(VGMA4-VGMA3) \times 700/1660$
28H	1	0	1	0	0	0	VH40	$VGMA3+(VGMA4-VGMA3) \times 800/1660$
29H	1	0	1	0	0	1	VH41	$VGMA3+(VGMA4-VGMA3) \times 900/1660$
2AH	1	0	1	0	1	0	VH42	$VGMA3+(VGMA4-VGMA3) \times 1000/1660$
2BH	1	0	1	0	1	1	VH43	$VGMA3+(VGMA4-VGMA3) \times 1100/1660$
2CH	1	0	1	1	0	0	VH44	$VGMA3+(VGMA4-VGMA3) \times 1210/1660$
2DH	1	0	1	1	0	1	VH45	$VGMA3+(VGMA4-VGMA3) \times 1320/1660$
2EH	1	0	1	1	1	0	VH46	$VGMA3+(VGMA4-VGMA3) \times 1430/1660$
2FH	1	0	1	1	1	1	VH47	$VGMA3+(VGMA4-VGMA3) \times 1540/1660$
30H	1	1	0	0	0	0	VH48	VGMA4
31H	1	1	0	0	0	1	VH49	$VGMA4+(VGMA5-VGMA4) \times 120/4120$
32H	1	1	0	0	1	0	VH50	$VGMA4+(VGMA5-VGMA4) \times 240/4120$
33H	1	1	0	0	1	1	VH51	$VGMA4+(VGMA5-VGMA4) \times 370/4120$
34H	1	1	0	1	0	0	VH52	$VGMA4+(VGMA5-VGMA4) \times 500/4120$
35H	1	1	0	1	0	1	VH53	$VGMA4+(VGMA5-VGMA4) \times 640/4120$
36H	1	1	0	1	1	0	VH54	$VGMA4+(VGMA5-VGMA4) \times 780/4120$
37H	1	1	0	1	1	1	VH55	$VGMA4+(VGMA5-VGMA4) \times 930/4120$
38H	1	1	1	0	0	0	VH56	$VGMA4+(VGMA5-VGMA4) \times 1080/4120$
39H	1	1	1	0	0	1	VH57	$VGMA4+(VGMA5-VGMA4) \times 1260/4120$
3AH	1	1	1	0	1	0	VH58	$VGMA4+(VGMA5-VGMA4) \times 1470/4120$
3BH	1	1	1	0	1	1	VH59	$VGMA4+(VGMA5-VGMA4) \times 1720/4120$
3CH	1	1	1	1	0	0	VH60	$VGMA4+(VGMA5-VGMA4) \times 2020/4120$
3DH	1	1	1	1	0	1	VH61	$VGMA4+(VGMA5-VGMA4) \times 2520/4120$
3EH	1	1	1	1	1	0	VH62	$VGMA4+(VGMA5-VGMA4) \times 3220/4120$
3FH	1	1	1	1	1	1	VH63	VGMA5

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
00H	0	0	0	0	0	0	VL0	VGMA10
01H	0	0	0	0	0	1	VL1	$VGMA10+(VGMA9-VGMA10) \times 1800/7080$
02H	0	0	0	0	1	0	VL2	$VGMA10+(VGMA9-VGMA10) \times 2800/7080$
03H	0	0	0	0	1	1	VL3	$VGMA10+(VGMA9-VGMA10) \times 3500/7080$
04H	0	0	0	1	0	0	VL4	$VGMA10+(VGMA9-VGMA10) \times 4100/7080$
05H	0	0	0	1	0	1	VL5	$VGMA10+(VGMA9-VGMA10) \times 4600/7080$
06H	0	0	0	1	1	0	VL6	$VGMA10+(VGMA9-VGMA10) \times 5000/7080$
07H	0	0	0	1	1	1	VL7	$VGMA10+(VGMA9-VGMA10) \times 5400/7080$
08H	0	0	1	0	0	0	VL8	$VGMA10+(VGMA9-VGMA10) \times 5700/7080$
09H	0	0	1	0	0	1	VL9	$VGMA10+(VGMA9-VGMA10) \times 6000/7080$
0AH	0	0	1	0	1	0	VL10	$VGMA10+(VGMA9-VGMA10) \times 6200/7080$
0BH	0	0	1	0	1	1	VL11	$VGMA10+(VGMA9-VGMA10) \times 6400/7080$
0CH	0	0	1	1	0	0	VL12	$VGMA10+(VGMA9-VGMA10) \times 6550/7080$
0DH	0	0	1	1	0	1	VL13	$VGMA10+(VGMA9-VGMA10) \times 6700/7080$
0EH	0	0	1	1	1	0	VL14	$VGMA10+(VGMA9-VGMA10) \times 6830/7080$
0FH	0	0	1	1	1	1	VL15	$VGMA10+(VGMA9-VGMA10) \times 6960/7080$
10H	0	1	0	0	0	0	VL16	VGMA9
11H	0	1	0	0	0	1	VL17	$VGMA9+(VGMA8-VGMA9) \times 120/1650$
12H	0	1	0	0	1	0	VL18	$VGMA9+(VGMA8-VGMA9) \times 230/1650$
13H	0	1	0	0	1	1	VL19	$VGMA9+(VGMA8-VGMA9) \times 340/1650$
14H	0	1	0	1	0	0	VL20	$VGMA9+(VGMA8-VGMA9) \times 450/1650$
15H	0	1	0	1	0	1	VL21	$VGMA9+(VGMA8-VGMA9) \times 550/1650$
16H	0	1	0	1	1	0	VL22	$VGMA9+(VGMA8-VGMA9) \times 650/1650$
17H	0	1	0	1	1	1	VL23	$VGMA9+(VGMA8-VGMA9) \times 750/1650$
18H	0	1	1	0	0	0	VL24	$VGMA9+(VGMA8-VGMA9) \times 850/1650$
19H	0	1	1	0	0	1	VL25	$VGMA9+(VGMA8-VGMA9) \times 950/1650$
1AH	0	1	1	0	1	0	VL26	$VGMA9+(VGMA8-VGMA9) \times 1050/1650$
1BH	0	1	1	0	1	1	VL27	$VGMA9+(VGMA8-VGMA9) \times 1150/1650$
1CH	0	1	1	1	0	0	VL28	$VGMA9+(VGMA8-VGMA9) \times 1250/1650$
1DH	0	1	1	1	0	1	VL29	$VGMA9+(VGMA8-VGMA9) \times 1350/1650$
1EH	0	1	1	1	1	0	VL30	$VGMA9+(VGMA8-VGMA9) \times 1450/1650$
1FH	0	1	1	1	1	1	VL31	$VGMA9+(VGMA8-VGMA9) \times 1550/1650$

NOTE: VGMA6>VGMA7>VGMA8>VGMA9>VGMA10>VSS2

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input Data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output Voltage
20H	1	0	0	0	0	0	VL32	VGMA8
21H	1	0	0	0	0	1	VL33	$VGMA8+(VGMA7-VGMA8) \times 100/1660$
22H	1	0	0	0	1	0	VL34	$VGMA8+(VGMA7-VGMA8) \times 200/1660$
23H	1	0	0	0	1	1	VL35	$VGMA8+(VGMA7-VGMA8) \times 300/1660$
24H	1	0	0	1	0	0	VL36	$VGMA8+(VGMA7-VGMA8) \times 400/1660$
25H	1	0	0	1	0	1	VL37	$VGMA8+(VGMA7-VGMA8) \times 500/1660$
26H	1	0	0	1	1	0	VL38	$VGMA8+(VGMA7-VGMA8) \times 600/1660$
27H	1	0	0	1	1	1	VL39	$VGMA8+(VGMA7-VGMA8) \times 700/1660$
28H	1	0	1	0	0	0	VL40	$VGMA8+(VGMA7-VGMA8) \times 800/1660$
29H	1	0	1	0	0	1	VL41	$VGMA8+(VGMA7-VGMA8) \times 900/1660$
2AH	1	0	1	0	1	0	VL42	$VGMA8+(VGMA7-VGMA8) \times 1000/1660$
2BH	1	0	1	0	1	1	VL43	$VGMA8+(VGMA7-VGMA8) \times 1100/1660$
2CH	1	0	1	1	0	0	VL44	$VGMA8+(VGMA7-VGMA8) \times 1210/1660$
2DH	1	0	1	1	0	1	VL45	$VGMA8+(VGMA7-VGMA8) \times 1320/1660$
2EH	1	0	1	1	1	0	VL46	$VGMA8+(VGMA7-VGMA8) \times 1430/1660$
2FH	1	0	1	1	1	1	VL47	$VGMA8+(VGMA7-VGMA8) \times 1540/1660$
30H	1	1	0	0	0	0	VL48	VGMA7
31H	1	1	0	0	0	1	VL49	$VGMA7+(VGMA6-VGMA7) \times 120/4120$
32H	1	1	0	0	1	0	VL50	$VGMA7+(VGMA6-VGMA7) \times 240/4120$
33H	1	1	0	0	1	1	VL51	$VGMA7+(VGMA6-VGMA7) \times 370/4120$
34H	1	1	0	1	0	0	VL52	$VGMA7+(VGMA6-VGMA7) \times 500/4120$
35H	1	1	0	1	0	1	VL53	$VGMA7+(VGMA6-VGMA7) \times 640/4120$
36H	1	1	0	1	1	0	VL54	$VGMA7+(VGMA6-VGMA7) \times 780/4120$
37H	1	1	0	1	1	1	VL55	$VGMA7+(VGMA6-VGMA7) \times 930/4120$
38H	1	1	1	0	0	0	VL56	$VGMA7+(VGMA6-VGMA7) \times 1080/4120$
39H	1	1	1	0	0	1	VL57	$VGMA7+(VGMA6-VGMA7) \times 1260/4120$
3AH	1	1	1	0	1	0	VL58	$VGMA7+(VGMA6-VGMA7) \times 1470/4120$
3BH	1	1	1	0	1	1	VL59	$VGMA7+(VGMA6-VGMA7) \times 1720/4120$
3CH	1	1	1	1	0	0	VL60	$VGMA7+(VGMA6-VGMA7) \times 2020/4120$
3DH	1	1	1	1	0	1	VL61	$VGMA7+(VGMA6-VGMA7) \times 2520/4120$
3EH	1	1	1	1	1	0	VL62	$VGMA7+(VGMA6-VGMA7) \times 3220/4120$
3FH	1	1	1	1	1	1	VL63	VGMA6

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 4.0	V
Driver supply voltage	VDD2	-0.3 to 13.0	V
Input voltage	VGMA1 to 10	-0.3 to VDD2 + 0.3	V
	TESTI1, TESTI2	-0.3 to VDD2 + 0.3	
	Others	-0.3 to VDD1 + 0.3	
Output voltage	DIO1, DIO2	-0.3 to VDD1 + 0.3	V
	Y1 to Y384	-0.3 to VDD2 + 0.3	
Operating power dissipation	Pd	300	mW
Operation temperature	Top	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	°C

CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 to VGMA10

Turn off power order: VGMA1 to VGMA10 → VDD2 → control signal input → VDD1

RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = - 20 to 75 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.7	3.0	3.6	V
Driver supply voltage	VDD2	7.0	10.0	12.0	V
Gamma corrected voltage	VGMA1 to VGMA5	0.5VDD2	-	VDD2 - 0.2	V
	VGMA6 to VGMA10	VSS2+ 0.2	-	0.5VDD2	V
Driver part output voltage	Vyo	VSS2+ 0.2	-	VDD2 - 0.2	V
Maximum clock frequency	fmax	VDD1 = 2.7V		85	MHz
Output load capacitance	CL	-	-	150	pF / PIN

DC CHARACTERISTICS

Table 5 . DC Characteristics
(Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 7.0 to 12.0 V, VSS1 = VSS2 = 0)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK1, POL, DATPOL, DIO1 (DIO2)	0.7VDD1	-	VDD1	V
Low level input voltage	VIL		VSS1	-	0.3VDD1	
Input leakage current	IL1		- 1	-	1	μA
TEST1 input leak current	IL2	TEST1(TESTI2)	- 1	-	1	
High level output voltage	VOH	DIO1(DIO2), IO = - 1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1(DIO2), IO = + 1.0 mA	-	-	0.5	
Resistance between gamma voltage	R0 to R62	Refer to Table 1. Resistor Strings	Rn × 0.7	-	Rn × 1.3	Ω
Driver output current	IVOH1	VDD2 = 10.0 V, Vx ⁽¹⁾ = 5.0 V, Vyo ⁽²⁾ = 9.0 V	-	- 0.8	- 0.4	mA
	IVOL1	VDD2 = 10.0 V, Vx = 5.0 V, Vyo = 1.0 V	0.4	0.8	-	
Output swing voltage difference deviation	DVrms ⁽³⁾	VDD2 = 10.0V Vyo = 1.5 V ~ 8.5 V	-	± 3	± 10	mV
		VDD2 = 10.0V Vyo = 0.2 V ~ 1.5 V Vyo = 8.5 V ~ 9.8 V	-	-	± 30	
Output pin voltage difference deviation	Dvo	VDD2 = 10.0V Vyo = 1.5 V ~ 8.5 V	-	± 20	± 30	
		VDD2 = 10.0V Vyo = 0.2 V ~ 1.5 V Vyo = 8.5 V ~ 9.8 V	-	± 30	-	
Output average voltage	AVo	VDD2 = 10.0V Dxx = 20H (32 G/S)	-	-	± 7	mV
Output voltage range	Vyo	Input data: 00H to 3FH	VSS2 + 0.2	-	VDD2 - 0.2	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V (4)	-	-	6	mA
Driver part dynamic current	IDD2	VDD2 = 10.0V Load condition 120pF ⁽⁵⁾⁽⁶⁾	-	-	25	
	IDD3	VDD2 = 10.0V No load condition ⁽⁵⁾⁽⁷⁾	-	-	15	

- NOTES:**
1. Vx is the voltage applied to analog output pins Y1 to Y384.
 2. Vyo is the output voltage of analog output pins Y1 to Y384.
 3. dVrms = max. deviation of (VHx-VLx)
VHx; the x gray level positive polarity driver output voltage
VLx; the x gray level negative polarity driver output voltage

4. CLK1 period = 20.68 μ s raster cycle at fCLKP = 65 MHz, input data pattern = 1010....., (checkerboard pattern) alternating data pattern per CLKP, Ta = 25 °C.
5. CLK1 period = 20.68 μ s raster cycle at fCLKP = 65 MHz, input data 00H fixed, alternating POL per raster cycle and VGMA1 = VDD2-0.2V, VGMA10 = VSS2 + 0.2V fixed, Ta = 25 °C.
6. Yout load condition : 120pF(tester load). Refer to Figure 4.
7. Yout load condition : No load(Yout open). Refer to Figure 4.

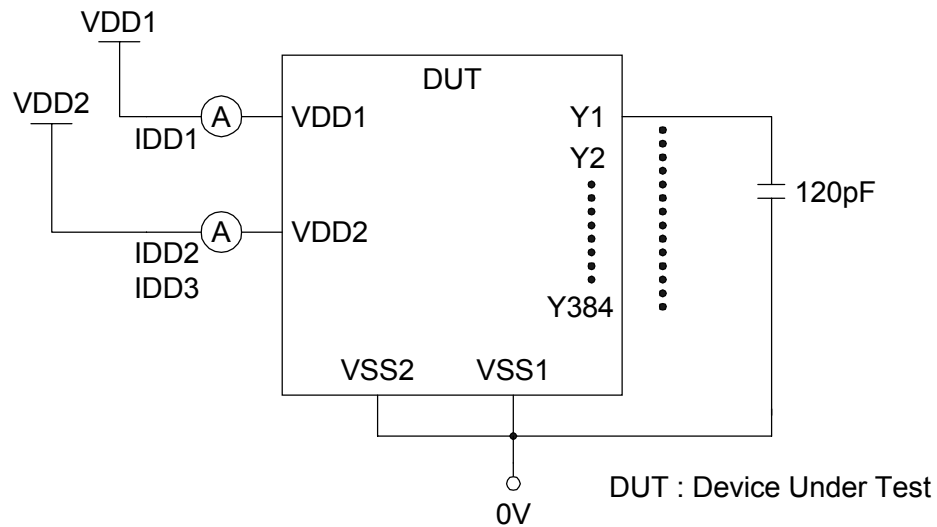


Figure 4. Yout Load Condition(IDD2&3)

RSDS CHARACTERISTICS

Table 6 . RSDS Characteristics
($T_a = -20$ to 75 °C, $V_{DD1} = 2.7$ to 3.6 V, $V_{DD2} = 7.0$ to 12.0 V, $V_{SS1} = V_{SS2} = 0$)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RSDS high input voltage	VIHRSDS	$V_{CMRSDS} = +1.1$ V ⁽¹⁾	100	200	-	mV
RSDS low input voltage	VILRSDS	$V_{CMRSDS} = +1.1$ V ⁽¹⁾	-	-200	-100	
RSDS common mode input voltage range	V_{CMRSDS}	$V_{IHRSDS} = +100$ mV $V_{ILRSDS} = -100$ mV ⁽²⁾	0.9	-	1.3	V
RSDS input leakage current	IDL	DxxP, DxxN, CLKP, CLKN	-10	-	10	μ A

NOTES:

- $V_{CMRSDS} = (V_{CLKP} + V_{CLKN})/2$ or $V_{CMRSDS} = (V_{DxxP} + V_{DxxN})/2$
- The positive sign means that DxxP (or CLKP) is higher than RSDS ground DxxN (or CLKN).
The negative sign means that DxxP (or CLKP) is lower than RSDS ground DxxN (or CLKN).

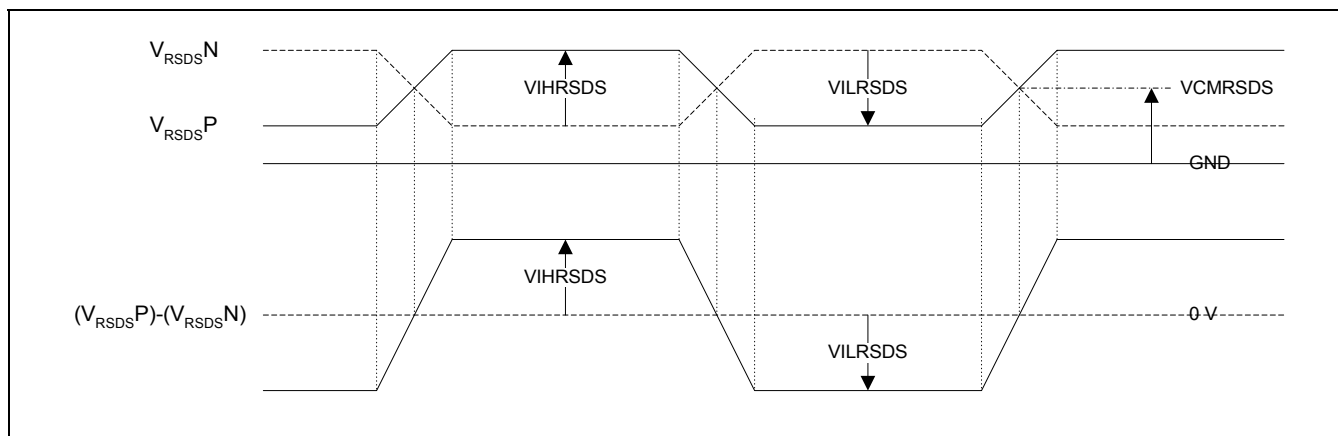


Figure 5. RSDS signal definition

AC CHARACTERISTICS

Table 7. AC Characteristics
($T_a = -20$ to 75 °C, $V_{DD1} = 2.7$ to 3.6 V, $V_{DD2} = 7.0$ to 12.0 V, $V_{SS1} = V_{SS2} = 0$ V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	-	11.7	-	-	ns
Clock pulse low period	PWCLK(L)	-	4	-	-	
Clock pulse high period	PWCLK(H)	-	4	-	-	
Data setup time	t _{SETUP1}	(1)	2	-	-	
Data hold time	t _{HOLD1}	(1)	0	-	-	
Start pulse setup time	t _{SETUP2}	(1)	4	-	-	
Start pulse hold time	t _{HOLD2}	(1)	2	-	-	
Start pulse delay time	t _{PLH1}	CL = 15pF	-	-	7.7	
DIO signal pulse width	PWDIO	-	1CLKP	-	2CLKP	CLKP period
CLK1 setup time	t _{SETUP3}	-	2CLKP	-	-	
CLK1 high pulse width	PWCLK1	-	5CLKP	-	-	
Driver output delay time1	t _{PHL1}	(2) (4)	-	-	6	μs
Driver output delay time2	t _{PHL2}	(3) (4)	-	-	10	
Last data timing	t _{LDT}	-	1CLKP	-	-	CLKP period
CLK1-CLKP time	t _{CLK1-CLKP}	CLK1 ↑ → CLKP ↓	4	-	-	ns
POL-CLK1 time	t _{POL-CLK1}	POL ↑ or ↓ → CLK1 ↑	14	-	-	
CLK1-POL time	t _{CLK1-POL}	CLK1 ↓ → POL ↑ or ↓	10	-	-	

NOTES:

- (1). $V_{CMRSDS} = +1.1V$, $V_{DIFFRSDS} = V_{RSDSP} - V_{RSDSN} = \pm 200mV$
- (2). The value is specified when the drive voltage value reaches the target output voltage level of 90%
- (3). The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
- (4). Yout load condition (refer to Figure 6)

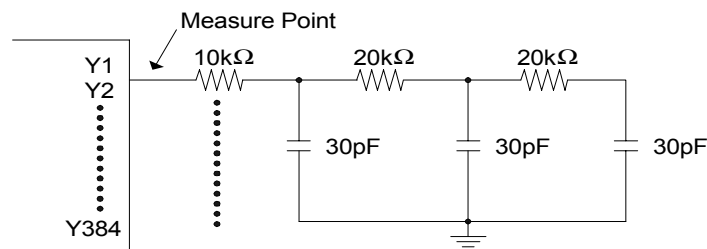


Figure 6. Yout load condition

WAVEFORMS

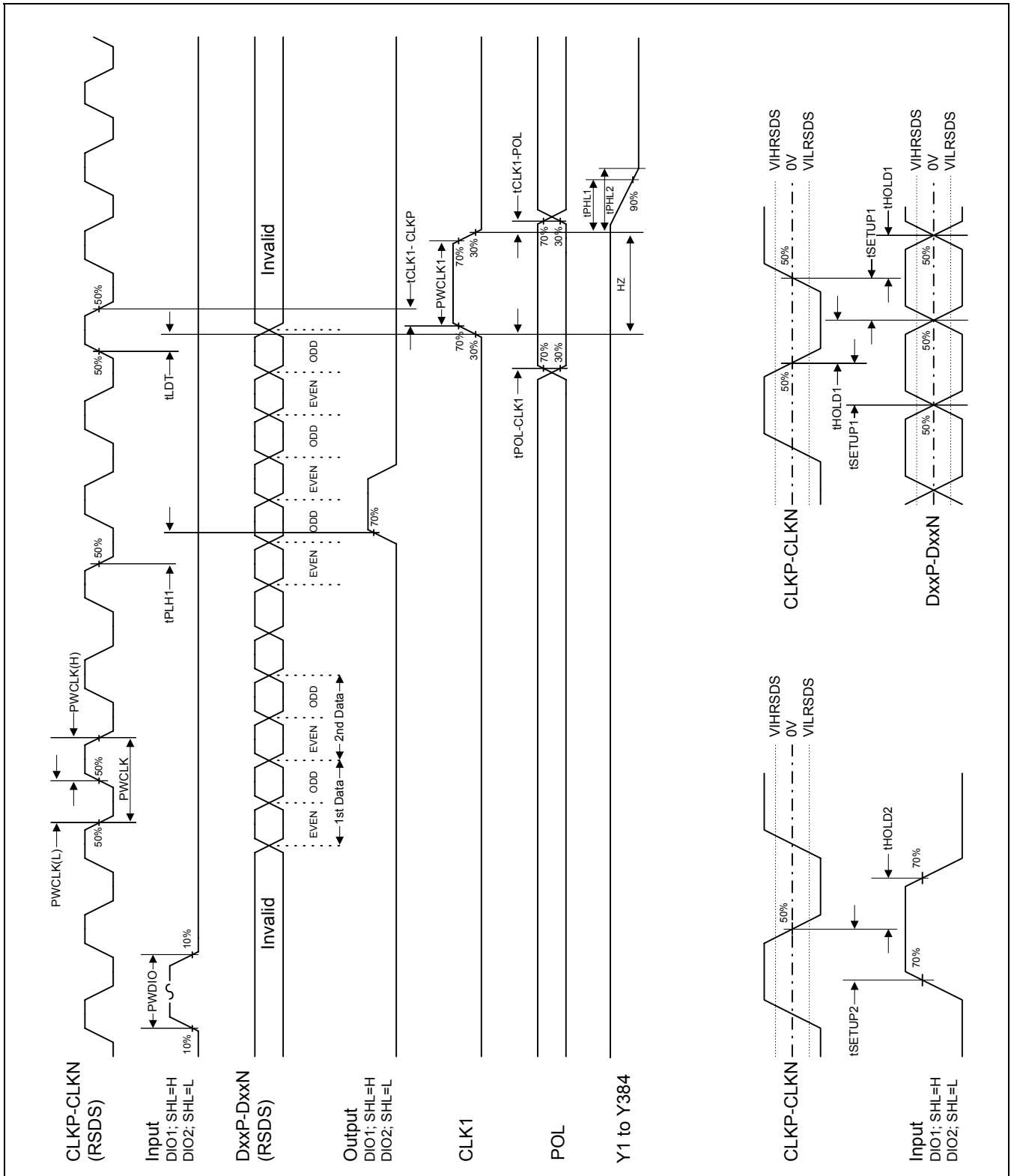


Figure 7. Waveforms

RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD

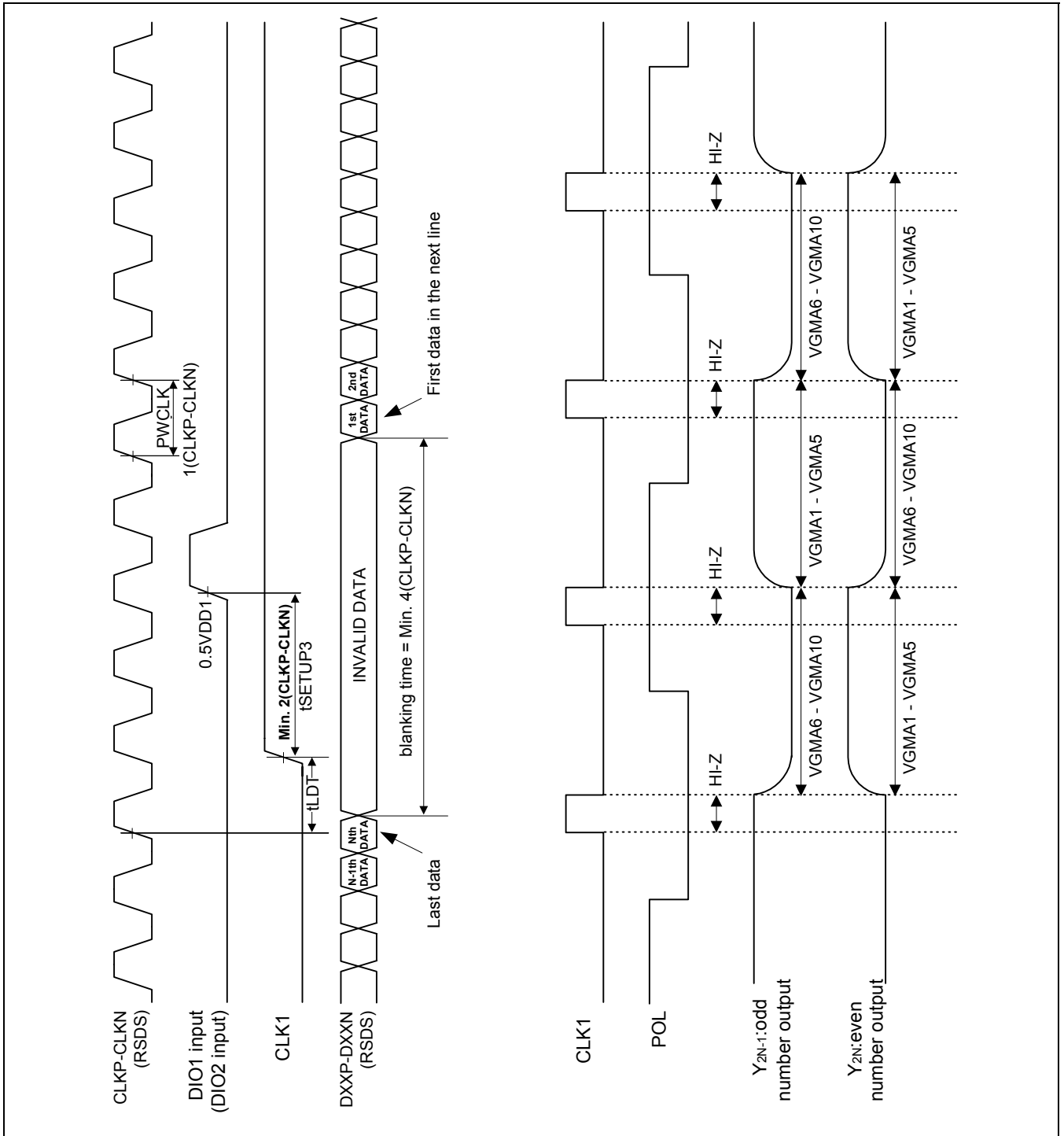


Figure 8. Waveforms

RSDS DATA TIMING DIAGRAM

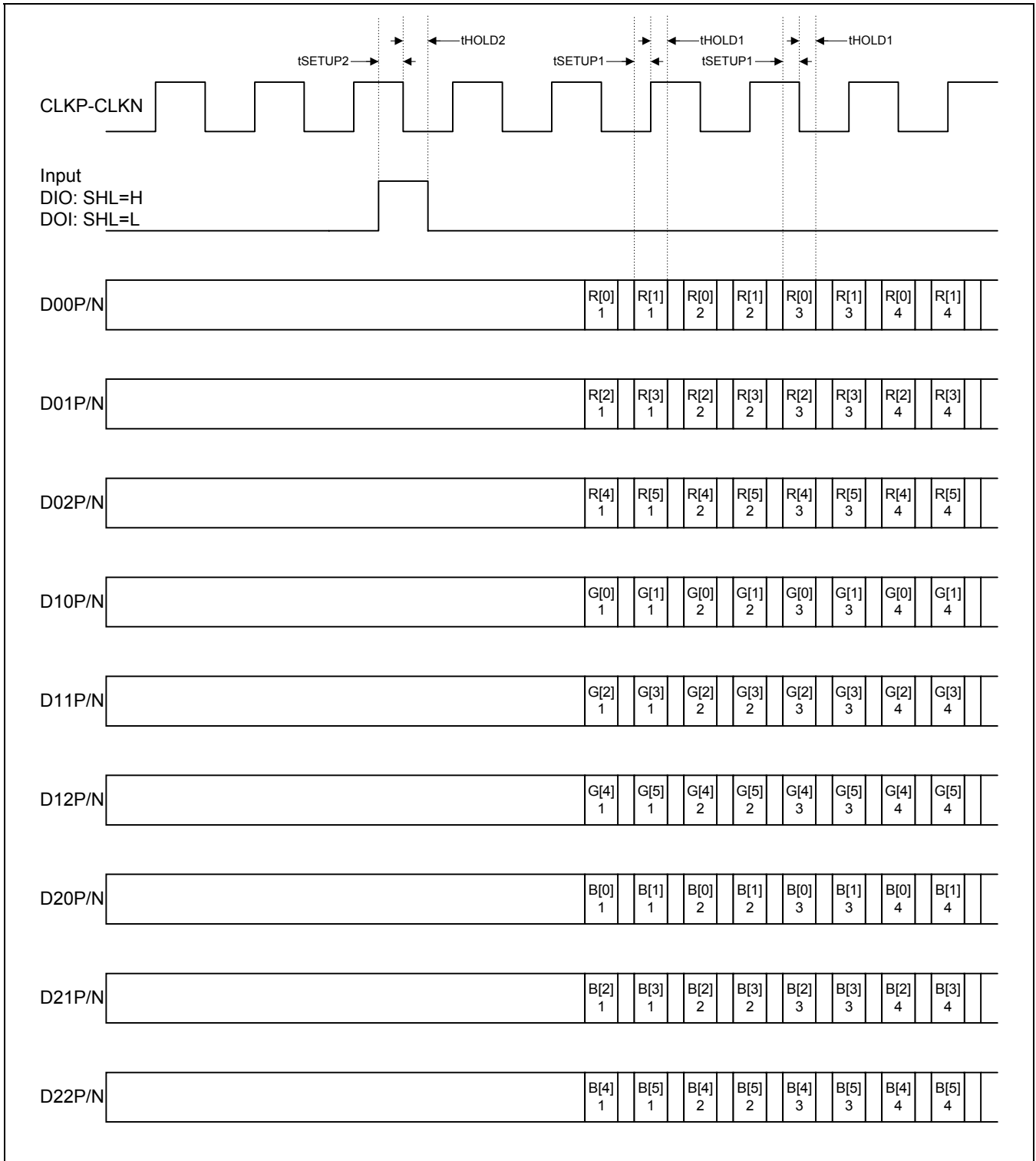


Figure 9. RSDS Data Timing Diagram