SSI 32R515R
9, 10-Channel Ferrite/MIG Read/Write Device

Preliminary Data

1

July, 1990

DESCRIPTION

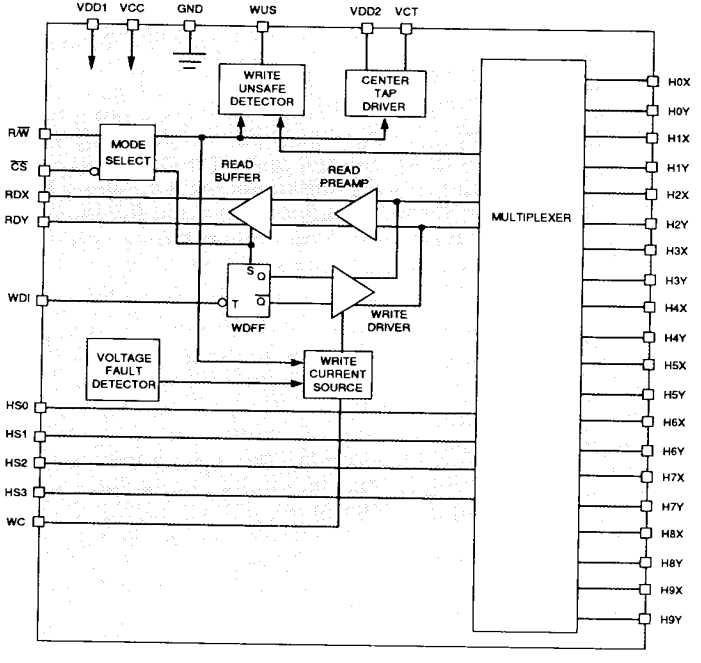
The SSI 32R515R is a bipolar monolithic integrated circuit designed for use with center-tapped ferrite or MIG recording heads. It provides a low noise read path, write current control, and data protection circuitry for as many as 10 channels. The SSI 32R515R requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R515R includes internal damping resistors. The SSI 32R515RM is functionally equivalent to the SSI 32R515R however, it has the mirror image pin arrangement to simplify layout when using multiple devices.

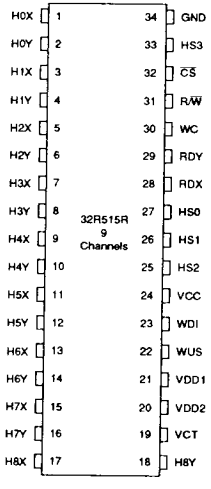
FEATURES

- **High Performance**
  - **Read Mode Gain = 100V/V**
  - **Input Noise = 1.5 nV/$\sqrt{Hz}$ max.**
  - **Input Capacitance = 20 pF**
  - **Write Current Range = 10 mA to 50 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Designed for center-tapped ferrite or MIG heads**
- **Programmable write current source**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Mirror image package option**

BLOCK DIAGRAM



PIN DIAGRAM



34-LEAD SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R515 gives the user the ability to address up to 10 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	X	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

0 = Low level 1 = High level

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R515 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in read mode
- Device not selected
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 96Ω x 50/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R515 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0-HS3	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables device
R/$\overline{W}$	I	Read/Write: a high level selects read mode
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition
WDI	I	Write Data In: negative transition toggles direction of head current
H0X-H9X H0Y-H9Y	I/O	X,Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal out
WC	*	Write Current: used to set the magnitude of the write current
VCT	-	Voltage Center Tap: voltage source for head center tap
VCC	-	+5V
VDD1	-	+12V
VDD2	-	Positive power supply for the center tap voltage source
GND	-	Ground

* When more than one Read/Write device is used, these signals can be wire OR'ed.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (All voltages referenced to GND. Currents into device are positive.)

PARAMETER		VALUE	UNITS
DC Supply Voltage	VDD1	-0.3 to +14	VDC
DC Supply Voltage	VDD2	-0.3 to +14	VDC
DC Supply Voltage	VCC	-0.3 to +6	VDC
Digital Input Voltage Range	VIN	-0.3 to VCC + 0.3	VDC
Head Port Voltage Range	VH	-0.3 to VDD1 + 0.3	VDC
WUS Pin Voltage Range	Vwus	-0.3 to +14	VDC
Write Current Zero Peak	Iw	60	mA
Output Current	RDX, RD Io	-10	mA
Output Current	IVCT	-60	mA
Output Current	Iwus	+12	mA
Storage Temperature Range	Tstg	-65 to 150	°C
Package Temperature PLCC, SO (20 sec Reflow)		215	°C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VDD1		10.8	12.0	13.2	VDC
DC Supply Voltage	VCC		4.5	5.0	5.5	VDC
Head Inductance	Lh		3		15	µH
RCT Resistor	RCT*	Iw = 50 mA	91	96	101	Ω
Write Current	IW		10		80	mA
Junction Temperature Range	Tj		+25		+135	°C
*For Iw = 50 mA. At other Iw levels refer to Applications Information that follows this specification.						

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Supply Current	Read/Idle Mode			35	mA
	Write Mode			30	mA
VDD Supply Current	Idle Mode			20	mA
(sum of VDD1 and VDD2)	Read Mode			35	mA
	Write Mode			20 + Iw	mA
Power Dissipation (Tj = +125°C)	Idle Mode			400	mW
	Read Mode			600	mW
	Write Mode, Iw = 50 mA, RCT = 0Ω			900	mW
	Write Mode, IW = 50 mA RCT = 96Ω			660	mW

DC CHARACTERISTICS (Continued)

DIGITAL I/O

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIL	Input Low Voltage				0.8	VDC
VIH	Input High Voltage		2.0		VCC + 0.3	VDC
IIL	Input Low Current	VIL = 0.8V	-0.4			mA
IIH	Input High Current	VIH = 2.0V			100	µA
VOL	WUS Output Low Voltage	IOL = 8 mA			0.5	VDC
IOH	WUS Output High Current	VOH = 5.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage VCT	Write Mode		6.0		VDC
Head Current (per side)	Write Mode, 0 ≤ VCC ≤ 3.7V, 0 ≤ VDD1 ≤ 8.7V	-200		200	µA
Write Current Range		10		50	mA
Write Current Constant "K"		2.375		2.625	
Iwc to Head Current Gain			0.99		mA/mA
Unselected Head Leakage Current				100	µA
RDX, RDY Output Offset Voltage	Write/Idle Mode	-20		+20	mV
RDX, RDY Common Mode Output Voltage	Write/Idle Mode		5.3		VDC
RDX, RDY Leakage	RDX, RDY = 6V Write/Idle Mode	-100		100	µA

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage	Read Mode	3.0	4.0	5.0	VDC
Head Current (per side)	Read or Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤ 13.2V	-200		200	µA
Input Bias Current (differential)				100	µA
Input Offset Voltage	Read Mode	-4		+4	mV
Common Mode Output Voltage	Read Mode	4.5		6.5	VDC

DYNAMIC CHARACTERISTICS AND TIMING

Unless otherwise specified, recommended operating conditions apply and Iw = 35 mA, Lh = 10 µH, Rd = 750Ω 32R515 only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		7.0			V(pk)
Unselected Head Transient Current				.5	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance		458	610	763	Ω
WDI Transition Frequency	WUS = low Iw = 35 mA LH = 4-10 µH	250			kHz
	WUS = low Iw = 20 mA LH = 4 µH	400			kHz

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain	Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 kΩ	85		115	V/V
Dynamic Range	DC Input Voltage, Vi, Where Gain Falls by 10%. Vin = Vi + 0.5 mVpp @ 300 kHz	-3		+3	mV
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			1.5	nV/√Hz
Differential Input Capacitance	f = 5 MHz			20	pF
Differential Input Resistance	f = 5 MHz	373		735	Ω
Common Mode Rejection Ratio	Vcm = VCT + 100 mVpp @ 5 MHz	50			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VDD1, VDD2 or VCC	45			dB
Channel Separation	Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp	45			dB
Single Ended Output Resistance	f = 5 MHz			30	Ω
Output Current	AC Coupled Load, RDX to RDY	±2.1			mA

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$ To Write	Delay to 90% of Write Current			1.0	µs
R/$\overline{W}$ to Read	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current			1.0	µs
$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope			1.0	µs
$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current			1.0	µs
HS0 - HS3 to any head	Delay to 90% of 100 mV, 10 MHz Read Signal Envelope			600	ns
WUS-Safe to Unsafe - TD1	Iw = 35 mA, LH = 4-10 µH	1.6		8	µs
	Iw = 20 mA, LH = 4 µH	1.0		5.0	µs
WUS-Unsafe to Safe - TD2	Iw = 35 mA			1.0	µs
Head Current (Lh = 0 µH, Rh = 0Ω)					
Prop. Delay - TD3	From 50% Points			25	ns
Asymmetry	WDI has 50% Duty Cycle and 1ns Rise/Fall Time			2	ns
Rise/Fall Time	10% - 90% Points			20	ns

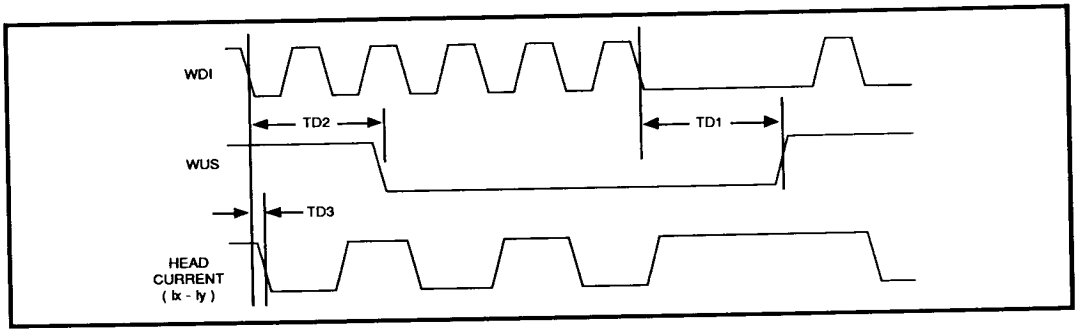
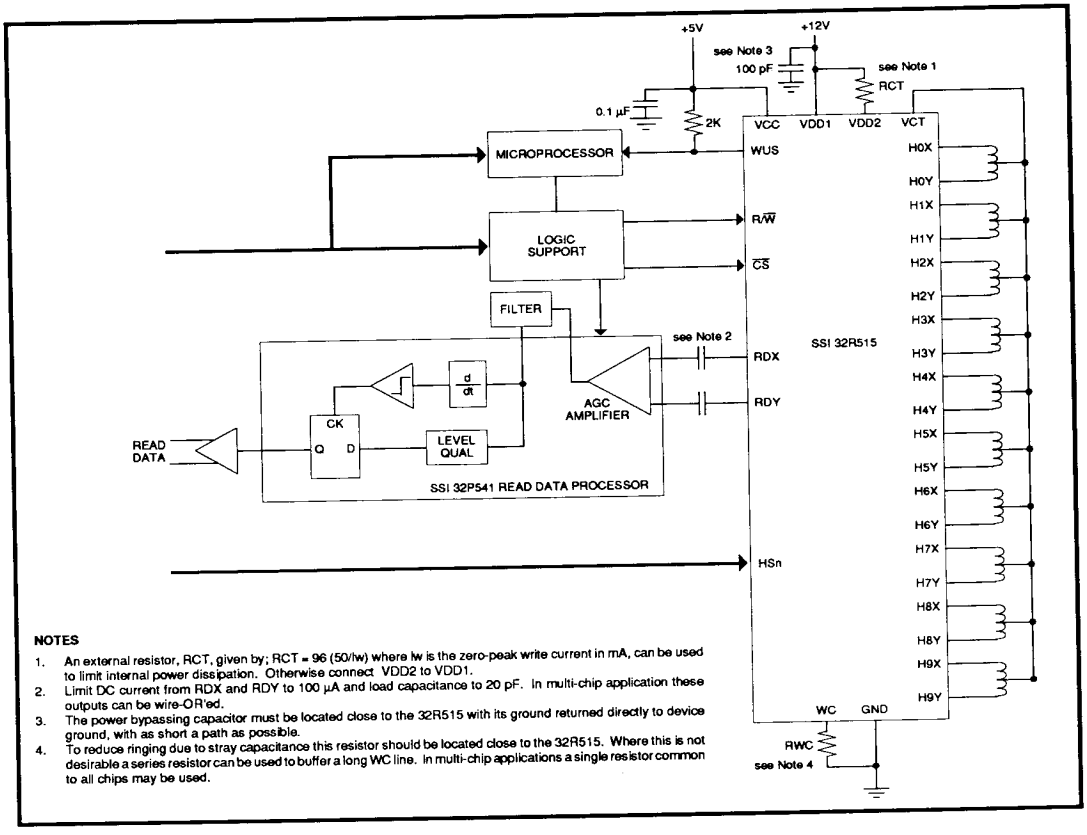


FIGURE 1: Write Mode Timing Diagram

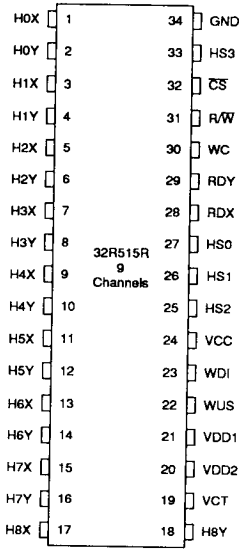


NOTES

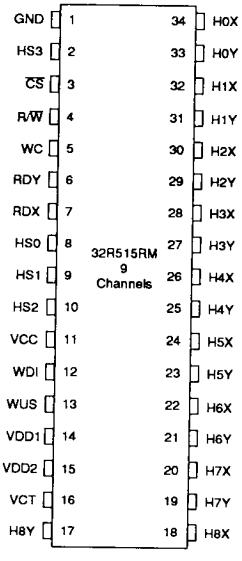
1. An external resistor, RCT, given by; RCT = 96 (50/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
3. The power bypassing capacitor must be located close to the 32R515 with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the 32R515. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

FIGURE 2: Applications Information

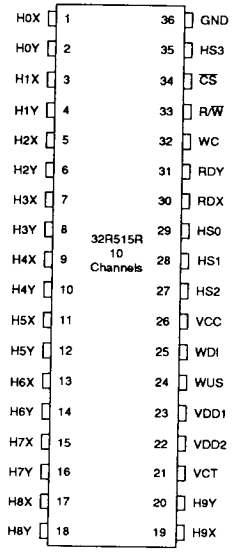
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



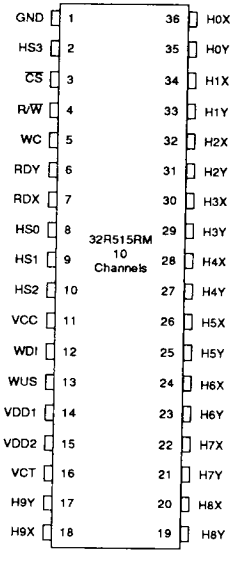
34-Lead SOL



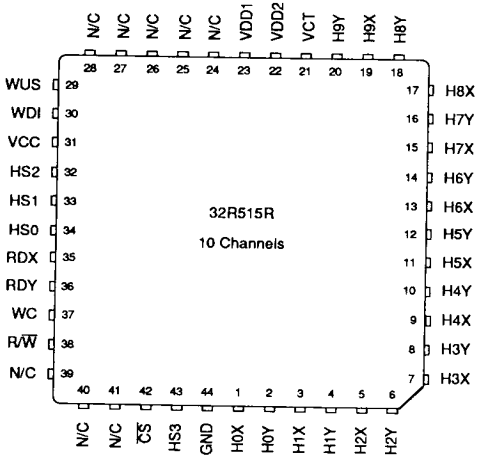
34-Lead SOL Mirror Image



36-Lead SOM



36-Lead SOM Mirror Image



44-Lead PLCC

THERMAL CHARACTERISTICS: Ø ja

34-Lead	SOL	50°C/W
36-Lead	SOM	50°C/W
44-Lead	PLCC	60°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32R515R		
9-Channel SOL	SSI 32R515R-9CL	32R515R-9CL
10-Channel PLCC	SSI 32R515R-10CH	32R515R-10CH
10-Channel SOM	SSI 32R515R-10CM	32R515R-10CM
SSI 32R515RM		
9-Channel SOL	SSI 32R515RM-9CL	32R515RM-10CL
10-Channel SOM	SSI 32R515RM-10CM	32R515RM-10CM

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457