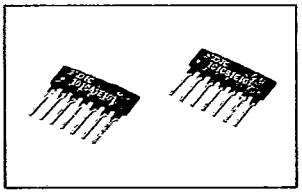
DELAY LINE MODULES

The delay line modules of FDK are the lumped constant elements consisting of low loss ferrite cores of original materials and laminated ceramic chip capacitors with a superb temperature coefficient. A fast rise and a low distortion rate are realized in these modules through a combination of electromagnetic and winding technologies deriving from many years of experience. In total conformity with the MIL-STD-202E, the modules ensure a high level of reliability. Active delay line modules containing TTL logic elements are also available, and FDK designs and supplies a wide selection of delay line modules in response to customer's specific requirements.

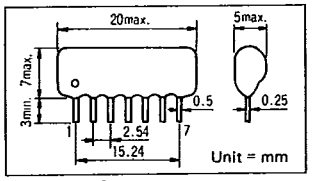
●PASSIVE DELAY LINE C-61 SERIES (7pin-SIP type)

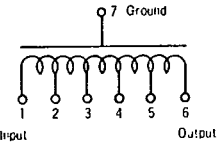


Features
- Capable of high-density mounting through ultra small, ultra thin single in-line structure
- Output 5 taps
- Low price

General specifications
Operating temperature : 0°C~+70°C
Storage temperature : −30°C~+100°C
Wave distortion : ±10% max.
Temperature coefficient : 150PPM/°C
Withstand voltage : DC 50V
Insulation resistance : 100MΩ @DC50V

Model name coding
101 C61 E 101
- Characteristic impedance (100Ω = 10×10¹ = 101)
- No. of taps
- Shape
- Dealy time (50ns.=500, 100ns.=101)

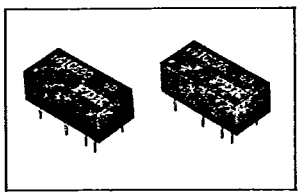
Shape and dimensions


Pin location


Electrical characteristics

Model name	200C61E101	250C61E101	500C61E101	101C61E101	151C61E101	201C61E101	251C61E101	200C61E201	250C61E201	500C61E201	101C61E201	151C61E201	201C61E201	200C61E301	250C61E301	500C61E301	101C61E301
Total delay time Td(ns.) ±5%	20 ± 2.0	25 ± 3.0	50 ± 3.0	100	150	200	250	20 ± 2.0	25 ± 3.0	50 ± 3.0	100	150	200	20 ± 2.0	25 ± 3.0	50 ± 3.0	100
Delay time between taps(ns.)	4 ± 1.5	5 ± 1.5	10 ± 2.0	20 ± 3.0	30 ± 3.0	40 ± 3.0	50 ± 3.0	4 ± 1.5	5 ± 1.5	10 ± 2.0	20 ± 3.0	30 ± 3.0	40 ± 3.0	4 ± 1.5	5 ± 1.5	10 ± 2.0	20 ± 3.0
Rise time Tr(ns.)max.	7.5	9.0	17.0	34.0	52.5	65.0	90.0	7.5	9.0	17.0	34.0	52.5	65.0	7.5	9.0	17.0	34.0
Charecteristic impedance Zo(Ω) ±10%	100	100	100	100	100	100	100	200	200	200	200	200	200	300	300	300	300

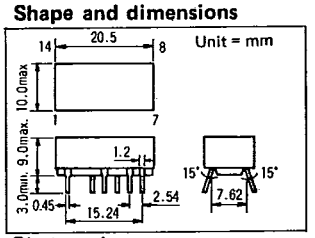
●ACTIVE DELAY LINE C-59 SERIES (14pin-Dip type)

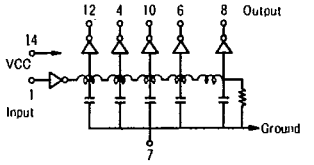


Features
- TTL with built-in IC
- Output 5 taps

General specifications
Operating temperature: 0°C~+70°C
Storage temperature : −55°C~+125°C
Supply voltage : 5V±5%(+7V max.)
Output(Logical:1) : 2.7V min.
Output(Logical:0) : 0.5V max.

Model name coding
101 C59 S
- Built-in IC (S:74S04, LS:74LS04)
- Shape
- Delay time(50ns.=500, 100ns.=101)

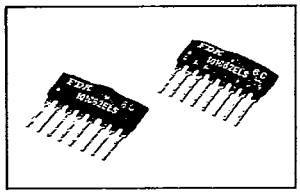
Shape and dimensions


Pin location


Electrical characteristics

Model name	200C59S	250C59S	500C59S	750C59S	101C59S	151C59S	201C59S	251C59S	500C59LS	750C59S	101C59LS	151C59LS	201C59LS	251C59LS
Total delay time Td(ns.) ±5%	20 ± 2.0	25 ± 2.0	50	75 ± 4.0	100	150	200	250	50	75 ± 4.0	100	150	200	250
Delay time between taps(ns.)	4 ± 2.0	5 ± 2.0	10 ± 2.0	15 ± 2.5	20 ± 3.0	30 ± 3.0	40 ± 3.0	50 ± 3.0	10 ± 3.0	15 ± 3.0	20 ± 3.0	30 ± 4.0	40 ± 4.0	50 ± 5.0
Rise time Tr(ns.)max.	3	3	3	3	3	3	3	3	4	4	4	4	4	4
Builit-in IC	74S04	74S04	74S04	74S04	74S04	74S04	74S04	74S04	74LS04	74LS04	74LS04	74LS04	74LS04	74LS04

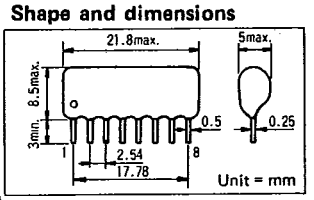
●ACTIVE DELAY LINE C-62 SERIES (8pin-SIP type)

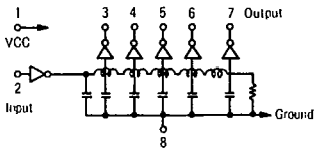


Features
- TTL with bult-in IC
- Capable of high-density mounting through ultra small, ultra thin single-line structure
- Output 5 taps
- Low price

General specifications
Operating temperature: 0°C~+70°C
Storage temperature : −30°C~+100°C
Supply voltage : 5V±5%(+7V max.)
Output(Logical:1) : 2.7V min.
Output(Logical:0) : 0.5V max.

Model name coding
101 C62 E S
- Built-in IC (S:74S04, LS:74LS04)
- No. of taps
- Shape
- Delay time (50ns.=500, 100ns.=101)

Shape and dimensions


Pin location


Electrical characteristics

Model name	200C62ES	250C62ES	500C62ES	750C62ES	101C62ES	151C62ES	201C62ES	251C62ES	500C62ELS	101C62ELS	151C62ELS	201C62ELS	251C62ELS
Total delay time Td(ns.) ±5%	20 ± 2.0	25 ± 2.0	50	75 ± 4.0	100	150	200	250	50	100	150	200	250
Delay time between taps(ns.)	4 ± 2.0	5 ± 2.0	10 ± 2.0	15 ± 2.5	20 ± 3.0	30 ± 3.0	40 ± 3.0	50 ± 3.0	10 ± 3.0	20 ± 3.0	30 ± 4.0	40 ± 4.0	50 ± 5.0
Rise time Tr(ns.)max.	3	3	3	3	3	3	3	3	4	4	4	4	4
Builit-in IC	74S04	74S04	74S04	74S04	74S04	74S04	74S04	74S04	74LS04	74LS04	74LS04	74LS04	74LS04