

DESCRIPTION

The HYM540A200 is a 2M x 40-bit Fast page mode CMOS DRAM module consisting of twenty HY514400A in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM. The HYM540A200M/LM are Tin-Lead plated and HYM540A200MG/LMG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- Low power dissipation

Max. battery back-up 44.0mW (L-part)

Max. CMOS standby 22.0mW (L-part)

110.0mW

Max. TTL standby 220.0mW

Max. operating

Speed	Power
50	7.26W
60	6.44W
70	5.61W

- Single power supply of 5V $\pm$ 10%

- TTL compatible inputs and outputs

- Fast access time

Speed	tRAC	tCAC	tPC
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	20ns	45ns

- Fast page mode operation

- CAS-before-RAS, RAS-only, Hidden refresh

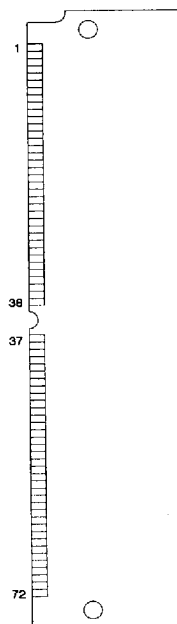
- 1024 refresh cycles / 128ms (L-part)

1024 refresh cycles / 16ms

PIN DESCRIPTION

RAS0, RAS1	Row Address Strobe
CAS0, AS1	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A9	Address Input
DQ0-DQ39	Data Input/Output
PD1-PD4	Presence Detect
VCC	Power (+5V)
VSS	Ground

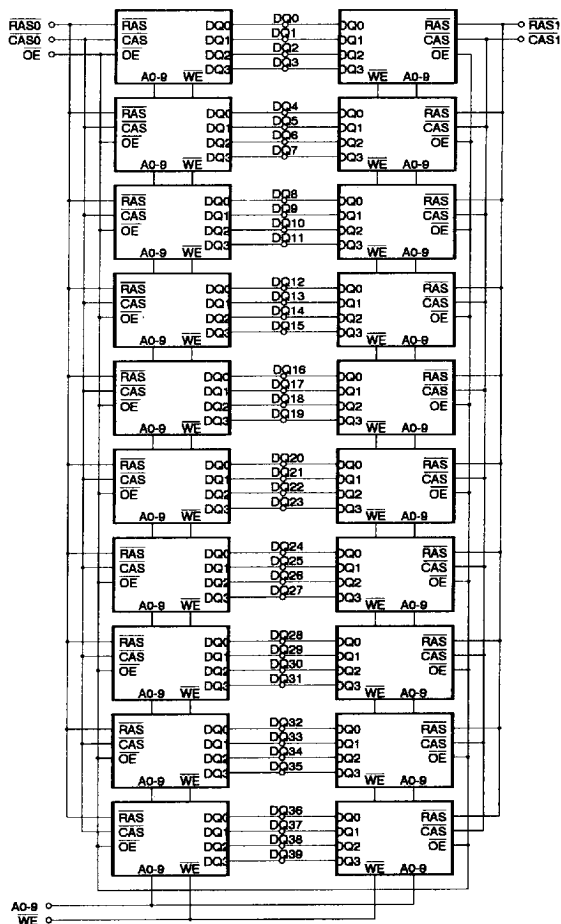
PIN CONNECTION



PIN NAME

#	NAME	#	NAME
1	Vss	37	DQ19
2	DQ0	38	DQ20
3	DQ1	39	Vss
4	DQ2	40	CAS0
5	DQ3	41	NC
6	DQ4	42	NC
7	DQ5	43	CAS1
8	DQ6	44	RAS0
9	DQ7	45	RAS1
10	Vcc	46	DQ21
11	NC	47	WE
12	A0	48	Vss
13	A1	49	DQ22
14	A2	50	DQ23
15	A3	51	DQ24
16	A4	52	DQ25
17	A5	53	DQ26
18	A6	54	DQ27
19	OE	55	DQ28
20	DQ8	56	DQ29
21	DQ9	57	DQ30
22	DQ10	58	DQ31
23	DQ11	59	Vcc
24	DQ12	60	DQ32
25	DQ13	61	DQ33
26	DQ14	62	DQ34
27	DQ15	63	DQ35
28	A7	64	DQ36
29	DQ16	65	DQ37
30	Vcc	66	DQ38
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	NC	70	PD4
35	DQ17	71	DQ39
36	DQ18	72	Vss

BLOCK DIAGRAM



PRESENCE DETECT PINS

PIN	-50	-60	-70
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	Vss	NC	Vss
PD4	Vss	NC	NC

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	18	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I _I	Input Leakage Current (Any Input Pin)	VSS ≤ VIN ≤ VCC + 1.0, All other pins not under test = VSS		-200	200	μA	
I _{LO}	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC, RAS & CAS at VIH		-20	20	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	50 60 70	- - -	1320 1170 1020	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	40	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	50 60 70	- - -	1320 1170 1020	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	50 60 70	- - -	820 720 620	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V	L-part	- -	20 4	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	trc = trc (min.)	50 60 70	- - -	1320 1170 1020	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	trc = 125μs, CAS = CBR cycling or 0.2V OE & WE = VCC - 0.2V A0-A9 = VCC - 0.2V or 0.2V DQ0-DQ39 = VCC - 0.2V, 0.2V, or open	trAS ≤ 300ns	-	6	mA	1,4,5
			trAS ≤ 1μs	-	8		
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = VIL and CAS = VIH.
4. Only trAS(max.) = 1μs is applied to refresh of battery backup but trAS(max.) = 10μs is applied to normal functional operation.
5. ICC5(max.) = 4mA and ICC7 are applied to L-part only (HYM540A200LM and HYM540A200LMG).

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM540A200M/LM/MG/LMG						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	130	-	150	-	180	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	75	-	80	-	95	-	ns	
5	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	15	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	RAS Hold Time	15	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	CAS Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	15	35	20	45	20	50	ns	9
19	tRAD	RAS to Column Address Delay Time	10	25	15	30	15	35	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	5	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	45	-	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	30	-	35	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	40	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	40	-	50	-	55	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	
		L-part	-	128	-	128	-	128		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

(continued)

#	SYMBOL	PARAMETER	HYM540A200M/LM/MG/LMG						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	35	-	35	-	40	-	ns	8
42	tRWD	RAS to WE Delay Time	70	-	80	-	95	-	ns	8
43	tAWD	Column Address to WE Delay Time	45	-	50	-	60	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	25	-	30	-	35	-	ns	
48	tROH	RAS Hold Time Referenced to OE	10	-	10	-	10	20	ns	
49	tOEA	OE Access Time	-	15	-	15	-	20	ns	
50	tOED	OE to Data Delay	15	-	15	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	20	ns	5
52	tOEH	OE Command Hold Time	15	-	15	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	55	-	60	-	70	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	40	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY514400A data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $t_{REF}(\text{max.}) = 128\text{ms}$ is applied to L-part only (HYM540A200LM and HYM540A200LMG).

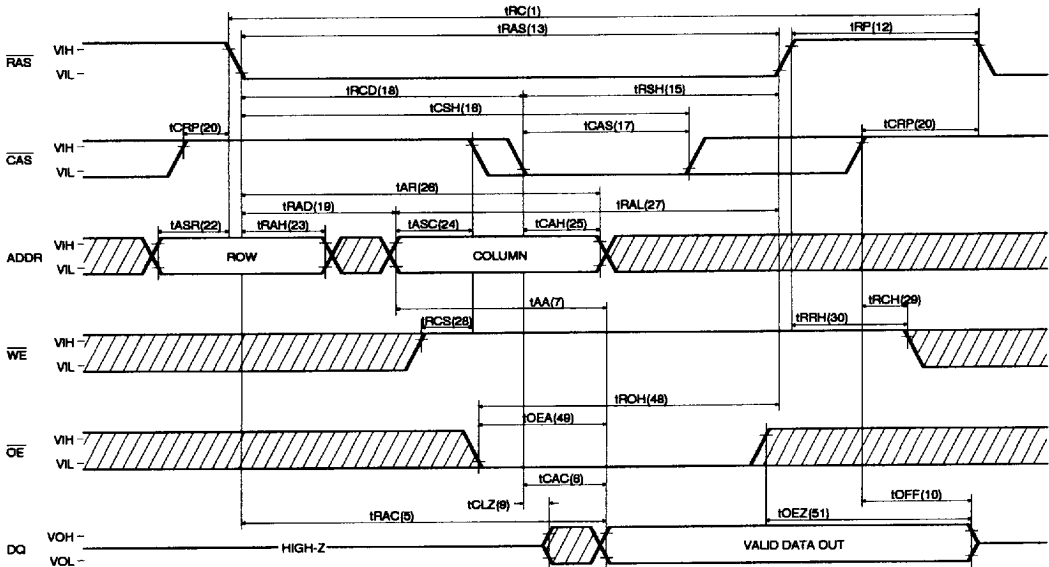
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $f = 1\text{MHz}$, unless otherwise noted.)

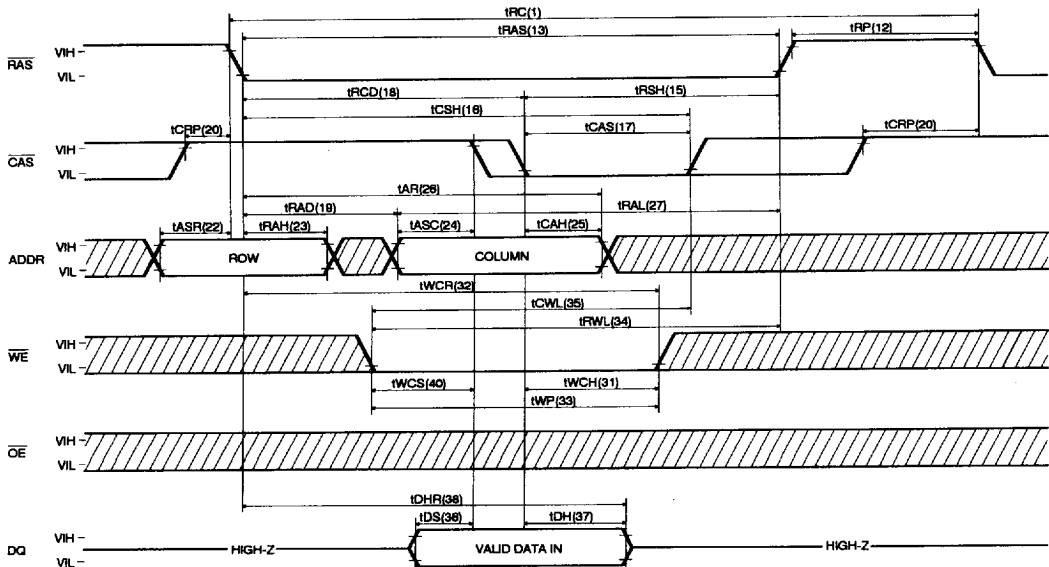
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	126	pF
CIN2	Input Capacitance (WE, OE)	-	130	pF
CIN3	Input Capacitance (RAS0, RAS1, CAS0, CAS1)	-	60	pF
CDO	Data Input/Output Capacitance (DQ0-DQ39)	-	29	pF

TIMING DIAGRAM

READ CYCLE



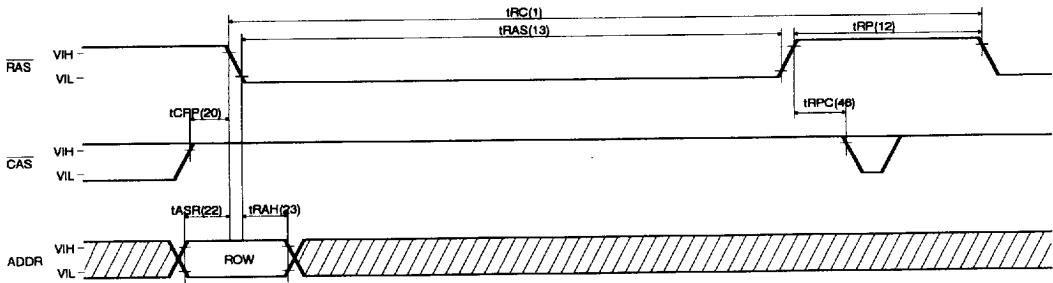
EARLY WRITE CYCLE



The timing diagram illustrates the relationship between the RAS, CAS, ADDR, WE, OE, and DQ signals. The signals are shown as digital waveforms, and the timing parameters are indicated by arrows and labels. The parameters are as follows:

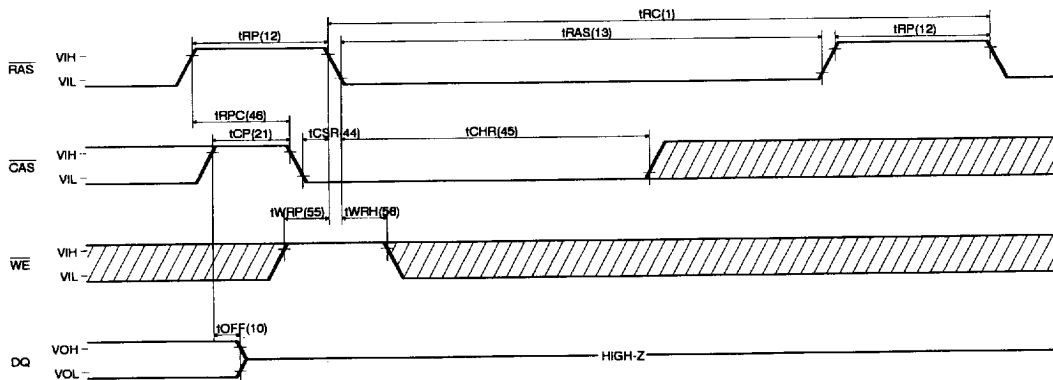
- RAS:** $t_{RASP}(14)$ (RAS Access Period), $t_{RCP}(12)$ (RAS to CAS Delay), $t_{RCHP}(54)$ (RAS to CAS Hold Period), $t_{RSH}(19)$ (RAS to CAS Setup Time), $t_{RCP}(20)$ (RAS to CAS Delay), $t_{RCHP}(54)$ (RAS to CAS Hold Period), $t_{RSH}(19)$ (RAS to CAS Setup Time).
- CAS:** $t_{CSP}(20)$ (CAS Setup Period), $t_{ICD}(18)$ (CAS to ICAS Delay), $t_{ICAS}(17)$ (CAS to ICAS Delay), $t_{ICP}(21)$ (CAS to ICAS Delay), $t_{ICAS}(17)$ (CAS to ICAS Delay), $t_{ICP}(21)$ (CAS to ICAS Delay), $t_{ICAS}(17)$ (CAS to ICAS Delay), $t_{ICP}(20)$ (CAS to ICAS Delay).
- ADDR:** $t_{ASQ}(22)$ (Address Setup Time), $t_{RAH}(23)$ (Row Address Hold Time), $t_{ASC}(24)$ (Address to Column Delay), $t_{CAH}(25)$ (Column Address Hold Time), $t_{ASC}(24)$ (Address to Column Delay), $t_{CAH}(25)$ (Column Address Hold Time), $t_{ASC}(24)$ (Address to Column Delay), $t_{CAH}(25)$ (Column Address Hold Time), $t_{RAL}(27)$ (Row Address to Column Delay).
- WE:** $t_{WCS}(40)$ (Write Enable Setup Time), $t_{WCH}(31)$ (Write Enable Hold Time), $t_{WCP}(33)$ (Write Enable to Column Delay), $t_{WCR}(32)$ (Write Enable to Column Delay), $t_{OEH}(52)$ (Write Enable to Column Delay), $t_{OEH}(52)$ (Write Enable to Column Delay), $t_{OEH}(52)$ (Write Enable to Column Delay).
- OE:** $t_{OEH}(52)$ (Output Enable Hold Time), $t_{OED}(50)$ (Output Enable Delay), $t_{OED}(50)$ (Output Enable Delay), $t_{OED}(50)$ (Output Enable Delay).
- DQ:** $t_{DHR}(38)$ (Data Hold Time), $t_{DS}(36)$ (Data Setup Time), $t_{DH}(37)$ (Data Hold Time), $t_{DS}(36)$ (Data Setup Time), $t_{DH}(37)$ (Data Hold Time), $t_{DS}(36)$ (Data Setup Time), $t_{DH}(37)$ (Data Hold Time).

RAS-ONLY REFRESH CYCLE



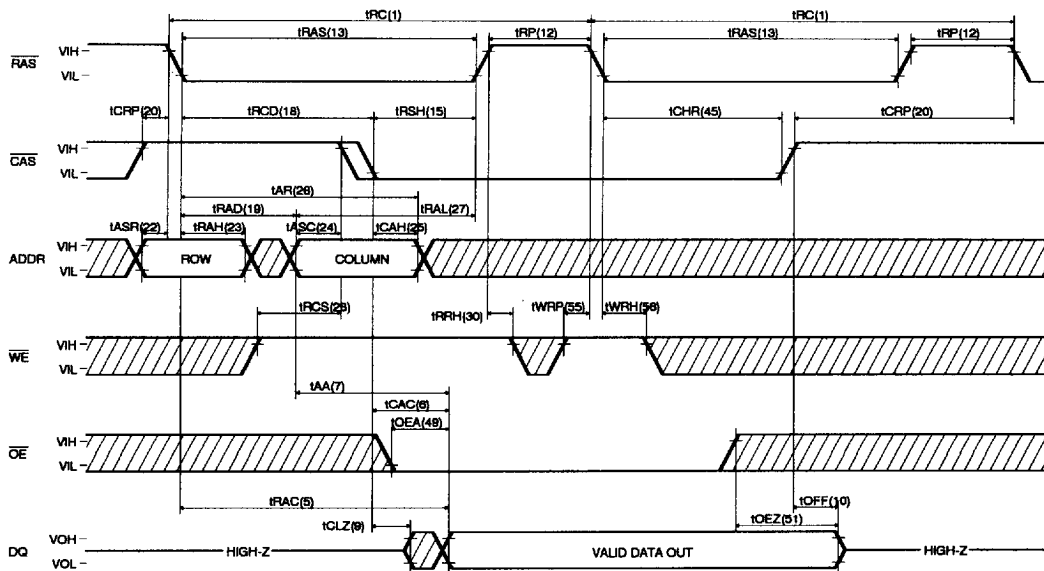
NOTE : WE and OE = "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

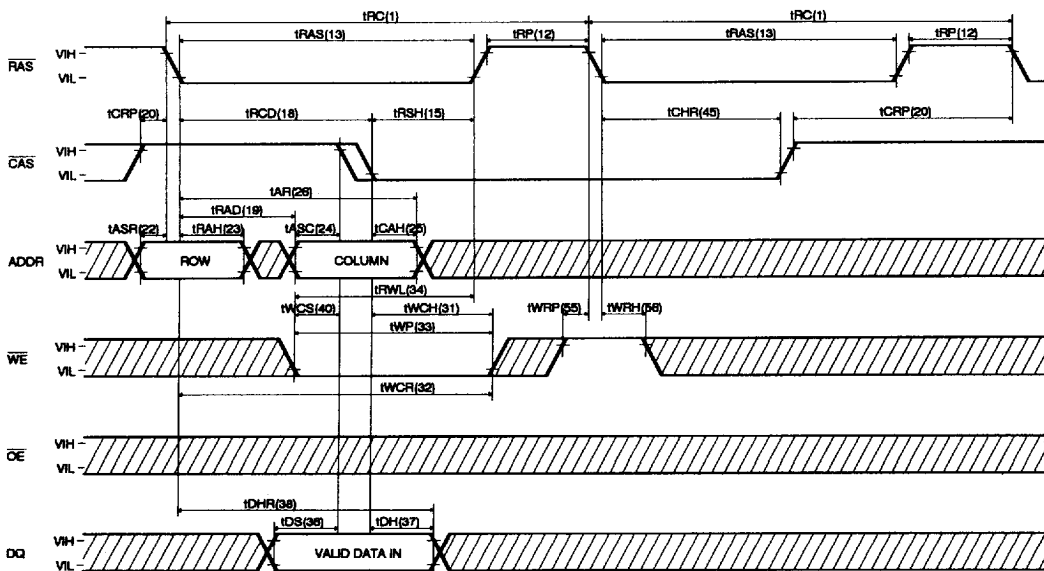


NOTE : ADDR and OE = "H" or "L"

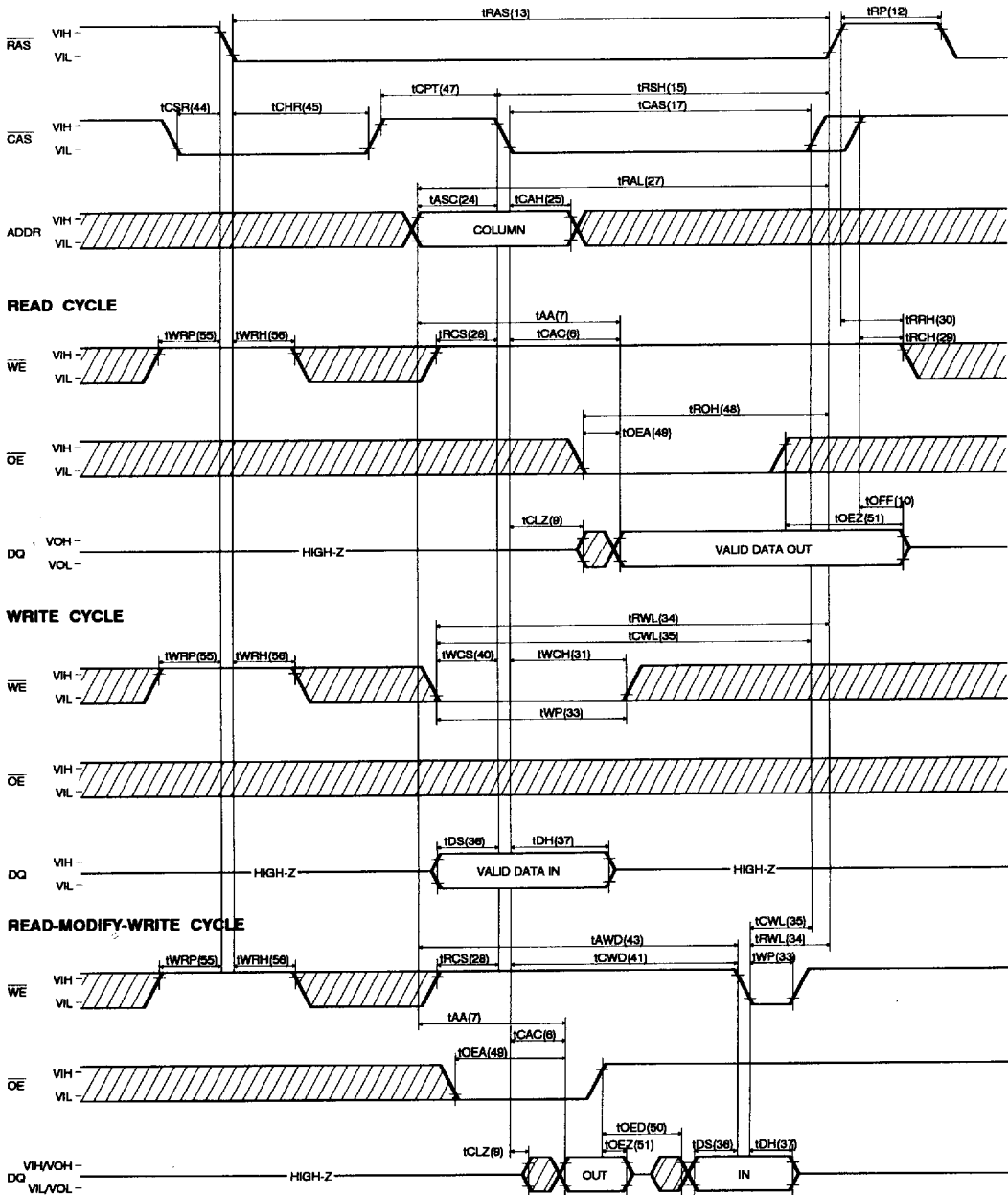
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



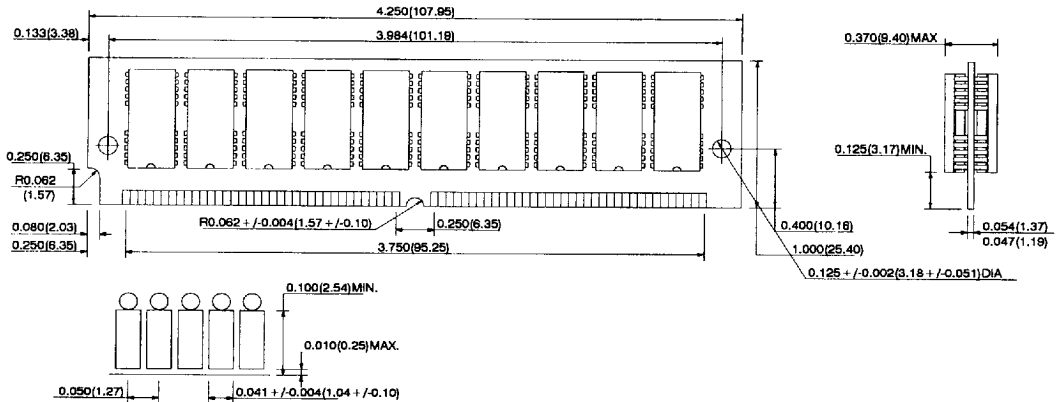
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

72 pin Single In-line Memory Module (M ; Tin-Lead plated, MG ; Gold plated)

UNIT : INCH(mm)
TOLERANCE : +/0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM540A200M	50/60/70		SIMM	Tin-Lead
HYM540A200LM	50/60/70	L-part	SIMM	Tin-Lead
HYM540A200MG	50/60/70		SIMM	Gold
HYM540A200LMG	50/60/70	L-part	SIMM	Gold