Ordering number : EN*5073A

CMOS LSI

# LC99062-W50

## Image Sensor Signal Processing LSI

**Preliminary**

## Overview

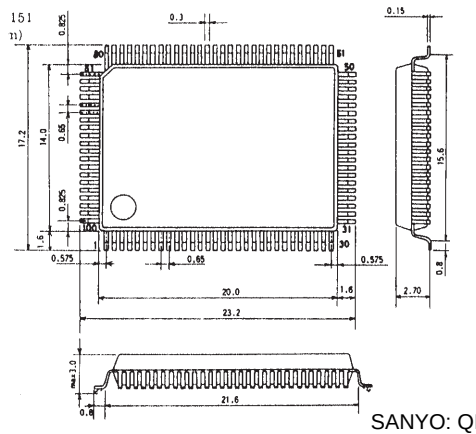
The LC99062-W50 is an external digital signal processor (DSP) that includes digital NTSC and PAL encoders on chip, and that supports color video. The LC99062-W50 is implemented in a single chip using standard cells.

## Package Dimensions

unit: mm

**3151-QFP100E**

[LC99062-W50]



SANYO: QIP100E

## Specifications

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | | –0.3 to +7.0 | V |
| I/O voltages | $V_I$, $V_O$ | | –0.3 to $V_{DD}$ + 0.3 | V |
| Allowable power dissipation | Pd max | | 850 | mW |
| Operating temperature | Topr | | –15 to +65 | °C |
| Storage temperature | Tstg | | –55 to +125 | °C |
| Soldering conditions | | Hand soldering: 3 seconds | 350 | °C |
| | | Reflow: 10 seconds | 235 | °C |
| I/O currents | $I_I$, $I_O$ | Per individual I/O reference cell | ±20 | mA |

### Allowable Operating Ranges at Ta = –15 to +65°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | 4.75 | 5.0 | 5.25 | V |
| Input voltage range | $V_{IN}$ | | 0 | | $V_{DD}$ | V |

## Electrical Characteristics at Ta = –15 to +65°C, $V_{DD}$ = 4.75 to 5.25 V, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high level voltage | $V_{IH}$ | CMOS compatible: applicable pin (1) | 0.7 $V_{DD}$ | | | V |
| Input low level voltage | $V_{IL}$ | CMOS compatible: applicable pin (1) | | | 0.3 $V_{DD}$ | V |
| Input high level voltage | $V_{IH}$ | TTL compatible Schmitt: applicable pin (2) | 2.5 | | | V |
| Input low level voltage | $V_{IL}$ | TTL compatible Schmitt: applicable pin (2) | | | 0.6 | V |
| Output high level voltage | $V_{OH}$ | $I_{OH}$ = –4 mA: applicable pin (3) | $V_{DD}$ – 2.1 | | | V |
| Output low level voltage | $V_{OL}$ | $I_{OL}$ = 4 mA: applicable pin (3) | | | 0.4 | V |
| Output high level voltage | $V_{OH}$ | $I_{OH}$ = –4 mA: applicable pin (4) | $V_{DD}$ – 2.1 | | | V |
| Output low level voltage | $V_{OL}$ | $I_{OL}$ = 4 mA: applicable pin (4) | | | 0.4 | V |
| Input leakage current | $I_L$ | $V_I$ = $V_{SS}$, $V_{DD}$: applicable pins (1) and (2) | –10 | | +10 | µA |
| Output leakage current | $I_{OZ}$ | In high-impedance output mode: applicable pin (3) | –10 | | +10 | µA |

Note: The applicable pin sets are defined as follows:

Input

(1) .....All input pins except REGSEL1 and REGSEL2

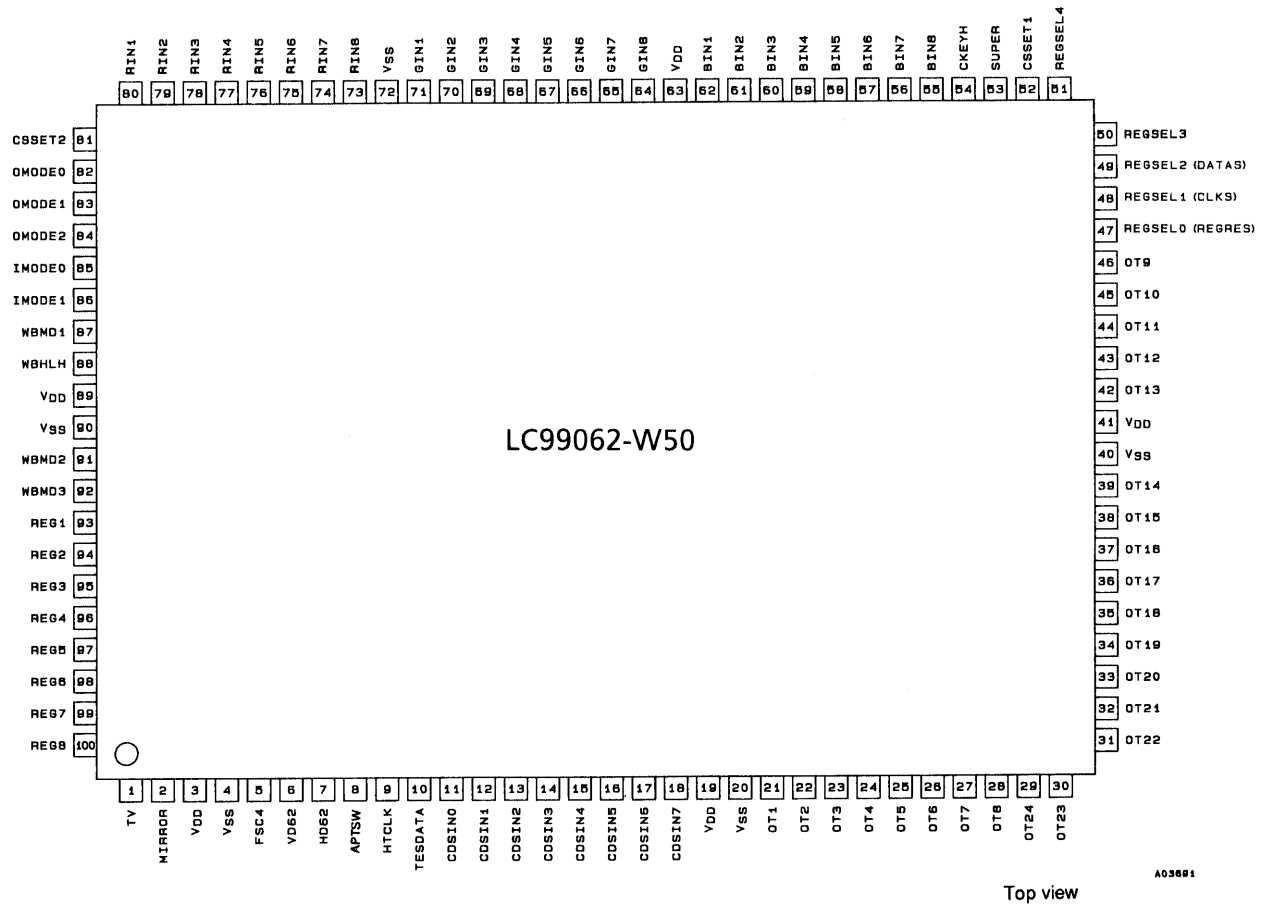
(2) .....REGSEL1, REGSEL2

Output

(3) .....OT1 to OT24

(4) .....CRKEYH

## Pin Assignment




Top view

## Pin Functions

I/O → I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | TV | I | 0: NTSC, 1: PAL |
| 2 | MIRROR | I | 0: Normal, 1: Mirror |
| 3 | $V_{DD}$ | P | |
| 4 | $V_{SS}$ | P | |
| 5 | FSC4 | I | CLK (from LC99052) NTSC: 14.31818 MHz, PAL: 14.1875 MHz |
| 6 | VD62 | I | VD (from LC99052) |
| 7 | HD62 | I | HD (from LC99052) |
| 8 | APTSW | I | Aperture switch 0: Off, 1: On |
| 9 | HTCLK | I | CLK = 8/3fsc (from LC99052) |
| 10 | TESDATA | I | 0: Run |
| 11 | CDSIN0 | I | 8-bit data input (from LC99052) (LSB) |
| 12 | CDSIN1 | I | 8-bit data input (from LC99052) |
| 13 | CDSIN2 | I | 8-bit data input (from LC99052) |
| 14 | CDSIN3 | I | 8-bit data input (from LC99052) |
| 15 | CDSIN4 | I | 8-bit data input (from LC99052) |
| 16 | CDSIN5 | I | 8-bit data input (from LC99052) |
| 17 | CDSIN6 | I | 8-bit data input (from LC99052) |
| 18 | CDSIN7 | I | 8-bit data input (from LC99052) (MSB) |
| 19 | $V_{DD}$ | P | |
| 20 | $V_{SS}$ | P | |
| 21 | OT1 | O | Output channel1 = CH1 (LSB) |
| 22 | OT2 | O | Output channel1 = CH1 |
| 23 | OT3 | O | Output channel1 = CH1 |
| 24 | OT4 | O | Output channel1 = CH1 |
| 25 | OT5 | O | Output channel1 = CH1 |
| 26 | OT6 | O | Output channel1 = CH1 |
| 27 | OT7 | O | Output channel1 = CH1 |
| 28 | OT8 | O | Output channel1 = CH1 (MSB) |
| 29 | OT24 | O | Output channel3 = CH3 (MSB) |
| 30 | OT23 | O | Output channel3 = CH3 |
| 31 | OT22 | O | Output channel3 = CH3 |
| 32 | OT21 | O | Output channel3 = CH3 |
| 33 | OT20 | O | Output channel3 = CH3 |
| 34 | OT19 | O | Output channel3 = CH3 |
| 35 | OT18 | O | Output channel3 = CH3 |
| 36 | OT17 | O | Output channel3 = CH3 (LSB) |
| 37 | OT16 | O | Output channel2 = CH2 (MSB) |
| 38 | OT15 | O | Output channel2 = CH2 |
| 39 | OT14 | O | Output channel2 = CH2 |
| 40 | $V_{SS}$ | P | |
| 41 | $V_{DD}$ | P | |
| 42 | OT13 | O | Output channel2 = CH2 |
| 43 | OT12 | O | Output channel2 = CH2 |
| 44 | OT11 | O | Output channel2 = CH2 |
| 45 | OT10 | O | Output channel2 = CH2 |
| 46 | OT9 | O | Output channel2 = CH2 (LSB) |
| 47<br>48<br>49<br>50<br>51 | REGSEL0<br>REGSEL1<br>REGSEL2<br>REGSEL3<br>REGSEL4 | I<br>I<br>I<br>I<br>I | (REGRES) 0: Register initialization 1: Register modification allowed<br>(CLKS) Serial clock input<br>(DATAS) Serial data input<br><br>REGSEL [4:0] = (11110) or (11**1); OT (24 to 1) → High impedance |
| 52 | CSSET1 | I | Must be set according to the phase of the LC99052 A/D converter clock. (This is true for pin 81 as well.)<br>Recommended value for current conditions: 1 |
| 53 | SUPER | I | Superimpose pulse input 1; superimpose 0; camera through |
| 54 | CKEYH | O | Chrominance key out H; chrominance key<br>The delay time is changed by the settings of pins 85 and 86. See pins 85 and 86. |

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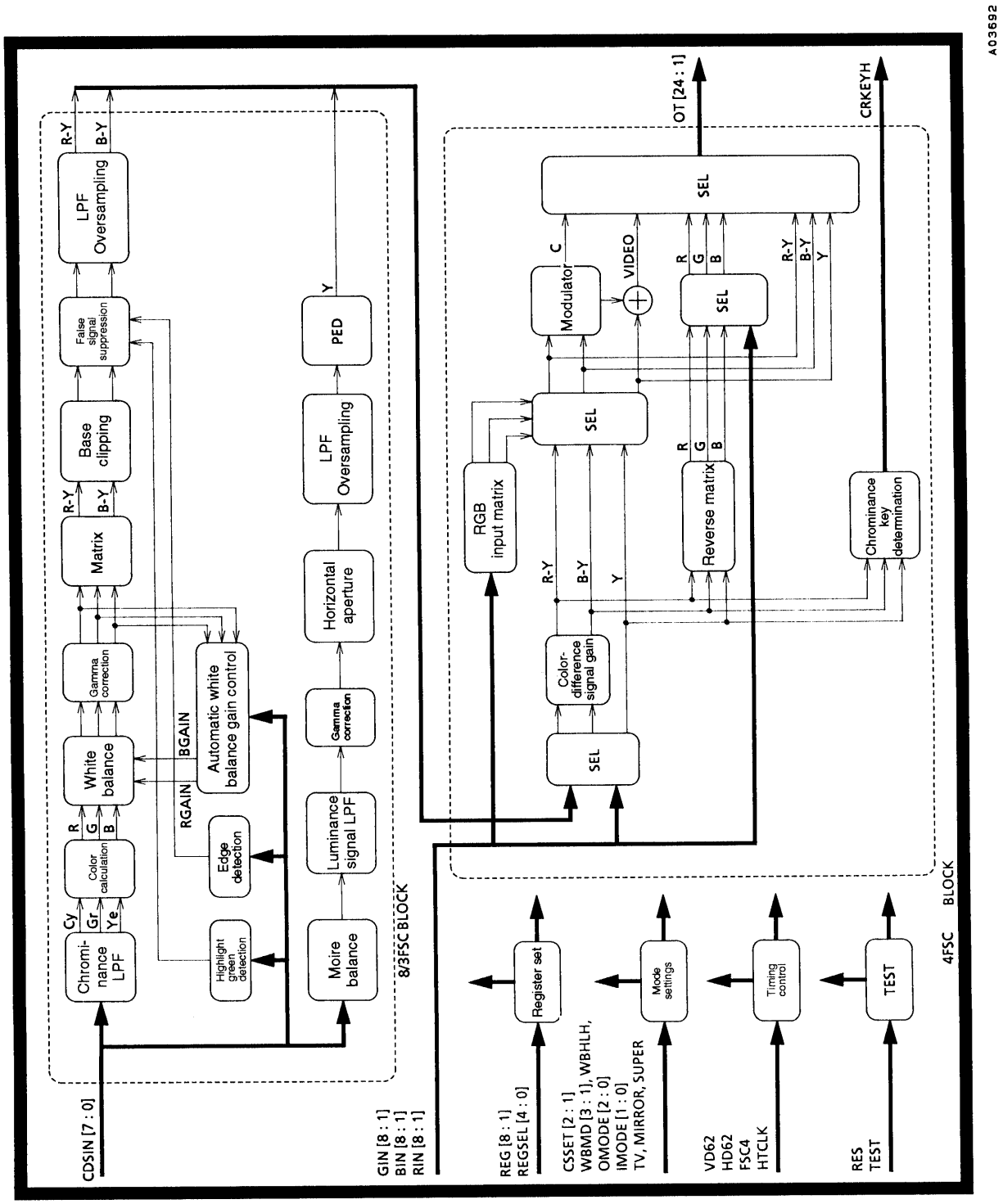
I/O → I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Unconnected pin

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 55 | BIN8 | I | 8-bit data input (MSB) |
| 56 | BIN7 | I | 8-bit data input |
| 57 | BIN6 | I | 8-bit data input |
| 58 | BIN5 | I | 8-bit data input |
| 59 | BIN4 | I | 8-bit data input |
| 60 | BIN3 | I | 8-bit data input or register setting pin |
| 61 | BIN2 | I | 8-bit data input or register setting pin |
| 62 | BIN1 | I | 8-bit data input (LSB) or register setting pin |
| 63 | $V_{DD}$ | P | |
| 64 | GIN8 | I | 8-bit data input (MSB) |
| 65 | GIN7 | I | 8-bit data input |
| 66 | GIN6 | I | 8-bit data input |
| 67 | GIN5 | I | 8-bit data input |
| 68 | GIN4 | I | 8-bit data input |
| 69 | GIN3 | I | 8-bit data input or register setting pin |
| 70 | GIN2 | I | 8-bit data input or register setting pin |
| 71 | GIN1 | I | 8-bit data input (LSB) or register setting pin |
| 72 | $V_{SS}$ | P | |
| 73 | RIN8 | I | 8-bit data input (MSB) |
| 74 | RIN7 | I | 8-bit data input |
| 75 | RIN6 | I | 8-bit data input |
| 76 | RIN5 | I | 8-bit data input |
| 77 | RIN4 | I | 8-bit data input |
| 78 | RIN3 | I | 8-bit data input or register setting pin |
| 79 | RIN2 | I | 8-bit data input or register setting pin |
| 80 | RIN1 | I | 8-bit data input (LSB) or register setting pin |
| 81 | CSSET2 | I | Must be set according to the phase of the LC99052 A/D converter clock. (This is true for pin 52 as well.)<br>Recommended value for current conditions: 1 |
| 82<br>83<br>84 | OMODE0<br>OMODE1<br>OMODE2 | I<br>I<br>I | Output mode select<br>000: Video (OT1 to OT8), ICON (OT24)<br>001: R (OT1 to OT8), G (OT9 to OT16), B (OT17 to OT24)<br>010: R-Y (OT1 to OT8), Y (OT9 to OT16), B-Y (OT17 to OT24)<br>011: Y (OT1 to OT8), C (OT9 to OT16), CSYNC (OT24)<br>100: Y (OT1 to OT8), U/V (OT9 to OT16), UVCONT (OT24)<br>101: VBS (OT1 to OT8), Y (OT12 to OT9), R-Y (OT16, OT15), B-Y (OT14, OT13)<br>110: VBS (OT1 to OT8), Y + CSYNC (OT9 to OT16), C (OT17 to OT24)<br>111: Y/U/V (OT1 to OT8) |
| 85<br>86 | IMODE0<br>IMODE1 | I<br>I | Input mode select<br>00: R (RIN4 to RIN8), G (GIN4 to GIN8), B (BIN4 to BIN8)*1<br>01: R (RIN4 to RIN8), G (GIN4 to GIN8), B (BIN4 to BIN8)*2<br>10: R (RIN1 to RIN8), G (GIN1 to GIN8), B (BIN1 to BIN8)*1<br>11: Y (RIN1 to RIN8), V (GIN1 to GIN8), U (BIN1 to BIN8)*1<br>Note: 1. The output is synchronized with the chrominance key out.<br>2. The chrominance key out is output 16 clock cycles in advance of this output. |
| 87 | WBMD1 | I | White balance mode SW1 |
| 88 | WBHLH | I | Auto white balance hold; 1: Hold, 0: Auto<br>Note: * Hold this pin low when the internal register is used. |
| 89 | $V_{DD}$ | P | |
| 90 | $V_{SS}$ | P | |
| 91 | WBMD2 | I | White balance mode SW2 |
| 92 | WBMD3 | I | White balance mode SW3 |
| 93 | REG1 | I | Register setting pin |
| 94 | REG2 | I | Register setting pin |
| 95 | REG3 | I | Register setting pin |
| 96 | REG4 | I | Register setting pin |
| 97 | REG5 | I | Register setting pin |
| 98 | REG6 | I | Register setting pin |
| 99 | REG7 | I | Register setting pin |
| 100 | REG8 | I | Register setting pin |

## Block Diagram



## Main Functions Provided by the LC99062-W50

DSP Functions for Sanyo Color CCD devices (LC9997G/LC9998G)

1. Luminance signal system processing
   - Includes a luminance matrix to reduce reflected noise (moire).
   - Includes a knee-processing circuit using complementary color filters.
   - Includes a seven-tap low-pass filter.
   - Gamma correction circuit using a five-line approximation technique. The intersection points for each line can be adjusted.
   - Provides second-order horizontal outline correction. The gain and coring are adjustable.
   - Forms a 1.5× sampling frequency conversion circuit.

2. Chrominance system signal processing
   - Includes a digital clamping circuit that prevents black balance slippage.
   - Forms the RGB signal using an 11-tap low-pass filter and a color calculation matrix.
   - Automatic white balance circuit
     — Includes all circuits and functions required for automatic white balance.
     — Allows switching between automatic and manual modes.
     — Allows holding from automatic mode.
     — Supports fine-grained gain settings using 7-bit gain data and a technique that takes valid bits into account. The R gain can be set from ×0.25 to ×4.0, and the B gain from ×0.5 to ×8.0.
     — Provides modes with seven patterns, including flesh correction.
     — Reduces incorrect operation by applying a response with hysteresis according to the degree of the discrepancy.
   - Gamma correction circuit using a three-line approximation technique
   - Includes a linear matrix for color difference signals. Allows color tone adjustment.
   - Includes a color noise suppression circuit that operates for low chrominance level signals. The suppression level is adjustable.
   - Includes a suppression circuit for false color signals that occur at edges and in high-luminance areas.
   - All of the above functions are formed with baseband signals.
   - Includes a 1.5x sampling frequency conversion circuit.

NTSC/PAL Encoder

- NTSC and PAL encoding is possible with only HD, VD, and CLK inputs (NTSC = 14.31818 MHz, PAL = 14.1875 MHz). In PAL mode, internal operations are used to generate the Fsc signal, and normally there is no need for a Fsc signal generated by a PLL or other circuit.
- The CSYNC, CBLK, and BF signals are formed internally.
- Allows burst phase adjustment (hue adjustment). (NTSC only)
- Allows pedestal and burst level adjustment.
- Includes a seven-tap low-pass filter for the color difference signals relative to the external RGB inputs. The luminance system 3.58 MHz trap can be turned on or off.

Input and Output Modes

1. Input modes
   - In addition to signal input from an LC99052-V64A, the LC99062-W50 also supports <R, G, B> and <Y, R–Y, B–Y> input modes.
   - Two of the above input systems can be superimposed.

2. Output modes
   - The LC99062-W50 supports eight output modes.
     — Composite video, 8-bit RGB, <Y, R-Y, B-Y>, <Y, C>, <Y, U/V>, and <4-bit Y, 2-bit R-Y, B-Y>
     — <Y + CSYNC, C> and <Y/U/V>

Other Functions

- Simplified chrominance key function
  — An arbitrary color can be detected by setting R-Y and B-Y data.
- A 2-pin serial interface is used for setting registers.
- Stand-alone operation is possible. The adjustments and settings are supported from external pins even in stand-alone mode.
- Support for mirror (left-right reversal) processing.