

## M390S1620ET1 SDRAM DIMM

16Mx72 SDRAM DIMM with PLL & Register based on 16Mx4, 4Banks 4K Ref., 3.3V Synchronous DRAMs with SPD

### GENERAL DESCRIPTION

The Samsung M390S1620ET1 is a 16M bit x 72 Synchronous Dynamic RAM high density memory module. The Samsung M390S1620ET1 consists of eighteen CMOS 16Mx4 bit Synchronous DRAMs in TSOP-II 400mil packages, three 18-bits Drive ICs for input control signal, one PLL in 24-pin TSSOP package for clock and one 2K EEPROM in 8-pin TSSOP package for Serial Presence Detect on a 168-pin glass-epoxy substrate. Two 0.22uF and one 0.0022uF decoupling capacitors are mounted on the printed circuit board in parallel for each SDRAM. The M390S1620ET1 is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### FEATURE

- Performance range

Part No.	Max Freq. (Speed)
M390S1620ET1-C75	133MHz (7.5ns @ CL=3)

- Burst mode operation
- Auto & self refresh capability (4096 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs  
Latency (Access from column address)  
Burst length (1, 2, 4, 8 & Full page)  
Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- PCB : **Height (1,700mil)**, double sided component

### PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	DQM1	57	DQ18	85	Vss	113	DQM5	141	DQ50
2	DQ0	30	CS0	58	DQ19	86	DQ32	114	*CS1	142	DQ51
3	DQ1	31	DU	59	VDD	87	DQ33	115	RAS	143	VDD
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	VDD	34	A2	62	*VREF	90	VDD	118	A3	146	*VREF
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	VDD	68	Vss	96	Vss	124	VDD	152	Vss
13	DQ9	41	VDD	69	DQ24	97	DQ41	125	*CLK1	153	DQ56
14	DQ10	42	CLK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2	73	VDD	101	DQ45	129	*CS3	157	VDD
18	VDD	46	DQM2	74	DQ28	102	VDD	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	VDD	77	DQ31	105	CB4	133	VDD	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	*CLK2	107	Vss	135	NC	163	*CLK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	**SA0
26	VDD	54	Vss	82	**SDA	110	VDD	138	Vss	166	**SA1
27	WE	55	DQ16	83	**SCL	111	CAS	139	DQ48	167	**SA2
28	DQM0	56	DQ17	84	VDD	112	DQM4	140	DQ49	168	VDD

### PIN NAMES

Pin Name	Function
A0 ~ A11	Address input (Multiplexed)
BA0 ~ BA1	Select bank
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit (Data-in/data-out)
CLK0	Clock input
CKE0	Clock enable input
CS0, CS2	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DQM0 ~ 7	DQM
VDD	Power supply (3.3V)
Vss	Ground
*VREF	Power supply for reference
REGE	Register enable
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
DU	Don't use
NC	No connection

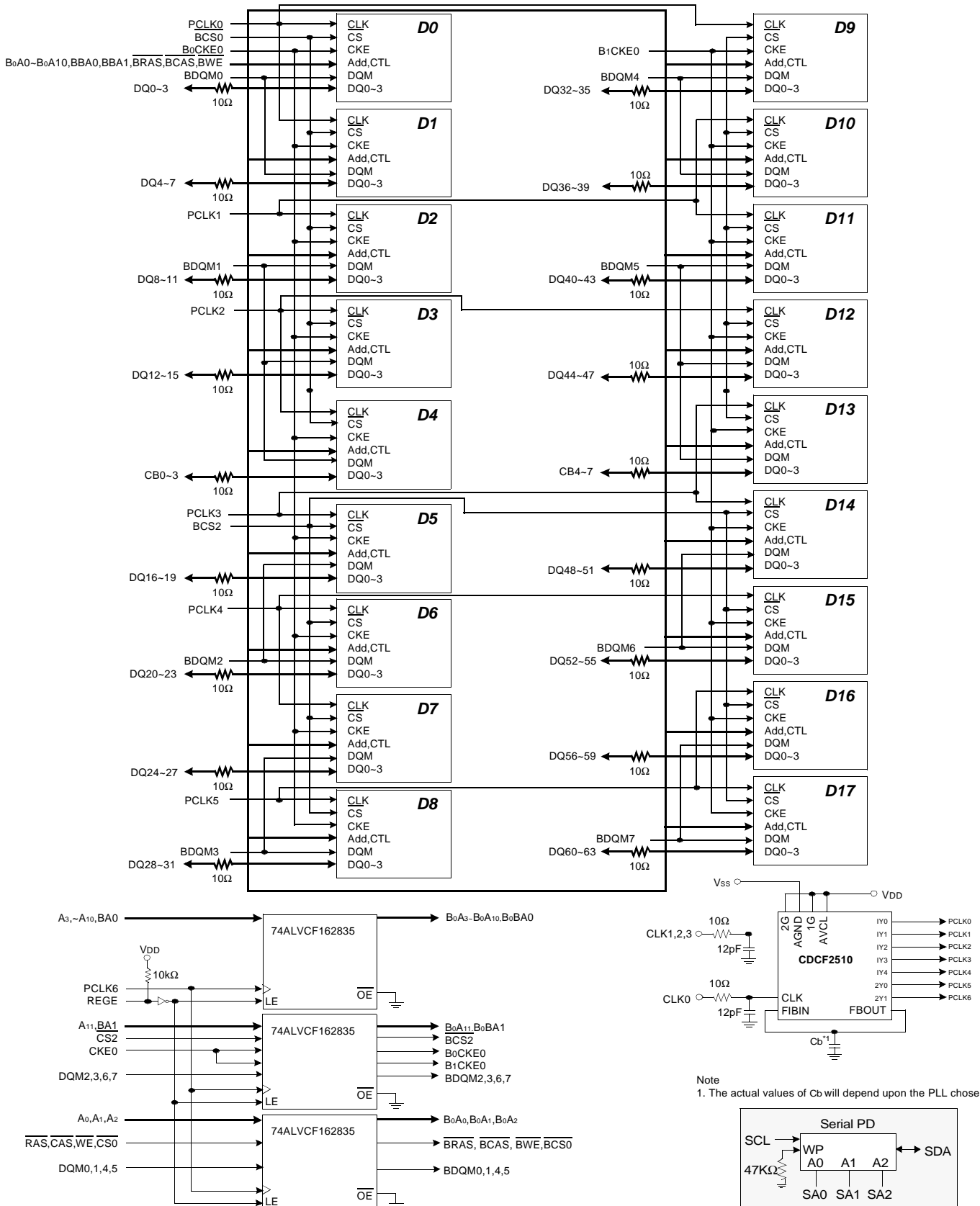
- \* These pins are not used in this module.  
\*\* These pins should be NC in the system which does not support SPD.

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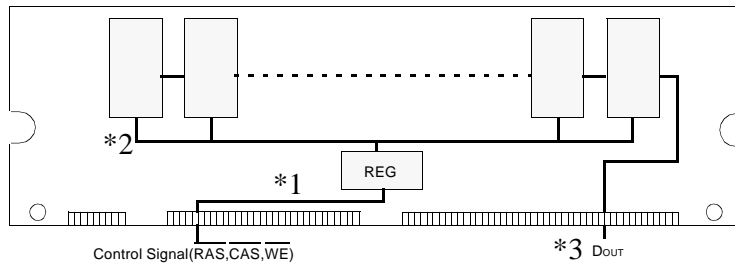
## PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	<i>System clock</i>	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	<i>Chip select</i>	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	<i>Clock enable</i>	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A11	<i>Address</i>	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA11, Column address : CA0 ~ CA9
BA0 ~ BA1	<i>Bank select address</i>	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	<i>Row address strobe</i>	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	<i>Column address strobe</i>	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	<i>Write enable</i>	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ active.
DQM0 ~ 7	<i>Data input/output mask</i>	Makes data output Hi-Z, tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	<i>Register enable</i>	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	<i>Data input/output</i>	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	<i>Check bit</i>	Check bits for ECC.
VDD/VSS	<i>Power supply/ground</i>	Power and ground for the input buffers and the core logic.

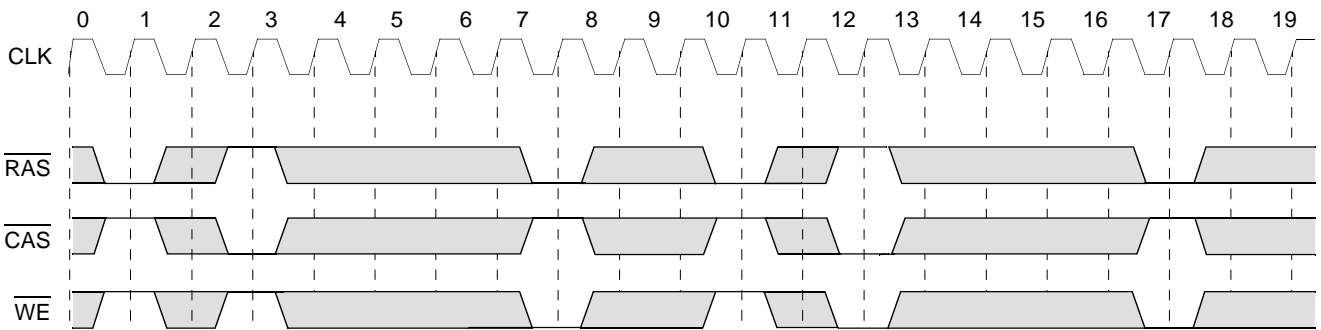
FUNCTIONAL BLOCK DIAGRAM



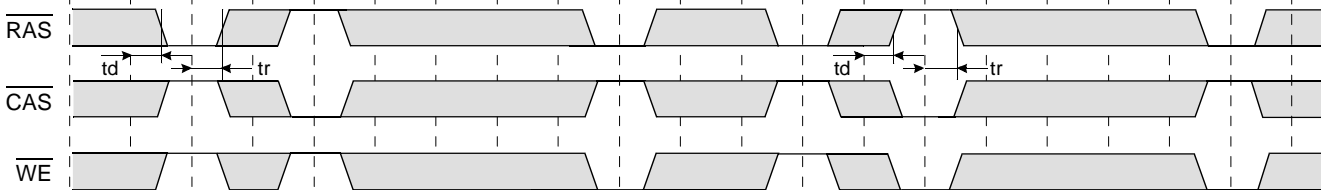
STANDARD TIMING DIAGRAM WITH PLL & REGISTER (CL=2, BL=4)



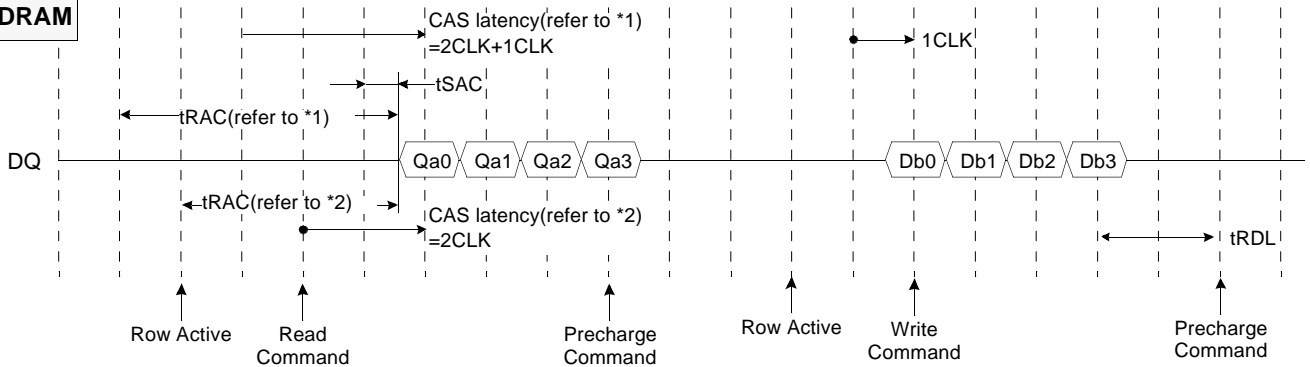
**\*1. Register Input**



**\*2. Register Output**



**\*3. SDRAM**



td, tr = Delay of register (74ALVCF162835)

**Notes :** 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, Input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.  
 2. D<sub>IN</sub> is to be issued 1clock after write command in external timing because D<sub>IN</sub> is issued directly to module.

□ : Don't care

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1.0 ~ 4.6	V
Voltage on V <sub>DD</sub> supply relative to Vss	V <sub>DD</sub> , V <sub>DDQ</sub>	-1.0 ~ 4.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	18	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.  
Functional operation should be restricted to recommended operating condition.  
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V <sub>DD</sub>	3.0	3.3	3.6	V	
Input high voltage	V <sub>IH</sub>	2.0	3.0	V <sub>DDQ</sub> +0.3	V	1
Input low voltage	V <sub>IL</sub>	-0.3	0	0.8	V	2
Output high voltage	V <sub>OH</sub>	2.4	-	-	V	I <sub>OH</sub> = -2mA
Output low voltage	V <sub>OL</sub>	-	-	0.4	V	I <sub>OL</sub> = 2mA
Input leakage current	I <sub>LI</sub>	-10	-	10	uA	3

**Notes :** 1. V<sub>IH</sub> (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.  
2. V<sub>IL</sub> (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.  
3. Any input 0V ≤ V<sub>IN</sub> ≤ V<sub>DDQ</sub>.  
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V<sub>DD</sub> = 3.3V, T<sub>A</sub> = 23°C, f = 1MHz, V<sub>REF</sub> = 1.4V ± 200 mV)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A <sub>0</sub> ~ A <sub>11</sub> )	C <sub>IN1</sub>	-	15	pF
Input capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ )	C <sub>IN2</sub>	-	15	pF
Input capacitance (CKE <sub>0</sub> )	C <sub>IN3</sub>	-	15	pF
Input capacitance (CLK <sub>0</sub> )	C <sub>IN4</sub>	-	20	pF
Input capacitance ( $\overline{\text{CS0}}$ , $\overline{\text{CS2}}$ )	C <sub>IN5</sub>	-	15	pF
Input capacitance (DQM <sub>0</sub> ~ DQM <sub>7</sub> )	C <sub>IN6</sub>	-	15	pF
Input capacitance (BA <sub>0</sub> ~ BA <sub>1</sub> )	C <sub>IN7</sub>	-	15	pF
Data input/output capacitance (DQ <sub>0</sub> ~ DQ <sub>63</sub> )	C <sub>OUT</sub>	-	16	pF
Data input/output capacitance (CB <sub>0</sub> ~ CB <sub>7</sub> )	C <sub>OUT1</sub>	-	16	pF

## DC CHARACTERISTICS

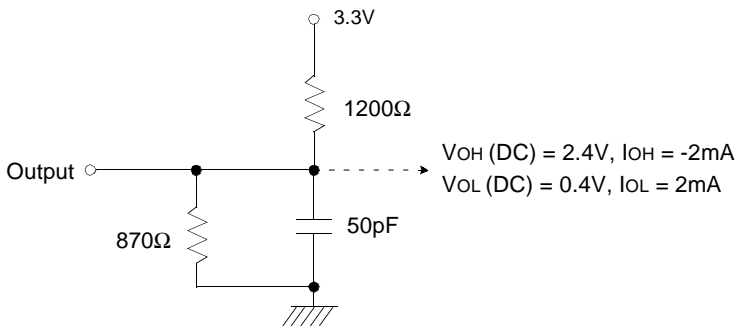
(Recommended operating condition unless otherwise noted, TA = 0 to 70°C)

Parameter	Symbol	Test Condition	Version	Unit	Note
			-75		
Operating current (One bank active)	I <sub>CC1</sub>	Burst length = 1 t <sub>RC</sub> ≥ t <sub>RC(min)</sub> I <sub>O</sub> = 0 mA	1,760	mA	1,3
Precharge standby current in power-down mode	I <sub>CC2P</sub>	CKE ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = 10ns	368	mA	3
	I <sub>CC2PS</sub>	CKE & CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞	20		
Precharge standby current in non power-down mode	I <sub>CC2N</sub>	CKE ≥ V <sub>IH(min)</sub> , $\overline{CS}$ ≥ V <sub>IH(min)</sub> , t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	620	mA	3
	I <sub>CC2NS</sub>	CKE ≥ V <sub>IH(min)</sub> , CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞ Input signals are stable	110		
Active standby current in power-down mode	I <sub>CC3P</sub>	CKE ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = 10ns	404	mA	3
	I <sub>CC3PS</sub>	CKE & CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞	56		
Active Standby current in non power-down mode	I <sub>CC3N</sub>	CKE ≥ V <sub>IH(min)</sub> , $\overline{CS}$ ≥ V <sub>IH(min)</sub> , t <sub>CC</sub> = 10ns Input signals are changed one time during 20ns	800	mA	3
	I <sub>CC3NS</sub>	CKE ≥ V <sub>IH(min)</sub> , CLK ≤ V <sub>IL(max)</sub> , t <sub>CC</sub> = ∞ Input signals are stable	272		
Operating current (Burst mode)	I <sub>CC4</sub>	I <sub>OL</sub> = 0mA Page burst 4 Banks activated t <sub>CCD</sub> = 2CLK	2,570	mA	1,3
Refresh current	I <sub>CC5</sub>	t <sub>RC</sub> ≥ t <sub>RC(min)</sub>	2,930	mA	2,3
Self refresh current	I <sub>CC6</sub>	CKE ≤ 0.2V	368	mA	3

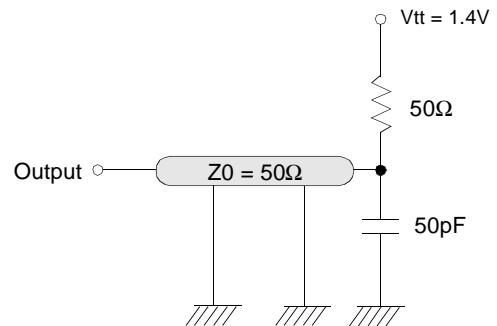
- Notes :**
1. Measured with outputs open.
  2. Refresh period is 64ms.
  3. Measured with 1 PLL & 3 Drive ICs.
  4. Unless otherwise noticed, Input swing level is CMOS(V<sub>IH</sub>/V<sub>IL</sub> = V<sub>DDQ</sub>/V<sub>SSQ</sub>)

**AC OPERATING TEST CONDITIONS** ( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = 0$  to  $70^\circ C$ )

Parameter	Value	Unit
AC input levels ( $V_{ih}/V_{il}$ )	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	$t_r/t_f = 1/1$	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

**OPERATING AC PARAMETER**

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version	Unit	Note
		-75		
Row active to row active delay	tRRD(min)	15	ns	1
RAS to CAS delay	tRCD(min)	20	ns	1
Row precharge time	tRP(min)	20	ns	1
Row active time	tRAS(min)	45	ns	1
	tRAS(max)	100	us	
Row cycle time	tRC(min)	65	ns	1
Last data in to row precharge	tRDL(min)	2	CLK	2,5
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns	-	5
Last data in to new col. address delay	tCDL(min)	1	CLK	2
Last data in to burst stop	tBDL(min)	1	CLK	2
Col. address to col. address delay	tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4
	-			

- Notes :**
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
  2. Minimum delay is required to complete write.
  3. All parts allow every cycle column address change.
  4. In case of row precharge interrupt, auto precharge and read burst stop.
  5. In 100MHz and below 100MHz operating conditions,  $t_{RDL}=1CLK$  and  $t_{DAL}=1CLK + 20ns$  is also supported. SAMSUNG recommends  $t_{RDL}=2CLK$  and  $t_{DAL}=2CLK + t_{RP}$ .

**AC CHARACTERISTICS** (AC operating conditions unless otherwise noted)**REFER TO THE INDIVIDUAL COMPONENT, NOT THE WHOLE MODULE.**

Parameter		Symbol	-75		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	tSAC	-	5.4	ns	1,2
Output data hold time	CAS latency=3	tOH	3	-	ns	1,2
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5.4	ns	1

**Notes :** 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns,  $(tr/2-0.5)$ ns should be added to the parameter.

3. Assumed input rise and fall time ( $tr$  &  $tf$ ) = 1ns.

If  $tr$  &  $tf$  is longer than 1ns, transient time compensation should be considered, i.e.,  $[(tr + tf)/2-1]$ ns should be added to the parameter.



SIMPLIFIED TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA <sub>0,1</sub>	A <sub>10/AP</sub>	A <sub>11</sub> , A <sub>9 ~ A<sub>0</sub></sub>	Note	
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2	
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3	
	Entry		L									3	
	Self Refresh	Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address			
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address (A <sub>0 ~ A<sub>9</sub></sub> )	4	
	Auto precharge enable									H		4,5	
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address (A <sub>0 ~ A<sub>9</sub></sub> )	4	
	Auto precharge enable									H		4,5	
Burst stop		H	X	L	H	H	L	X	X			6	
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X		
	All banks								X	H			
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X				
				L	V	V	V						
Exit	Exit	L	H	X	X	X	X	X	X				
				L	V	V	V						
Precharge power down mode	Entry	H	L	H	X	X	X	X	X				
				L	H	H	H						
	Exit	Exit	L	H	H	X	X	X	X	X			
					L	V	V	V					
DQM		H	X					V	X		7		
No operation command		H	X	H	X	X	X	X	X				
L	H			H	H								

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Notes : 1. OP Code : Operand code

A<sub>0 ~ A<sub>11</sub></sub> & BA<sub>0 ~ BA<sub>1</sub></sub> : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

A new command can be issued after 2 clock cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA<sub>0 ~ BA<sub>1</sub></sub> : Bank select addresses.

If both BA<sub>0</sub> and BA<sub>1</sub> are "Low" at read, write, row active and precharge, bank A is selected.

If both BA<sub>0</sub> is "Low" and BA<sub>1</sub> is "High" at read, write, row active and precharge, bank B is selected.

If both BA<sub>0</sub> is "High" and BA<sub>1</sub> is "Low" at read, write, row active and precharge, bank C is selected.

If both BA<sub>0</sub> and BA<sub>1</sub> are "High" at read, write, row active and precharge, bank D is selected.

If A<sub>10/AP</sub> is "High" at row precharge, BA<sub>0</sub> and BA<sub>1</sub> is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

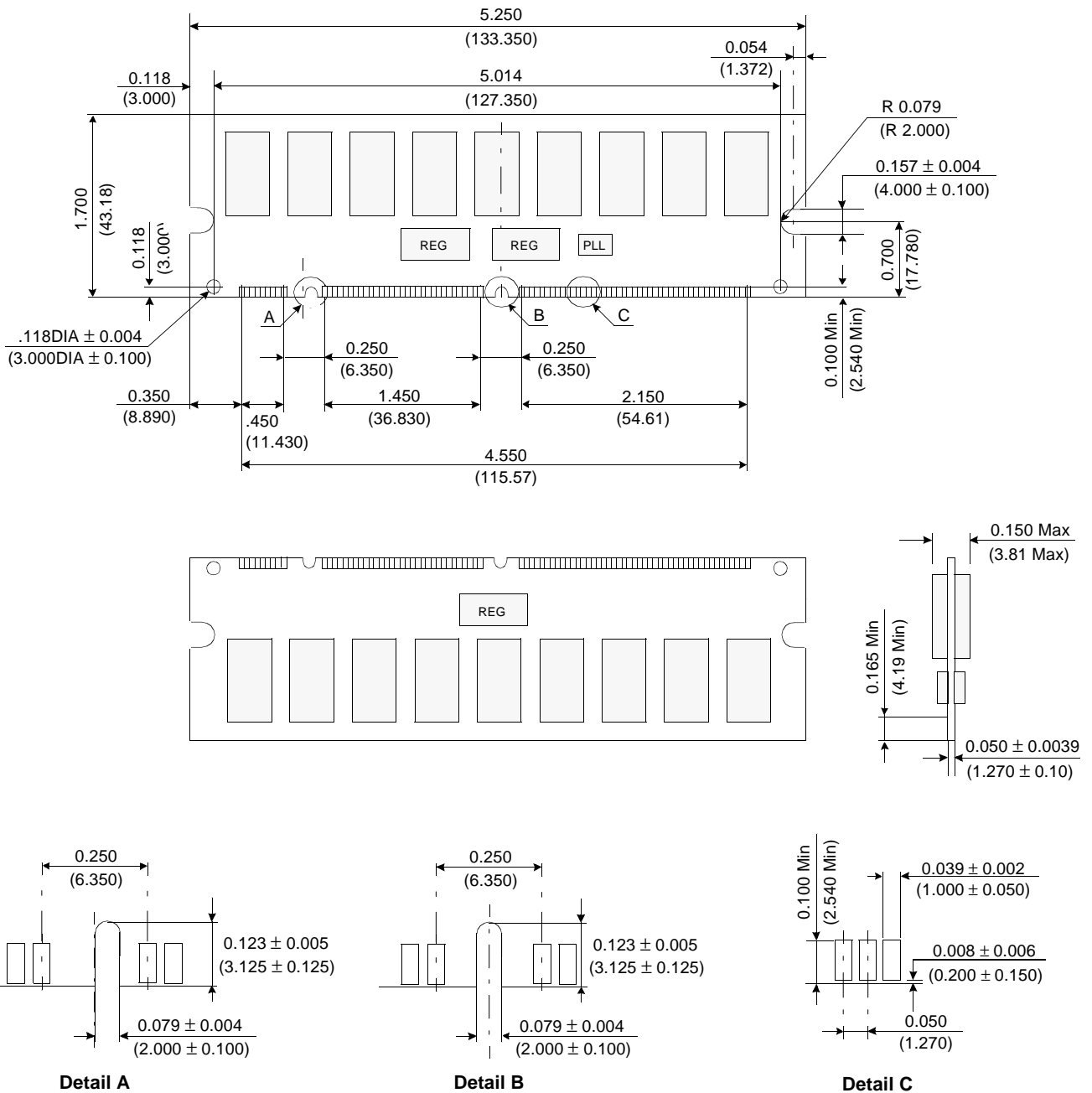
New row active of the associated bank can be issued at TRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified

The used device is 16Mx4 SDRAM, TSOP  
SDRAM Part No. : K4S640432E-TC75

This module is based on JEDEC PC133 Specification

# M390S1620ET1

# PC133 Registered DIMM

## M390S1620ET1-C75

- Organization : 16Mx72
- Composition : 16MX4 \*18
- Used component part # : K4S640432E-TC75
- # of rows in module : 1 Row
- # of banks in component : 4 banks
- Feature : 1,700mil height & double sided
- Refresh : 4K/64ms
- **Contents ;**

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
0	# of bytes written into serial memory at module manufacturer	128bytes	80h	
1	Total # of bytes of SPD memory device	256bytes (2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row address on this assembly	12	0Ch	1
4	# of column address on this assembly	10	0Ah	1
5	# of module rows on this assembly	1 Row	01h	
6	Data width of this assembly	72 bits	48h	
7	..... Data width of this assembly	-	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time @CAS latency of 3	7.5ns	75h	2
10	SDRAM access time from clock @CAS latency of 3	5.4ns	54h	2
11	DIMM configuration type	ECC	02h	
12	Refresh rate & type	15.625us, support self refresh	80h	
13	Primary SDRAM width	x4	04h	
14	Error checking SDRAM width	x4	04h	
15	Minimum clock delay for back-to-back random column address	tCCD = 1CLK	01h	
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	SDRAM device attributes : # of banks on SDRAM device	4 banks	04h	
18	SDRAM device attributes : CAS latency	3	04h	
19	SDRAM device attributes : CS latency	0 CLK	01h	
20	SDRAM device attributes : Write latency	0 CLK	01h	
21	SDRAM module attributes	Registered/Buffered DQM, address & control inputs and On-Card PLL	1Fh	
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh	
23	SDRAM cycle time @CAS latency of 2	-	00h	2
24	SDRAM access time from clock @CAS latency of 2	-	00h	2
25	SDRAM cycle time @CAS latency of 1	-	00h	
26	SDRAM access time from clock @CAS latency of 1	-	00h	
27	Minimum row precharge time (=tRP)	20ns	14h	
28	Minimum row active to row active delay (tRRD)	15ns	0Fh	
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h	
30	Minimum activate precharge time (=tRAS)	45ns	2Dh	
31	Module row density	1 Row of 128MB	20h	
32	Command and address signal input setup time	1.5ns	15h	
33	Command and address signal input hold time	0.8ns	08h	
34	Data signal input setup time	1.5ns	15h	

Byte #	Function Described	Function Supported	Hex value	Note
		-75	-75	
35	Data signal input hold time	0.8ns	08h	
36~61	Superset information (maybe used in future)	-	00h	
62	SPD data revision code	JEDEC2	02h	
63	Checksum for bytes 0 ~ 62	-	C6h	
64	Manufacturer JEDEC ID code	Samsung	CEh	
65~71	..... Manufacturer JEDEC ID code	Samsung	00h	
72	Manufacturing location	Onyang Korea	01h	
73	Manufacturer part # (Memory module)	M	4Dh	
74	Manufacturer part # (DIMM Configuration)	3	33h	
75	Manufacturer part # (Data bits)	Blank	20h	
76	..... Manufacturer part # (Data bits)	9	39h	
77	..... Manufacturer part # (Data bits)	0	30h	
78	Manufacturer part # (Mode & operating voltage)	S	53h	
79	Manufacturer part # (Module depth)	1	31h	
80	..... Manufacturer part # (Module depth)	6	36h	
81	Manufacturer part # (Refresh, #of banks in Comp. & Interface)	2	32h	
82	Manufacturer part # (Composition component)	0	30h	
83	Manufacturer part # (Component revision)	E	45h	
84	Manufacturer part # (Package type)	T	54h	
85	Manufacturer part # (PCB revision & type)	1	31h	
86	Manufacturer part # (Hyphen)	" - "	2Dh	
87	Manufacturer part # (Power)	C	43h	
88	Manufacturer part # (Minimum cycle time)	7	37h	
89	Manufacturer part # (Minimum cycle time)	5	35h	
90	Manufacturer part # (TBD)	Blank	20h	
91	Manufacturer revision code (For PCB)	1	31h	
92	..... Manufacturer revision code (For component)	E-die (6th Gen.)	45h	
93	Manufacturing date (Year)	-	-	3
94	Manufacturing date (Week)	-	-	3
95~98	Assembly serial #	-	-	4
99~125	Manufacturer specific data (may be used in future)	Undefined	-	5
126	Reserved	100MHz	64h	
127	Reserved	CLK0, CL-3, ConAP	85h	
128+	Unused storage locations	Undefined	-	5

- Note :**
1. The row select address is excluded in counting the total # of addresses.
  2. This value is based on the component specification.
  3. These bytes are programmed by code of Date Week & Date Year with BCD format.
  4. These bytes are programmed by Samsung 's own Assembly Serial # system. All modules may have different unique serial #.
  5. These bytes are Undefined and can be used for Samsung's own purpose.