MOBILE PENTIUM® II PROCESSOR AT 233 MHz, 266 MHz, AND 300 MHz

- **Available at 233 MHz, 266 MHz and 300 MHz**
- **Supports the Intel Architecture with Dynamic Execution**
- **Dual Independent Bus (DIB) architecture**
- **Integrated primary 16-Kbyte instruction cache and 16-Kbyte write back data**
- **Integrated second level cache (512-Kbyte)**
- **Integrated thermal diode and sensor**
- **Mini-cartridge packaging technology**
  - **Supports thin form factor notebook designs**
  - **Exposed die enables more efficient heat dissipation**
- **Fully compatible with previous Intel microprocessors**
  - **Binary compatible with all applications**
  - **Support for MMX™ technology**
- **Power Management Features**
  - **Quick Start and Deep Sleep modes provide extremely low power dissipation**
- **Low-Power GTL+ processor system bus interface**
- **Integrated math co-processor**
- **High Reliability error detection with 64-bit system bus with Error Correction Code**

The Intel® Mobile Pentium® II processor introduces a higher level of performance for today's mobile computing environment, including multimedia enhancements and improved Internet and communications capabilities. It provides an improved performance[1] available for applications running on advanced operating systems such as Windows 98*. On top of its built-in power management capabilities, the Mobile Pentium II processor takes advantage of software designed for Intel's MMX™ technology to unleash enhanced color, smoother graphics and other multimedia and communications enhancements.

The Mobile Pentium II processor may contain design defects or errors know as errata which may cause the product to deviate from published specifications. Current characterized errata are available upon request.

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1. Refer to the *Mobile Pentium® II Processor Performance Brief*.

ORDER NUMBER: 243669-002

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1. INTRODUCTION

The Mobile Pentium® II processor is the first implementation of the Pentium II Processor family that is optimized for the mobile platform. It will initially be offered at three speeds: 300 MHz, 266 MHz, and 233 MHz, with a system bus speed of 66 MHz. It consists of a Mobile Pentium II processor core with an integrated L2 cache controller and a 64-bit high performance system bus. The Mobile Pentium II processor has a private cache bus that allows a high performance 64-bit wide cache subsystem to be gluelessly implemented using a TagRAM and two PBSRAM (Pipeline Burst SRAM) devices. The Mobile Pentium II processor is able to cache the first 512 Mbytes of memory using a 512-Kbyte cache data array composed of PBSRAMs. The private L2 cache bus complements the system bus by providing critical data faster, improving performance, and reducing total system power consumption. The Mobile Pentium II processor's 64-bit wide Low Power GTL+ (Gunning Transceiver Logic) system bus is compatible with the 440BX AGPset and provides a glueless, point-to-point interface for an I/O bridge/memory controller. Figure 1.1 shows the various parts of a Mobile Pentium II processor-based system and how the Mobile Pentium II processor connects to them.

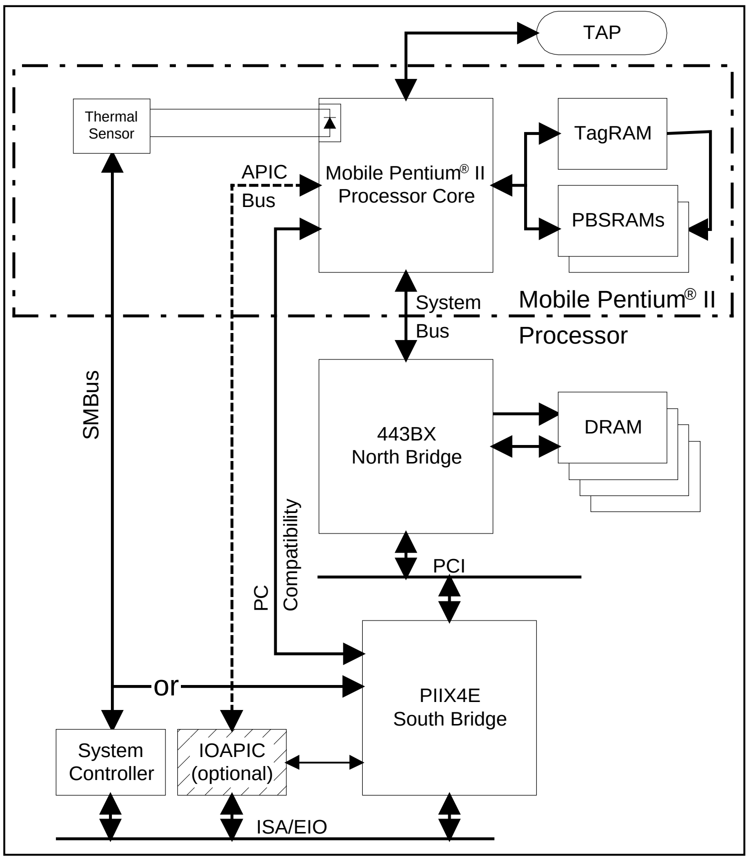

Figure 1.1 Signal Groups of a Mobile Pentium® II Processor-based System

1.1. Architecture Overview

- Architectural enhancements to improve performance
    - Supports the Intel Architecture with Dynamic Execution
    - Supports the Intel Architecture MMX™ technology
    - Integrated Intel Floating-Point Unit compatible with the IEEE Std 754
- Integrated primary (L1) instruction and data caches
    - 4-way set associative, 32-byte line size, 1 line per sector
    - 16-Kbyte instruction cache and 16-Kbyte writeback data cache
    - Cacheable range programmable by processor programmable registers
- Integrated second level (L2) cache
    - Dedicated 64-bit wide bus for high speed data transfers
    - 512-Kbyte, ECC protected cache data array
    - Uses Intel designed TagRAM
    - Clock to PBSRAMs turns off when processor is in low power states
- Low Power GTL+ system bus interface
    - 64-bit data bus, 66-MHz operation
    - Uni-processor, two loads only (processor and I/O bridge/memory controller)
    - Short trace length and low capacitance allows for single ended termination
- Voltage reduction technology
- New Pentium II processor family clock control
    - Quick Start for low power, low exit latency clock "throttling"
    - Deep Sleep mode for an extremely low power dissipation
- Accurate processor temperature sensor

1.2. Terminology

In this document a '#' symbol following a signal name indicates that the signal is active low. This means that when the signal is asserted (based on the name of the signal) it is in an electrical low state. Otherwise, signals are driven in an electrical high state when they are asserted. In state machine diagrams, a signal name in a condition indicates the condition of that signal being asserted. If the signal name is preceded by a '!' symbol, then it indicates the condition of that signal not being asserted. For example, the condition '!STPCLK# and HS' is equivalent to 'the active low signal STPCLK# is unasserted (i.e., it is at 2.5V) and the HS condition is true.' The symbols 'L' and 'H' refer respectively to electrical low and electrical high signal levels. The symbols '0' and '1' refer respectively to logical low and logical high signal levels. For example, BD[3:0] = '1010' = 'HLHL' refers to a hexadecimal 'A', and D[3:0]# = '1010' = 'LHLH' also refers to a hexadecimal 'A'.

1.3. References

Pentium® II Processor at 233 MHz, 266 MHz, 300 MHz and 333 MHz (Order Number 243335)

Pentium® II Processor Developer's Manual (Order Number 243341)

CKDM66-M Clock Driver Specification (Contact your Intel Field Sales Representative)

Intel Architecture Software Developer's Manual (Order Number 243193)

Volume I: Basic Architecture (Order Number 243190-001)
Volume II: Instruction Set Reference (Order Number 243191-001)
Volume III: System Programming Guide (Order Number 243192-001)

Mobile Pentium® II Processor I/O Buffer Models, IBIS Format (Available in electronic format; contact your Intel Field Sales Representative)

Mobile Pentium® II Processor System Bus Layout Guideline (Order Number 243672-001)

Mobile Pentium® II Processor Mini-cartridge Processor Mechanical and Thermal User's Guide (Order Number 243671-001)

System Management Bus Specification, Revision 1.0 (Available on the World Wide Web; contact your Intel Field Sales Representative)

Mobile Pentium® II Processor and Pentium II Processor Mobile Module Thermal Power Consumption (Order Number 243670-001)

Mobile Pentium® II Processor/440BX AGPset Datasheet (Order Number 290633-001)

Mobile Pentium® II Processor and Pentium II Processor Mobile Module Thermal Sensor Programming Interface Specification (Contact your Intel Field Sales Representative)

2. MOBILE PENTIUM® II PROCESSOR FEATURES

2.1. Differences Between the Mobile Pentium® II Processor and the Pentium II Processor

- Fault Tolerance (FRC)

The Pentium® II processor supports a master/checker processor configuration for high integrity, fault tolerant operation. This mode is not supported in the Mobile Pentium II processor and there is no FRCERR pin.

- Local APIC

The Pentium® II processor requires that the PICCLK pin be driven with a valid APIC clock signal even when the APIC is not used. No APIC clock signal is required in the Mobile Pentium II processor if the PICD0 pin is strapped to ground at reset.

- Voltage Reduction Technology

The Pentium® II processor uses a single voltage for the core and the L2 cache I/O buffers while the Mobile Pentium II processor permits the core voltage to be lower than the L2 I/O voltage. This allows the processor to achieve a much lower power consumption while maintaining a 1.8V L2 interface. Both processors have 2.5V tolerant buffers for non-GTL+ system logic signals (clocks, APIC, TAP and PC compatibility).

- Low Power GTL+

The Pentium® II processor GTL+ bus uses 56Ω termination at both ends or one end of the bus and limits on stub lengths to allow three loads on the long GTL+ bus. The Mobile Pentium II processor supports Low Power GTL+ with a short, point-to-point, two load bus with the possibility of a socketed CPU. The recommended termination under Low Power GTL+ is single-ended and 120Ω termination resistors.

- Uniprocessor

The Pentium® II processor supports 2-way multi-processing but the Mobile Pentium II processor can only be used in uniprocessor systems.

- Thermal Sensor

The Mobile Pentium® II processor core has a thermal diode with a low impedance connection to anode and cathode package pins. On the Mobile Pentium II processor there is a thermal sensor attached to the diode that communicates the processor core temperature to the system logic through a system management bus (SMBus) interface. Having a thermal sensor integrated onto the processor core allows for better thermal management of the Mobile Pentium II processor system.

- THERM-TRIP#

The Mobile Pentium® II processor does not have a THERMTRIP# pin.

- L2 Cache Clock Stopping

The Pentium® II processor turns off the clocks to the L2 cache on the cache bus only when it is in the Deep Sleep state and leaves them running at all other times. The Mobile Pentium II processor core turns off the clocks to the PBSRAMs when it is in the Quick Start and Sleep states. The TagRAM clock is left running except in the Deep Sleep state.

- Quick Start

The Mobile Pentium® II processor has a new clock control state that is similar to the Stop Grant state but consumes less power. The Stop Grant state supports snooping of bus transactions generated by the priority bus device (usually the PCI bridge) and by symmetric processors. The Quick Start state only snoops bus priority device transactions, thus it is only usable in uniprocessor systems. The Stop Grant state supports the recognition of changes in input signals and the latching of edge-triggered interrupts (e.g., NMI, SMI#). In the Quick Start state input signal transitions are not allowed (see Section 2.2.5).

- Clock Ratio Selection

  The Pentium® II processor clock ratio is programmed into the processor at reset time on the LINT[1:0], IGNNE# and A20M# pins according to the encoding scheme in the *Pentium® II Processor Developer's Manual*. This requires logic on the system board to multiplex the clock ratio code onto these pins during reset. On the Mobile Pentium II processor the clock ratio is preprogrammed during manufacturing. The LINT[1:0], IGNNE# and A20M# pins are ignored at Reset on the Mobile Pentium II processor.

2.2. Power Management

2.2.1. THE MOBILE PENTIUM® II PROCESSOR CLOCK CONTROL ARCHITECTURE

The Mobile Pentium® II processor clock control architecture (Figure 2.1) has been optimized for leading edge deep green desktop and mobile computer designs. The Auto Halt state provides a low power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low power, low exit latency clock state that can be used for hardware controlled "idle" computer states. The Deep Sleep state provides an extremely low power state that can be used for "Power-on Suspend" computer states, which is an alternative to shutting off the processor's power. Compared to the Pentium processor exit latency of 1 msec, the exit latency of the Deep Sleep state has been reduced to 30 µsec in the Mobile Pentium II processor. The Stop Grant and Sleep states shown in Figure 2.1 are intended for use in "Deep Green" desktop and server systems — not in mobile systems. Performing state transitions not shown in Figure 2.1 is neither recommended nor supported.

The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep and Deep Sleep states. The Stop Grant and Quick Start clock states are mutually exclusive, i.e., a strapping option on pin A15# chooses which state is entered when the STPCLK# signal is asserted. The Quick Start state is enabled by strapping the A15# pin to ground at Reset; otherwise, asserting the STPCLK# signal puts the processor into the Stop Grant state. The Stop Grant state has a higher power level than the Quick Start state and is designed for SMP platforms. The Quick Start state has a much lower power level, but it can only be used in uniprocessor platforms. Table 2.2 provides clock state characteristics (power numbers based on estimates for a Mobile Pentium II processor running at 266 MHz), which are described in detail in the following sections.

2.2.2. NORMAL STATE

The Normal state of the processor is the normal operating mode where the processor's internal clock is running and the processor is actively executing instructions.

Table 2.1 New Pins in the Mobile Pentium® II Processor

Pin Name	Type	Description
SMBALERT#	O	Thermal sensor attention signal.
SMBCLK	I/O	SMBus clock signal. Refer to the *System Management Bus Specification* for descriptions and specifications of the three SMBus signals.
SMBDATA	I/O	SMBus data signal. Refer to the *System Management Bus Specification* for descriptions and specifications of the three SMBus signals.

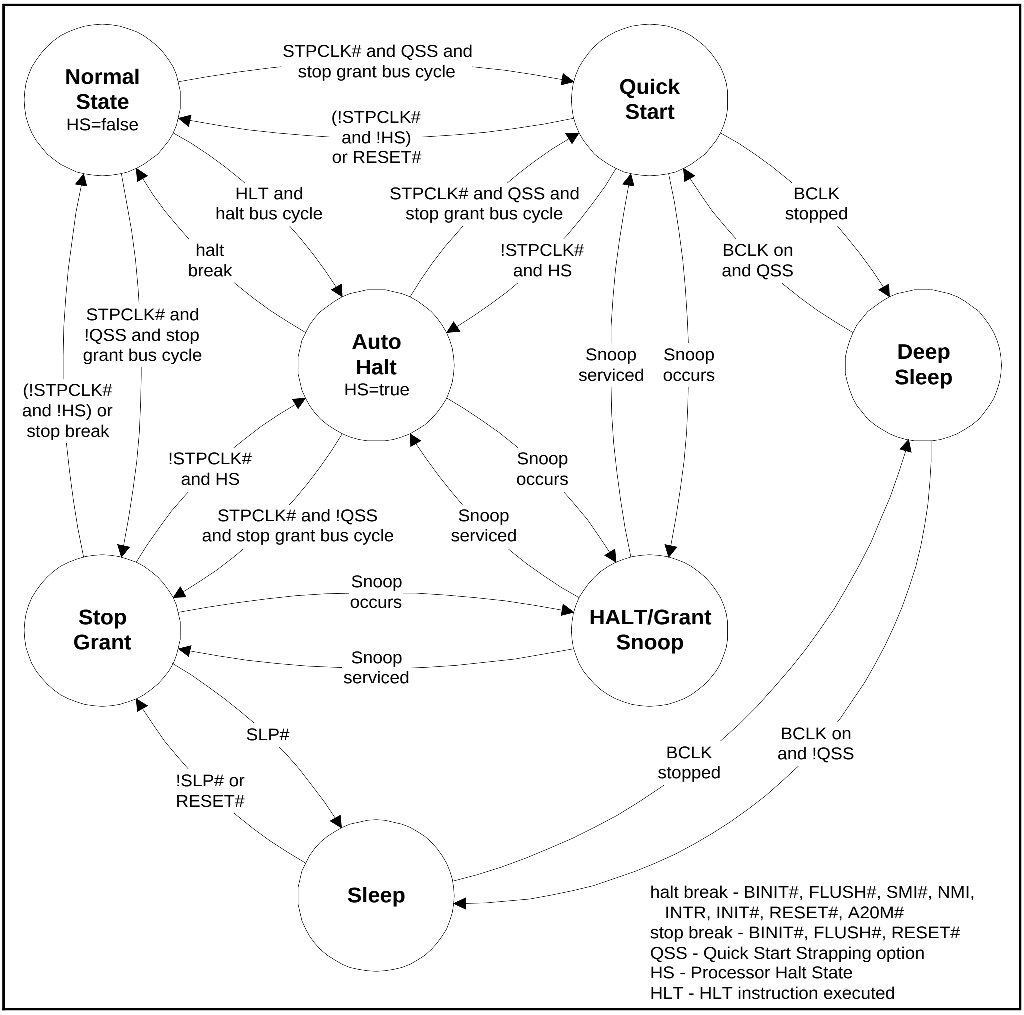

Figure 2.1 Mobile Pentium® II Processor Clock Control States

Table 2.2 Mobile Pentium® II Processor Clock State Characteristics

Clock State	Exit Latency	Power	Snooping?	System Uses
Normal	N/A	Varies	Yes	Normal program execution
Auto Halt	Approximately 10 bus clocks	1.2 W	Yes	S/W controlled entry idle mode
Stop Grant	10 bus clocks	1.2 W	Yes	H/W controlled entry/exit mobile throttling
Quick Start	Through snoop, **to *HALT/Grant Snoop*** state: immediate Through STPCLK#, to ***Normal*** state: 10 bus clocks	0.5 W	Yes	H/W controlled entry/exit mobile throttling
HALT/ Grant Snoop	A few bus clocks after the end of snoop activity.	Not specified	Yes	Supports snooping in the low power states
Sleep	To ***Stop Grant*** state 10 bus clocks	0.5 W	No	H/W controlled entry/exit desktop idle mode support
Deep Sleep	30 µsec	100 mW	No	H/W controlled entry/exit Mobile powered-on suspend support

NOTE: Not 100% tested. Specified at 50ºC by design/characterization.

2.2.3. AUTO HALT STATE

This is a low power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH# or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Stop Grant or Quick Start state, where a Stop Grant Acknowledge bus cycle will be issued. By deasserting STPCLK#, system logic can return the processor to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# interrupt is recognized in the Auto Halt state. The return from the System Management Interrupt (SMI) handler can be to either the Normal state or the Auto Halt state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from SMM.

The FLUSH# signal is serviced in the Auto Halt state. After the on-chip and off-chip caches have been flushed, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# pin are recognized while in the Auto Halt state.

2.2.4. STOP GRANT STATE

The processor enters this mode with the assertion of the STPCLK# signal when it is configured for Stop Grant state (via the A15# strapping option). The processor is still able to respond to snoop requests and latch interrupts. Latched interrupts will be serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event will be latched. A transition back to the Normal state can be made by the de-assertion of the STPCLK# signal, or the occurrence of a stop break event (a BINIT#, FLUSH# or RESET# assertion).

While in the Stop Grant state, SMI#, INIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the normal state. Only one occurrence of each event will be recognized upon return to the normal state.

The processor will return to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been de-asserted.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Stop Grant state after initialization until STPCLK# is deasserted.

If the FLUSH# signal is asserted, the processor will flush the on-chip and off-chip caches and return to the Stop Grant state. A transition to the Sleep state can be made by the assertion of the SLP# signal (see Section 2.2.7 for a description).

2.2.5. QUICK START STATE

This is a mode entered by the processor with the assertion of the STPCLK# signal when it is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state the processor is only capable of acting on snoop transactions generated by the system bus priority device. Because of its snooping behavior, Quick Start can only be used in a Uniprocessor (UP) configuration.

A transition to the Deep Sleep state (see Section 2.2.8) can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupt, servicing snoop transactions from symmetric bus masters or responding to FLUSH# or BINIT# assertions. While the processor is in the Quick Start state, it will not respond properly to any input signal other than STPCLK#, RESET# or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state. The thermal sensor will respond normally to SMBus transactions when the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

Asserting the SLP# signal when the processor is configured for Quick Start will result in unpredictable behavior and is not recommended.

2.2.6. HALT/GRANT SNOOP STATE

The Mobile Pentium® II processor will respond to snoop transactions on the system bus while in the Auto Halt, Stop Grant or Quick Start state. When a snoop transaction is presented on the system bus the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop on the system bus has been serviced and the system bus is quiet. After the snoop has been serviced, the processor will return to the previous Auto Halt, Stop Grant or Quick Start state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state, except for those signal transitions that are required to perform the snoop.

2.2.7. SLEEP STATE

The Sleep state is a very low power state in which the processor maintains its context and the phase-locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state, the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or Auto Halt states.

The processor can be reset by the RESET# pin while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly executes the Reset sequence.

Input signals (other than RESET#) may not change while the processor is in the Sleep state or transitioning into or out of the Sleep state. Input signal changes at these times will cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state. The thermal sensor will respond normally to SMBus transactions when the processor is in the Sleep state.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by removing the processor's input clock. PICCLK may be removed in the Sleep state.

2.2.8. DEEP SLEEP STATE

The Deep Sleep state is the lowest power mode the processor can enter while maintaining its context. The Deep Sleep state is entered by stopping the BCLK input to the processor, while it is in the Sleep or Quick Start state. For proper operation, the BCLK input should be stopped in the low state.

To re-enter either the Sleep or Quick Start state from the Deep Sleep state, the BCLK input must be restarted. The processor will return to the Sleep or Quick Start state, as appropriate, after 30 msec. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on when transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion will result in unpredictable behavior. The thermal sensor will respond normally to SMBus transactions when the processor is in the Deep Sleep state.

2.2.9. CURRENTLY SUPPORTED CLOCK STATES

Table 2.3 shows the low-power clock states supported by the Pentium® II processor family product line.

2.2.10. OPERATING SYSTEM IMPLICATIONS OF THE QUICK START AND SLEEP STATES

There are a number of architectural features of the Mobile Pentium® II processor that are not available when the Quick Start state is enabled or do not function in the Quick Start or Sleep state as they do in the Stop Grant state. These features are part of the APIC, time-stamp counter and performance monitor counters.

The local APIC timer does not behave properly when the processor is in the Quick Start or Sleep state. There is no guarantee that the local APIC timer will count down in the Quick Start or Sleep state. If the timer counts down to zero when the processor is in or about to enter the Quick Start or Sleep state, the processor's behavior will be unpredictable. Inter-Processor Interrupts (IPIs)

Table 2.3 Low-Power Clock States Supported by Processor

Processor	Clock State				
	Stop Grant	**Auto Halt**	**Quick Start**	**Sleep**	**Deep Sleep**
Pentium® Pro Processor	X	X			
Pentium® II Processor	X	X		X	X
Mobile Pentium® II Processor	X	X	X	X	X

should not be used in Mobile Pentium II processor systems. If software generates an IPI just before the processor enters the Quick Start or Sleep state, then a message on the APIC bus will be generated. This violates the requirement stated in Section 2.2.5 that no input signals toggle in the Quick Start or Sleep state. Any software-generated IPI in a Mobile Pentium II processor system (uniprocessor system) will always result in an error.

The time-stamp counter and the performance monitor counters are not guaranteed to count in the Quick Start or Sleep states. If software sets the APIC interrupt enable bit of either of the performance counters, then the resulting behavior will be unpredictable.

2.3. Low Power GTL+

The Mobile Pentium® II processor system bus signals use a *variation* of the low-voltage GTL (Gunning Transceiver Logic) signaling technology. The Mobile Pentium II processor system bus specification is similar to the Pentium II processor system bus specification, which is itself a version of GTL with enhanced noise margins and less ringing. The Mobile Pentium II processor system bus specification reduces system cost and power consumption by raising the termination voltage and termination resistance and changing the termination from dual ended to single ended. Because the specification is different from the standard GTL specification and from the Pentium II processor GTL+ specification, it is referred to as Low Power GTL+.

The Pentium® II processor GTL+ system bus depends on incident wave switching and uses flight time for timing calculations of the GTL+ signals. The Low Power GTL+ system bus is short and lightly loaded. With Low Power GTL+ signals, timing calculations are based on capacitive derating. Analog signal simulation of the system bus including trace lengths is highly recommended to ensure that there are no significant transmission line effects. Contact your field sales representative to receive the IBIS models for the Mobile Pentium II processor.

The GTL+ system bus of the Pentium II processor was designed to support high speed data transfers with multiple loads on a long bus that behaves like a transmission line. However, in a mobile system, the system bus only has two loads (the processor and the chipset) and the bus traces are short enough that transmission line effects are not significant. It is possible to change the layout and termination of the system bus to take advantage of the mobile environment using the same GTL+ I/O buffers. The benefit is that it reduces the number of terminating resistors in half and substantially reduces the AC and DC power dissipation of the system bus. Low Power GTL+ uses GTL+ I/O buffers, although only two loads are allowed. The trace length is limited and the bus is terminated at one end only. Since the system bus is small and lightly loaded, it behaves like a capacitor, and the GTL+ I/O buffers behave like high speed open-drain buffers. With a 66-MHz bus frequency, the pull-up would be 120Ω. V_{TT} has been increased from 1.5V to processor core V_{CC} to eliminate the need for a 1.5V power plane. If 100Ω termination resistors are used rather than 120Ω, then 20 percent more power will be dissipated in the termination resistors. 120Ω termination is recommended to conserve power.

Refer to the *Mobile Pentium® II Processor System Bus Layout Guideline* for details on laying out the Low Power GTL+ system bus.

2.3.1. LOW POWER GTL+ PINS

Two signals of the system bus will potentially not meet the Low Power GTL+ layout requirements: PRDY# and RESET#. These two signals connect to the debug port described in Section 7 and thus cannot meet the maximum length requirements. Also, RESET# is potentially used to generate a reset configuration selection signal. If PRDY# or RESET# do not meet the layout requirements for Low Power GTL+, then they must be terminated using dual-ended termination at 120Ω. Higher resistor values can be used if simulations show that the signal quality specifications in Section 4 are met.

2.4. Mobile Pentium® II Processor CPUID

The CPUID instruction does not distinguish between the Mobile Pentium® II and Pentium II processors. After a power-on RESET, or when the CPUID instruction is executed, the EAX register contains the values shown in Table 2.4.

Table 2.4 Mobile Pentium® II Processor CPUID

Reserved [31:14]	Type [13:12]	Family [11:8]	Model [7:4]	Stepping [3:0]
X	0	6	5	X

3. ELECTRICAL SPECIFICATIONS

3.1. The Mobile Pentium® II Processor System Signals

Table 3.1 lists the Mobile Pentium® II processor system signals by type. All Low Power GTL+ signals are synchronous with the BCLK signal. All TAP signals are synchronous with the TCK signal except TRST#. All PC Compatibility signals (CMOS inputs) can be applied asynchronously.

The CMOS, Clock, APIC and TAP inputs can be driven from ground to 2.5V. The FERR#, IERR#, APIC and TAP outputs are open drain and should be pulled up to 2.5V using resistors with the values shown in Table 3.2. If open drain drivers are used for input signals, then they should also be pulled up to 2.5V using resistors with the values shown in Table 3.2.

Table 3.1 System Signal Groups

Group Name	Signals
Low Power GTL+ Input	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
Low Power GTL+ Output	PRDY#
Low Power GTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
CMOS Input[1,2]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD, SLP#, SMI#, STPCLK#
Open Drain Output[2]	FERR#, IERR#
Thermal Sensor	SMBALERT#, SMBCLK, SMBDATA
Clock[2]	BCLK
APIC Clock[2]	PICCLK
APIC I/O[2]	PICD[1:0]
TAP Input[2]	TCK, TDI, TMS, TRST#
TAP Output[2]	TDO
Power/Other[3]	V_{CC}, V_{CC_S}, V_{CCP}, V_{CCP_S}, V_{CC3}, VID[3:0], V_{SS}, V_{SS_S}

NOTES:

1. See Section A.1 in Appendix A for information on the PWRGOOD signal.
2. These signals are tolerant to 2.5V only.
3. V_{CC} is the power supply for the Mobile Pentium® II processor core.
   V_{CCP} is the power supply for the Cache Bus I/O voltage.
   V_{CC3} is the power supply for the Tag RAM and the PBSRAM cores.
   V_{SS} is system ground.
   V_{CC_S}, V_{CCP_S} and V_{SS_S} are the voltage sense pins for V_{CC}, V_{CCP} and V_{SS}, respectively.

Table 3.2 Recommended Pull-Up Resistors for Open Drain Signals[1, 2]

Recommended Resistor Value (Ω)	Open Drain Signal
150	PICD[1:0], TDI, TDO
680	STPCLK#
1K	INIT#, TCK, TMS
4.7K	A20M#, FERR#, FLUSH#, IERR#, IGNNE#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD, SLP#, SMI#

NOTES:

1. TRST# should be pulled to ground with a 680Ω to 1kΩ resistor.
2. Refer to Section 3.1.7 for the required pull-up or pull-down resistors for signals that are not being used.

3.1.1. POWER SEQUENCING REQUIREMENTS

The Mobile Pentium® II processor has no power sequencing requirements. It is recommended that all of the processor power planes rise to their specified values within one second of each other. The V_{CC} power plane must not rise too fast. At least 200 µsec (T_R) must pass from the time that V_{CC} is at 10% of its nominal value until the time that V_{CC} is at 90% of its nominal value (see Figure 3.0).

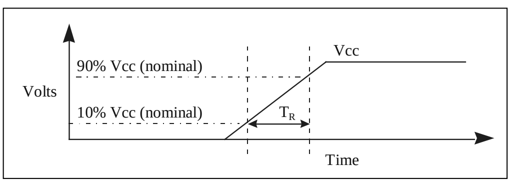

Figure 3.0 V_{CC} Ramp Rate Requirement

3.1.2. VOLTAGE SENSE PINS

The Mobile Pentium® II processor has three voltage sense pins to allow the V_{CC} and V_{CCP} power regulators to sense the V_{CC} and V_{CCP} voltage levels on the processor after the voltage drop at the connector. These pins are V_{CC_S}, V_{CCP_S} and V_{SS_S}. V_{SS_S} can also be used to generate a system shutdown signal if the system is turned on with no processor installed. If these pins are not used for voltage sense or processor presence sense, then they should be connected to V_{CC}, V_{CCP} and V_{SS}, respectively.

3.1.3. TEST ACCESS PORT (TAP) CONNECTION

The TAP interface is an implementation of the IEEE 1149.1 (“JTAG”) standard. Due to the voltage levels supported by the TAP interface, it is recommended that the Mobile Pentium® II processor and the other 2.5V JTAG specification compliant devices be last in the JTAG chain after any devices with 3.3V or 5V JTAG interfaces within the system. A translation buffer should be used to reduce the TDO output voltage of the last 3.3/5V device down to the 2.5V range that the Mobile Pentium II processor can tolerate. Multiple copies of TMS and TRST# must be provided, one for each voltage level.

A Debug Port and connector has been defined in Section 7. It may be placed at the start and end of the JTAG chain containing the processor, with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. There are no requirements for placement of the Mobile Pentium II processor in the JTAG chain, except for those dictated by voltage requirements of the TAP signals.

3.1.4. THERMAL SENSOR

Within the Mobile Pentium® II processor, there is a thermal sensor connected to the SMBus pins. The programming interface for the thermal sensor is described in the *Mobile Pentium® II Processor and Pentium® II Processor Mobile Module Thermal Sensor Programming Interface Specification*. The Mobile Pentium II processor thermal sensor supports an ACPI-compliant system implementation for monitoring the temperature of the processor. The thermal sensor only provides an accurate reading of the processor temperature when the processor is fully powered. The address of the thermal sensor on the processor SMBus is 1001101.

3.1.5. CATASTROPHIC THERMAL PROTECTION

The Mobile Pentium® II processor does not support catastrophic thermal protection. The thermal sensor must be used to protect the processor and the system against excessive temperatures.

3.1.6. SMBUS PINS

SMBus is a subset of the I^2C bus/protocol developed by Intel. I^2C is a two-wire communications bus/protocol developed by Philips*. Contact your Intel Field Sales Representative for a copy of the System Management Bus specification.

3.1.7. UNUSED PINS

All RESERVED pins must be unconnected. Unused Low Power GTL+ inputs, outputs and bi-directional signals should be individually connected to V_{CC} with 120Ω pull-up resistors. Unused CMOS active low inputs should be connected to 2.5V and unused active high inputs should be connected to V_{SS}. Unused open-drain outputs should be unconnected. If the processor is configured to enter the Quick Start state rather than the Stop Grant state, then the SLP# pin should be connected to 2.5V. When tying any signal to power or ground, a resistor will allow for system testability. For unused pins, it is suggested that 10kΩ resistors be used for pull-ups and 1kΩ resistors be used for pull-downs. If the VID[3:0] pins are not used then they should be connected to V_{SS} with a 1kΩ resistor.

If the local APIC is hardware disabled, then PICCLK and PICD[1:0] should be tied to V_{SS} with a 1kΩ resistor. Otherwise PICCLK must be driven with a clock that meets specification (see Table 3.13) and the PICD[1:0] pins must be pulled up to 2.5V with 150Ω resistors, even if the local APIC is not used.

3.1.8. PIN STATE IN LOW POWER STATES

3.1.8.1. System Bus Signals

All of the system bus pins have Low Power GTL+ input, output or input/output drivers. Except when servicing snoops, the system bus pins are tri-stated and pulled up by the termination resistors. Snoops are not permitted in the Sleep and Deep Sleep states.

3.1.8.2. PC Compatibility / Sideband Signals

The PC compatibility input pins are allowed to be in either the logic high or low state when the processor is in a low power state. In the Auto Halt and Stop Grant states these signals are allowed to toggle. These input buffers have no internal pull-up or pull-down resistors and system logic can use CMOS or open-drain drivers to drive them.

The PC compatibility output pins have open drain drivers and external pull-up resistors are required. One of the two output pins (IERR#) is a catastrophic error indicator and is tri-stated (and pulled-up) when the processor is functioning normally. The FERR# output can be either tri-stated or driven to V_{SS} when the processor is in a low power state depending on the condition of the floating point unit. Since this pin is a DC current path when it is driven to V_{SS}, it is recommended that the software clear or mask any floating point error condition before putting the processor into the Deep Sleep state.

3.1.8.3. Other Signals

The system bus clock (BCLK) must be driven in all of the low power states except the Deep Sleep state. The APIC clock (PICCLK) must be driven whenever BCLK is driven unless the APIC is hardware disabled or the processor is in the Sleep State. Otherwise, it is permitted to turn off PICCLK by holding it at V_{SS}. The system bus clock should be held at V_{SS} when it is stopped in the Deep Sleep state.

In the Auto Halt and Stop Grant states the APIC bus data pins (PICD[1:0]) may toggle due to APIC bus messages. These pins are required to be tri-stated and pulled-up when the processor is in the Quick Start, Sleep or Deep Sleep states unless the APIC is hardware disabled.

The state of the SMBus pins is determined by the policy embodied in the SMBus host controller. The thermal sensor can be accessed in all processor states as long as power is applied to the processor.

3.2. Decoupling Requirements

The Mobile Pentium® II processor has high frequency decoupling capacitors on all three power planes, but additional bulk decoupling capacitance is required. The amount of bulk decoupling required to meet the processor voltage tolerance requirement is a strong function of power supply design. Contact your Intel Field Sales Representative for tools to help determine how much decoupling is required. The cache bus power plane (V_{CCP}) requires 50 to 100 µF of decoupling. The L2 cache of the Mobile Pentium II processor requires 100 µF of decoupling on the 3.3V power plane (V_{CC3}) in addition to the decoupling required by the other 3.3V system components.

For the Low Power GTL+ pull-up resistors, one 0.1µF high frequency decoupling capacitor is recommended per resistor pack. There should be no more than eight pull-up resistors per resistor pack.

3.3. System Bus Clock and Processor Clocking

The 2.5V BCLK input directly controls the operating speed of the system bus interface. All system bus timing parameters are specified with respect to the rising edge of the BCLK input. The Mobile Pentium II processor core frequency is a multiple of the BCLK frequency. The ratio between the core frequency and the BCLK frequency is configured when the processor is manufactured.

Multiplying the bus clock frequency is necessary to increase performance while allowing for easier distribution of signals within the system. Clock multiplication within the processor is provided by the internal Phase Lock Loop (PLL), which requires a constant frequency BCLK input. During Reset, or on exit from the Deep Sleep state, the PLL requires some amount of time to acquire the phase of BCLK. This time is called the PLL lock latency, which is specified in Section 3.6.

3.4. Maximum Ratings

Table 3.3 contains the Mobile Pentium® II processor stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are provided in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

3.5. DC Specifications

Table 3.4 through Table 3.7 list the DC specifications for the Mobile Pentium® II processor. Specifications are valid only while meeting specifications for case temperature, clock frequency and input voltages. Care should be taken to read all notes associated with each parameter.

Table 3.3 Mobile Pentium® II Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{Storage}$	Storage Temperature	–40	85	°C	
$V_{CC(Abs)}$	Supply Voltage with respect to V_{SS}	–0.5	VID voltage + 1.0	V	
V_{CCP}	L2 cache I/O voltage	–0.3	3.0	V	
V_{CC3}	Tag RAM and PBSRAM core voltage	–0.3	4.0	V	
V_{IN}	Low Power GTL+ Buffer DC Input Voltage with respect to V_{SS}	–0.3	V_{CC} + 0.7	V	1
V_{IN25}	2.5V Buffer DC Input Voltage with respect to V_{SS}	–0.3	3.3	V	2
V_{SMB}	SMBus Buffer DC Input Voltage with respect to V_{SS}	–0.3	6.0	V	3
I_{VID}	VID pin current		5	mA	
I_{VSS_S}	V_{SS} sense pin current		5	mA	4

NOTES:

1. Parameter applies to the Low Power GTL+ signal groups only.
2. Parameter applies to PC Compatibility, APIC and TAP bus signal groups only.
3. Parameter applies to SMBCLK, SMBDATA and SMBALERT# signals.
4. When used as a processor presence detect signal.

Table 3.4 Mobile Pentium® II Processor Power Specifications [1]

T_{PROC} (processor core temperature) = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CC}	V_{CC} for core frequency	@ 300 MHz @ 266 MHz @ 233 MHz	1.48 1.48 1.48	1.6 1.6 1.6	1.72 1.72 1.72	V V V	±120 mV
$V_{CC,LP}$	V_{CC} when I_{CC} < 300 mA	@ 300 MHz @ 266 MHz @ 233 MHz	1.48 1.48 1.48	1.6 1.6 1.6	1.79 1.79 1.79	V V V	-120 mV [2] +190 mV
V_{CCP}	V_{CC} for L2 cache I/O buffers		1.71	1.8	1.89	V	1.8V ±5%
V_{CC3}	V_{CC} for Tag RAM and PBSRAM cores		3.135	3.3	3.465	V	3.3V ±5%
I_{CC}	I_{CC} for V_{CC} at core frequency	@ 300 MHz @ 266 MHz @ 233 MHz			7.91 7.03 6.15	A	[3]
I_{CCP}	I_{CC} for V_{CCP} (L2 cache I/O buffers)				0.5	A	[3, 4, 5]
I_{CC3}	I_{CC} for V_{CC3} (Tag RAM and PBSRAM cores)				0.75	A	[3, 4]
$I_{CC,DSLP}$	Processor core Deep Sleep leakage current				290	mA	$V_{CC, max}$ and 95°C core temperature[6]
$I_{CCP,DSLP}$	Processor L2 cache bus I/O Deep Sleep leakage current				5	mA	$V_{CCP, max}$ and 115°C core temperature[6]
$I_{CC3,DSLP}$	Processor L2 cache core and thermal sensor Deep Sleep leakage current				10	mA	$V_{CC3, max}$ and 115°C core temperature[6]
dI_{CC}/dt	Core power supply current slew rate				15	A/µs	[7, 8]
dI_{CC3}/dt	L2 core power supply current slew rate				1	A/µs	[7, 8]

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. A higher $V_{CC,MAX}$ is allowed when the processor is in a low power state to enable high efficiency, low current modes in the power regulator.
3. $I_{CCx,max}$ specifications are specified at $V_{CC,max}$, $V_{CCP,max}$ $V_{CC3,max}$ and $T_{CASE,max}$ and under maximum signal loading conditions. $I_{CCx,max}$ specifications are not specified at $V_{CC,LP,max}$. If that voltage specification is used then slightly higher current can be expected.
4. I_{CCP} is the current supply for the Mobile Pentium II processor L2 cache I/O buffers and the I/O buffers on the TagRAM and the PBSRAMs. I_{CC3} is the current supply for the Tag RAM and PBSRAM cores. These currents are specified for a processor with a 512 KB L2 cache.
5. Not 100% tested. Specified by design/characterization.
6. $I_{CCx,DSLP}$ specifications are specified at maximum voltages and temperatures and under maximum signal loading conditions.
7. Based on simulations and averaged over the duration of any change in current. Used to compute the maximum inductance and reaction time of the voltage regulator. This parameter is not tested.
8. Maximum values specified by design/characterization at nominal V_{CC} and V_{CC3}.

The signals on the Mobile Pentium® II processor system bus are included in the Low Power GTL+ signal group. These signals are specified to be terminated to V_{CC}. The termination and reference voltage specifications for these signals are listed in Table 3.5. The Mobile Pentium® II processor requires external termination and generates its own V_{REF}; the information in Table 3.5 is provided for system design.

The DC specifications for the Low Power GTL+ signals are listed in Table 3.6. Refer to the *Mobile Pentium® II Processor System Bus Layout Guideline* for full details of system V_{TT} and V_{REF} requirements.

The Clock, PC Compatibility and TAP pins are designed to interface at 2.5V CMOS levels to allow connection to other devices. The DC specifications for these 2.5V tolerant pins are listed in Table 3.7.

Table 3.5 Low Power GTL+ Bus DC Specifications

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{TT}	Bus Termination Voltage	$V_{CC,MIN}$	V_{CC}	$V_{CC,MAX}$	V	1
V_{REF}	Input Reference Voltage	$^5/_9V_{TT}$ - 2%	$^5/_9V_{TT}$	$^5/_9V_{TT}$ + 2%	V	± 2% [2]

NOTES:

1. The intent is to use the same power supply for V_{CC} and $V_{TT.}$
2. V_{REF} for the system logic should be created from V_{TT} by a voltage divider.

Table 3.6 Low Power GTL+ Signal Group DC Specifications

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	$^5/_9V_{TT}$ - 0.2	V	See Table 3.5 [1]
V_{IH}	Input High Voltage	$^5/_9V_{TT}$ + 0.2	V_{CC}	V	1
V_{OH}	Output High Voltage	—	—	V	See V_{TT} max in Table 3.5
R_{ON}	Output Low Drive Strength		35	Ω	
I_L	Leakage Current		± 100	µA	2
I_{LO}	Output Leakage Current		± 15	µA	3

NOTES:

1. V_{REF} worst case, not nominal. Noise on V_{REF} should be accounted for.
2. $(0 \leq V_{IN} \leq V_{CC})$.
3. $(0 \leq V_{OUT} \leq V_{CC})$.

Table 3.7 Clock, APIC, TAP and PC Compatibility Signal Group DC Specifications

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.3	0.7	V	
$V_{IL,BCLK}$	Input Low Voltage, BCLK at connector	–0.3	0.6	V	1
V_{IH}	Input High Voltage	1.7	2.625	V	
$V_{IH,BCLK}$	Input High Voltage, BCLK at connector	1.8	2.625	V	
V_{OL}	Output Low Voltage		0.4	V	2
V_{OH}	Output High Voltage	N/A	2.625	V	All outputs are open-drain
I_{OL}	Output Low Current		14	mA	
I_{LI}	Input Leakage Current		± 100	µA	3

NOTES:

1. V_{IL} for BCLK at the connector is 0.6V. Any timing specification that is relative to BCLK at the connector uses this voltage specification.
2. Parameter measured at 14 mA.
3. $(0 \le V_{IN} \le 2.625V)$.

3.6. AC Specifications

3.6.1. SYSTEM BUS, CLOCK, APIC, TAP AND PC COMPATIBILITY AC SPECIFICATIONS

The system bus timings specified in this section are defined at the Mobile Pentium® II processor connector.

Table 3.8 through Table 3.16 provide Mobile Pentium II processor AC specifications. The AC specifications are divided into the following categories: Tables 3.8 contains the system bus clock specifications; Table 3.9 contains the processor core frequencies and L2 cache bus frequencies; Table 3.10 contains the Low Power GTL+ specifications; Table 3.11 contains the PC Compatibility signal group specifications; Table 3.12 contains timings for the reset conditions; Table 3.13 contains the APIC specifications; Table 3.14 contains the TAP specifications; and Tables 3.15 and 3.16 contain the power management timing specifications.

All system bus AC specifications for the Low Power GTL+ signal group are relative to the rising edge of the BCLK input at $V_{IL,BCLK}$. All Low Power GTL+ timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

Table 3.8 System Bus Clock AC Specifications[1]

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Nom	Max	Unit	Figure	Notes
	System Bus Frequency		66.67		MHz		
T1	BCLK Period		15		ns	3.2	2
T1B	BCLK offset from connector to processor core	0.45		0.70	ns	3.1	3
T2	BCLK Period Stability			± 250	ps		4, 5
T3	BCLK High Time	4.84			ns	3.2	@>1.8V
T4	BCLK Low Time	5.1			ns	3.2	@<0.6V
T5	BCLK Rise Time	0.52		1.43	ns	3.2	(0.6V – 1.8V) 4
T6	BCLK Fall Time	0.52		1.43	ns	3.2	(1.8V – 0.6V) 4

NOTES:

1. All AC timings for Low Power GTL+ and CMOS signals are referenced to the BCLK rising edge at $V_{IL,BCLK}$ at the processor connector pins. This reference is to account for trace length and capacitance on the processor substrate, allowing for the processor core to receive the signal with a reference at 1.25V. All Low Power GTL+ signals are referenced at V_{REF} at the processor connector pins. All CMOS signals are referenced at 1.25V at the processor connector pins.
2. The BCLK period allows a +0.5 ns tolerance for clock driver variation.
3. The BCLK offset time is the absolute difference needed between the BCLK signal arriving at the connector at 0.6V vs. arriving at the processor core at 1.25V. The positive offset is needed to account for the delay between the connector and the processor core. The positive offset ensures that both the processor core and the system logic receive the BCLK edge concurrently.
4. Not 100% tested. Specified by design/characterization.
5. Measured on the rising edge of adjacent BCLKs at 1.25V. The jitter present must be accounted for as a component of BCLK skew between devices.

Table 3.9 Valid Mobile Pentium® II Processor Frequencies

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

BCLK Frequency (MHz)	Frequency Multiplier	Core Frequency (MHz)	Second Level Cache (MHz)
66.67	7/2	233.33	116.67
66.67	4	266.67	133.33
66.67	9/2	300.00	150.00

Table 3.10 Low Power GTL+ Signal Groups AC Specifications[1, 2]

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV
R_{TT} = 120Ω terminated to V_{CC}, V_{REF} = 5/9 V_{CC}, load = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	On system board signal trace length	2.54	10.67	cm		guideline
T7	Low Power GTL+ Output Valid Delay	0.0	8.0	ns	3.3	
T8	Low Power GTL+ Input Setup Time	3.2		ns	3.4	3, 4
T9	Low Power GTL+ Input Hold Time	0.9		ns	3.4	5
T10	RESET# Pulse Width	1		ms	3.5	6

NOTES:

1. All AC timings for Low Power GTL+ signals are referenced to the BCLK rising edge at $V_{IL,BCLK}$ at the processor connector pins. All Low Power GTL+ signals are referenced at V_{REF} at the processor connector pins.
2. Not 100% tested. Specified by design characterization. Equivalent specifications are tested at the processor core.
3. RESET# can be asserted (active) asynchronously, but must be de-asserted synchronously.
4. Specification is for a minimum 0.40V swing.
5. Specification is for a maximum 1.0V swing.
6. After V_{CC}, V_{CCp}, V_{CC3} and BCLK become stable, PWRGOOD must be asserted.

Table 3.11 PC Compatibility Signal Group AC Specifications[1, 2]

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T11	2.5V Output Valid Delay	0.9	10.4	ns	3.3	3, 4
T12	2.5V Input Setup Time	5.5		ns	3.4	5, 6, 7, 8
T13	2.5V Input Hold Time	1.8		ns	3.4	5
T14	2.5V Input Pulse Width, except PWRGOOD and LINT[1:0]	2		BCLKs	3.3	Active and Inactive states
T14B	LINT[1:0] Input Pulse Width	6		BCLKs	3.3	9
T15	PWRGOOD Inactive Pulse Width	10		BCLKs	3.6	10, 11

NOTES:

1. All AC timings for PC Compatibility signals are referenced to the BCLK rising edge at $V_{IL,BCLK}$ at the processor connector pins. All CMOS signals are referenced at 1.25V at the processor connector pins.
2. Not 100% tested. Specified by design characterization. Equivalent specifications are tested at the processor core.
3. Valid delay timings for these signals are specified into 150Ω to 2.5V and 30 pF.
4. Valid delay timings for these signals are specified to 2.5V + 5%. See Table 3.2 for pull-up resistor values.

5. These inputs may be driven asynchronously. However, to guarantee recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
6. A20M#, IGNNE#, INIT# and FLUSH# can be asynchronous inputs, but to guarantee recognition of these signals following an I/O write instruction, they must be valid with the TRDY# assertion of the corresponding bus transaction.
7. INTR and NMI function as PC Compatibility signals only when the APIC is disabled; otherwise, they function as LINT[1:0] signals. The PC Compatibility signal AC specifications apply in either case.
8. To use the I/O instruction restart feature of the Mobile Pentium® II processor, the SMI# signal must meet these setup and hold specifications at the clock edge two system bus clocks before the RS[2:0]# assertion of the bus transaction for the I/O instruction.
9. This specification only applies when the APIC is enabled and the LINT1 or LINT0 pin is configured as an edge-triggered interrupt with fixed delivery; otherwise specification T14 applies.
10. When driven inactive, or after V_{CC}, V_{CCP}, V_{CC3} and BCLK become stable. PWRGOOD must remain below $V_{IL,max}$ from Table 3.7 until all the voltage planes meet the voltage tolerance specifications in Table 3.4 and BCLK has met the BCLK AC specifications in Table 3.8 for at least 10 clock cycles. PWRGOOD must rise glitch-free and monotonically to 2.5V.
11. If the BCLK signal meets its AC specification within 150 ns of turning on then the PWRGOOD Inactive Pulse Width specification (T15) is waived and BCLK may start after PWRGOOD is asserted. PWRGOOD must still remain below $V_{IL,max}$ until all the voltage planes meet the voltage tolerance specifications.

Table 3.12 Reset Configuration AC Specifications[1]

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T16	Reset Configuration Signals (A[15:5]#, BR0#, FLUSH#, INIT#, PICD0) Setup Time	4		BCLKs	3.5	Before deassertion of RESET#
T17	Reset Configuration Signals (A[15:5]#, BR0#, FLUSH#, INIT#, PICD0) Hold Time	2	20	BCLKs	3.5	After clock that deasserts RESET#
T18	Reset PLL Lock Latency	1		ms	3.5 3.6	Before deassertion of RESET#

NOTE:

1. T19 and T20, although valid for other systems, are not relevant in mobile systems.

Table 3.13 APIC Bus Signal AC Specifications[1]

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T21	PICCLK Frequency	2	33.3	MHz		2
T22	PICCLK Period	30	500	ns	3.2	
T23	PICCLK High Time	12.0		ns	3.2	
T24	PICCLK Low Time	12.0		ns	3.2	
T25	PICCLK Rise Time	1	5	ns	3.2	
T26	PICCLK Fall Time	1	5	ns	3.2	
T27	PICD[1:0] Setup Time	8.5		ns	3.4	3
T28	PICD[1:0] Hold Time	3.0		ns	3.4	3
T29	PICD[1:0] Valid Delay	3.0	12.0	ns	3.3	3, 4, 5

NOTES:

1. All AC timings for APIC signals are referenced to the PICCLK rising edge at V_{IL} at the processor connector pins. All CMOS signals are referenced at 1.25V at the processor connector pins.
2. The minimum frequency is 2 MHz when PICD0 is at 2.5V at reset. If PICD0 is strapped to V_{SS} at reset then the minimum frequency is 0 MHz.
3. Referenced to PICCLK Rising Edge.
4. For open drain signals, Valid Delay is synonymous with Float Delay.
5. Valid delay timings for these signals are specified into 150Ω to 2.5V and 50 pF.

Table 3.14 TAP Signal AC Specifications at the Processor Connector Pins[1]

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T30	TCK Frequency	—	16.67	MHz		
T31	TCK Period	60	—	ns	3.2	
T32	TCK High Time	25.0		ns	3.2	≥ 1.7V [2]
T33	TCK Low Time	25.0		ns	3.2	≤ 0.7V [2]
T34	TCK Rise Time		5.0	ns	3.2	(0.7V-1.7V) [2, 3]
T35	TCK Fall Time		5.0	ns	3.2	(1.7V-0.7V) [2, 3]
T36	TRST# Pulse Width	40.0		ns	3.8	Asynchronous[2]
T37	TDI, TMS Setup Time	5.0		ns	3.7	[4]
T38	TDI, TMS Hold Time	14.0		ns	3.7	[4]
T39	TDO Valid Delay	0.9	10	ns	3.7	[5, 6]
T40	TDO Float Delay	0.0	25	ns	3.7	[2, 5, 6]
T41	All Non-Test Outputs Valid Delay	2.0	25	ns	3.7	[5, 7, 8]
T42	All Non-Test Outputs Float Delay		25	ns	3.7	[2, 5, 7, 8]
T43	All Non-Test Inputs Setup Time	5.0		ns	3.7	[4, 7, 8]
T44	All Non-Test Inputs Hold Time	13.0		ns	3.7	[4, 7, 8]

NOTES:

1. All AC timings for TAP signals are referenced to the TCK rising edge at V_{IL} at the processor connector pins. All CMOS signals are referenced at 1.25V at the processor connector pins.
2. Not 100% tested. Specified by design/characterization.
3. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16 MHz.
4. Referenced to TCK rising edge.
5. Referenced to TCK falling edge.
6. Valid delay timing for this signal is specified into 150Ω terminated to 2.5V and 50 pF.
7. Non-Test Outputs and Inputs are the normal output or input signals (except TCK, TRST#, TDI, TDO and TMS). These timings correspond to the response of these signals due to boundary scan operations.
8. During Debug Port operation use the normal specified timings rather than the TAP signal timings.

Table 3.15 Quick Start/Deep Sleep AC Specifications

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T45	Stop Grant Cycle Completion to Clock Stop	100		BCLKs	3.9	
T46	Stop Grant Cycle Completion to Input Signals Stable		0	ns	3.9	1
T47	Clock Start to PLL Lock		30	µs	3.9	
T48	STPCLK# Hold Time from PLL Lock	0		ns	3.9	
T49	Input Signal Hold Time from STPCLK# Deassertion	8		BCLKs	3.9	

NOTE:

1. Input signals other than SMBus, RESET# and BPRI# must be held constant in the Quick Start state.

Table 3.16 Stop Grant/Sleep/Deep Sleep AC Specifications

T_{PROC} = 0 °C to 100 °C, V_{CC} = 1.6V ±120mV, V_{CCP} = 1.8V ±90mV, V_{CC3} = 3.3V ±165mV

Symbol	Parameter	Min	Max	Unit	Figure	Notes
T50	SLP# Signal Hold Time from Stop Grant Cycle Completion	100		BCLKs	3.10	
T51	SLP# Assertion to Input Signals Stable		0	ns	3.10	1
T52	SLP# Assertion to Clock Stop	10		BCLKs	3.10	
T53	Clock Start to PLL Lock		30	µs	3.10	
T54	SLP# Hold Time from PLL Lock	0		ns	3.10	
T55	STPCLK# Hold Time from SLP# Deassertion	10		BCLKs	3.10	
T56	Input Signal Hold Time from SLP# Deassertion	10		BCLKs	3.10	

NOTE:

1. Input signals other than SMBus and RESET# must be held constant in the Sleep state.

Figures 3.1 through 3.10 are to be used in conjunction with Tables 3.8 through 3.16.

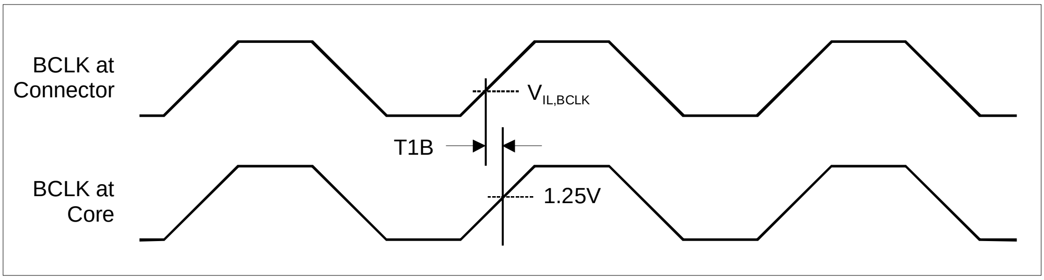

Figure 3.1 BCLK Connector to Core Offset

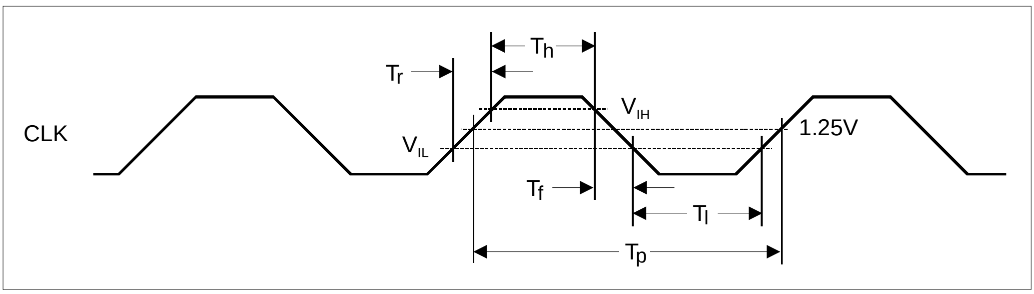

Figure 3.2 Generic Clock Waveform

NOTES:

T_r = T5, T34, T25 = Rise Time
T_f = T6, T35, T26 = Fall Time
T_h = T3, T32, T23 = High Time
T_l = T4, T33, T24 = Low Time
T_p = T1, T31, T22 = Period

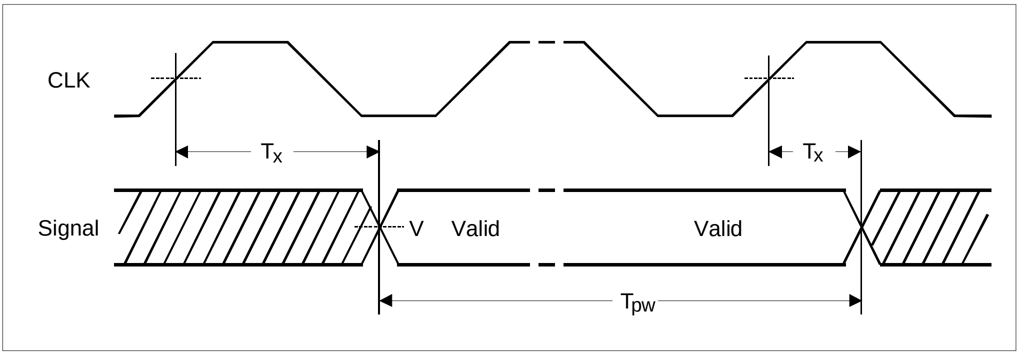

Figure 3.3 Valid Delay Timings

NOTES:

T_x = T7, T11, T29 = Valid Delay
T_{pw} = T14, T14B = Pulse Width
V = V_{REF} for Low Power GTL+ signal group; 1.25V for PC Compatibility, APIC and TAP signal groups

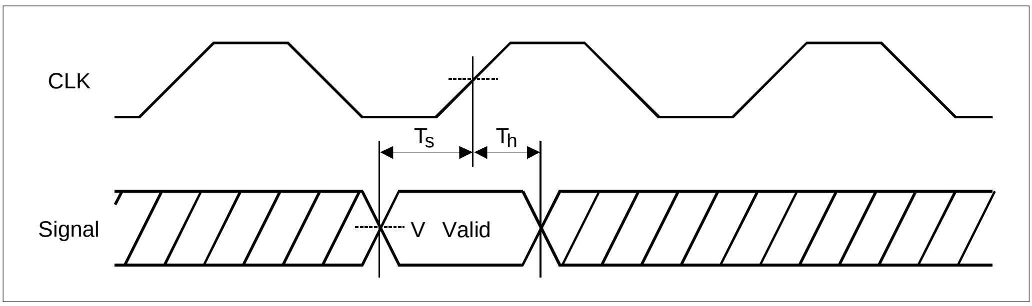

Figure 3.4 Setup and Hold Timings

NOTES:

T_s = T8, T12, T27 = Setup Time
T_h = T9, T13, T28 = Hold Time
V = V_{REF} for Low Power GTL+ signals; 1.25V for PC Compatibility, APIC and TAP signals

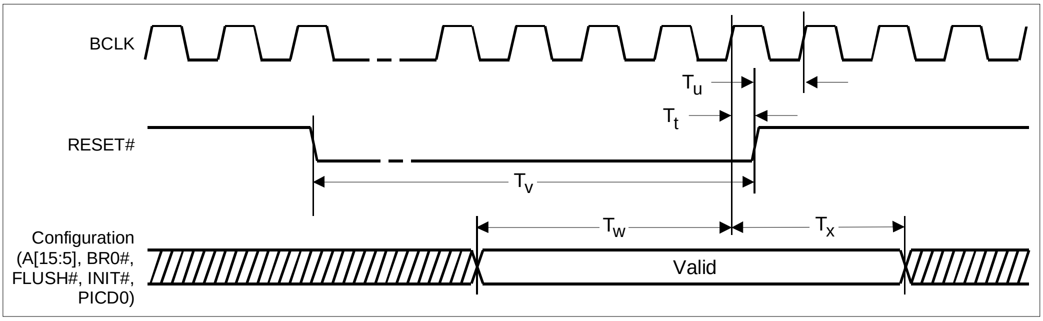

Figure 3.5 Cold/Warm Reset and Configuration Timings

NOTES:

T_t = T9 (Low Power GTL+ Input Hold Time)
T_u = T8 (Low Power GTL+ Input Setup Time)
T_v = T10 (RESET# Pulse Width)
T18 (Reset PLL Lock Latency)
T_w = T16 (Reset Configuration Signals (A[15:5]#, BR0#, FLUSH#, INIT#, PICD0) Setup Time)
T_x = T17 (Reset Configuration Signals (A[15:5]#, BR0#, FLUSH#, INIT#, PICD0) Hold Time)

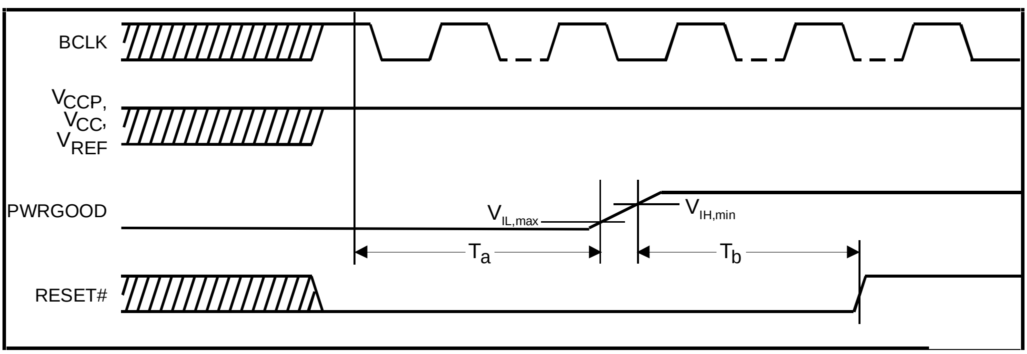

Figure 3.6 Power-On Reset Timings

NOTES:

T_a = T15 (PWRGOOD Inactive Pulse Width)
T_b = T10 (RESET# pulse width)
T18 (Reset PLL Lock Latency)

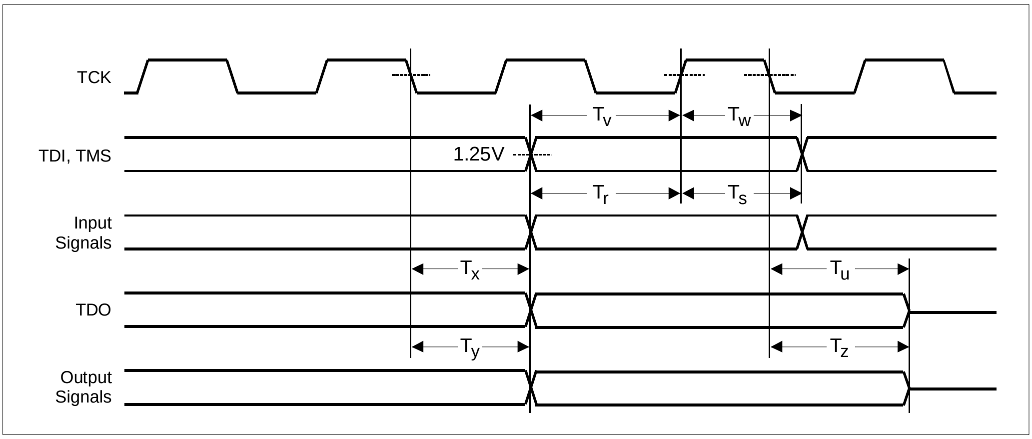

Figure 3.7 Test Timings (Boundary Scan)

NOTES:

T_r = T43 (All Non-Test Inputs Setup Time)
T_s = T44 (All Non-Test Inputs Hold Time)
T_u = T40 (TDO Float Delay)
T_v = T37 (TDI, TMS Setup Time)
T_w = T38 (TDI, TMS Hold Time)
T_x = T39 (TDO Valid Delay)
T_y = T41 (All Non-Test Outputs Valid Delay)
T_z = T42 (All Non-Test Outputs Float Delay)

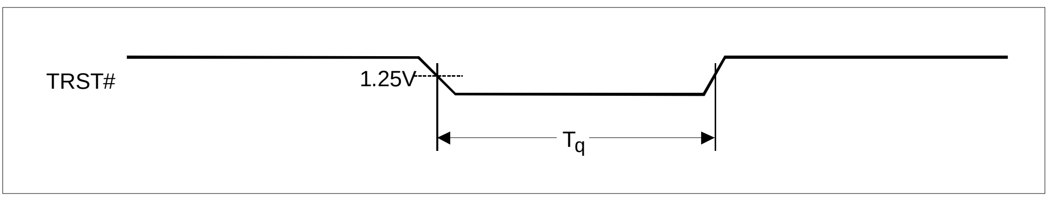

Figure 3.8 Test Reset Timings

NOTE:

T_q = T36 (TRST# Pulse Width)

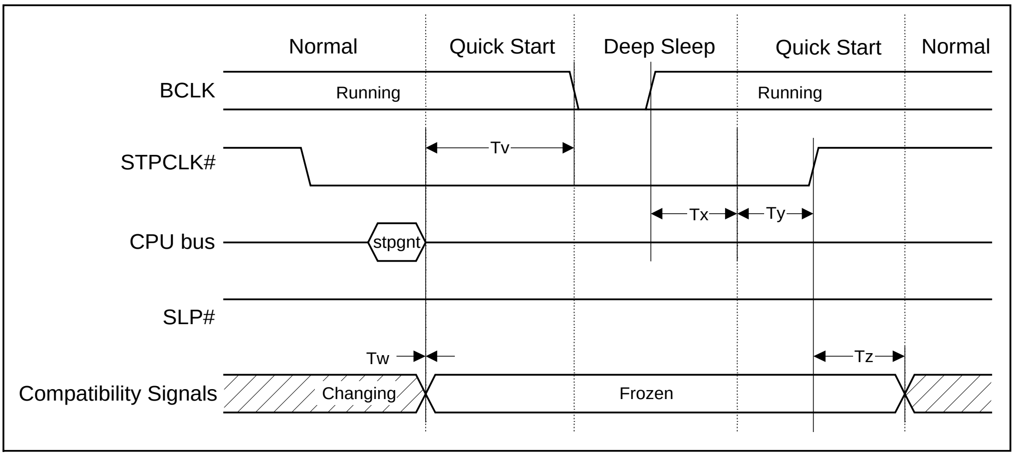

Figure 3.9 Quick Start/Deep Sleep Timing

NOTES:

T_v = T45 (Stop Grant Acknowledge Bus Cycle Completion to Clock Shut Off Delay)
T_w = T46 (Setup Time to Input Signal Hold Requirement)
T_x = T47 (PLL Lock Latency After Clocks Restart)
T_y = T48 (PLL Lock to STPCLK# Hold Time)
T_z = T49 (Input Signal Hold Time)

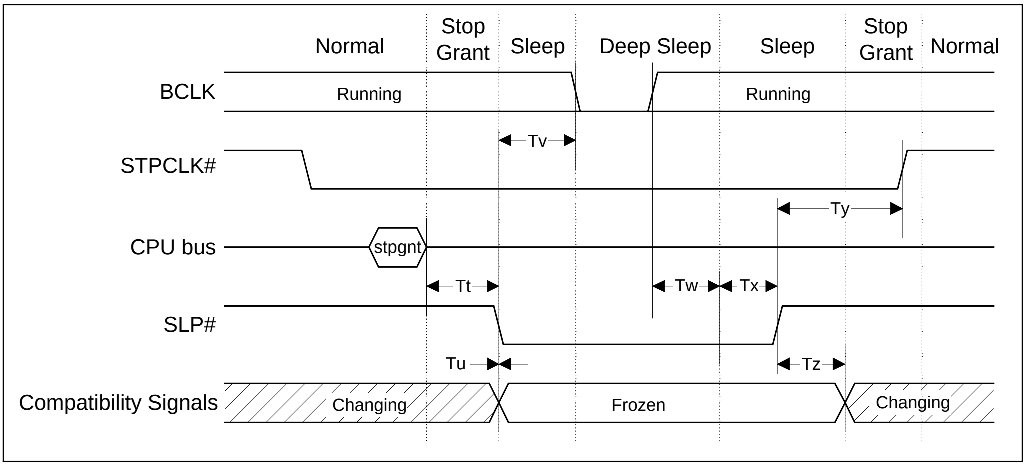

Figure 3.10 Stop Grant/Sleep/Deep Sleep Timing

NOTES:

T_t = T50 (Stop Grant Acknowledge Bus Cycle Completion to SLP# Assertion Delay)
T_u = T51 (Setup Time to Input Signal Hold Requirement)
T_v = T52 (SLP# Assertion to Clock Shut Off Delay)
T_w = T53 (PLL Lock Latency after Clocks Restart)
T_x = T54 (SLP# Hold Time)
T_y = T55 (STPCLK# Hold Time)
T_z = T56 (Input Signal Hold Time)

4. SYSTEM SIGNAL SIMULATIONS

Many scenarios have been simulated to generate a set of Low Power GTL+ layout guidelines which are available in the *Mobile Pentium® II Processor System Bus Layout Guideline.* All waveforms described in this section are simulated at the pad on the processor core. Systems must be simulated using the IBIS model to determine if they are compliant with this specification. A set of signal quality guidelines are also provided. Violations of these guidelines are allowed; but if they occur, then simulations of signal quality at the processor core should be performed to ensure that no violations of the signal quality specifications occur. Meeting the guideline does not guarantee meeting the specification.

4.1. System Bus Clock (BCLK) Signal Quality Specifications

Table 4.1 and Figure 4.1 show the signal quality for the system bus clock (BCLK) signal as simulated at the processor core. Table 4.2 and Figure 4.2 show the signal quality for BCLK as measured at the processor connector. The timings illustrated in Figure 4.2 are taken from Tables 3.8. BCLK is a 2.5V clock.

4.2. Low Power GTL+ Signal Quality Specifications

Table 4.3 and Figure 4.3 illustrate the Low Power GTL+ signal quality specifications for the Mobile Pentium® II processor, simulated at the core. Table 4.4 shows the Low Power GTL+ signal quality guidelines for the Mobile Pentium II processor, measured at the connector. Refer to the *Pentium® II Processor Developer's Manual* for the GTL+ buffer specification.

Table 4.1 BCLK Signal Quality Specifications at the Processor Core

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1	$V_{IL,BCLK}$		0.7	V	4.1	[1]
V2	$V_{IH,BCLK}$	1.8		V	4.1	[1]
V3	V_{IN} Absolute Voltage Range	–0.7	3.5	V	4.1	Undershoot, Overshoot
V4	Rising Edge Ringback	1.8		V	4.1	Absolute Value [2]
V5	Falling Edge Ringback		0.7	V	4.1	Absolute Value [2]
	BCLK rising/falling slew rate	0.8	4.4	V/ns		

NOTES:

1. At the core, BCLK must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,BCLK}$.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits.

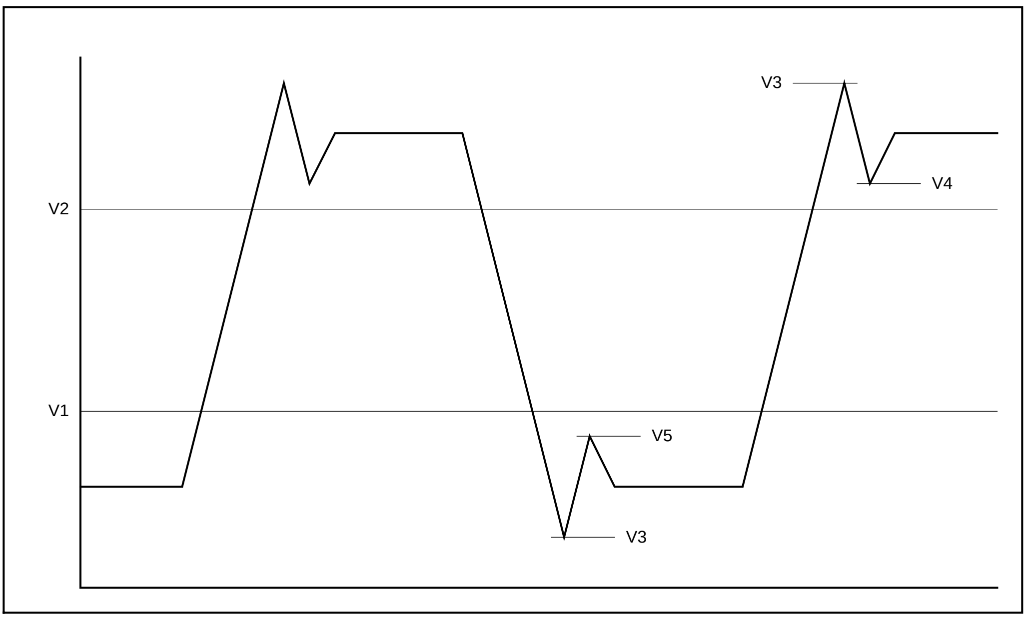

Figure 4.1 BCLK Generic Clock Waveform at the Processor Core

Table 4.2 BCLK Signal Quality Guidelines at the Processor Connector

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V1′	$V_{IL,BCLK}$		0.6	V	4.2	
V2′	$V_{IH,BCLK}$	1.8		V	4.2	
V3′	V_{IN} Absolute Voltage Range	-0.5	3.3	V	4.2	Overshoot, Undershoot
V4′	Rising Edge Ringback	1.8		V	4.2	Absolute Value [1]
V5′	Falling Edge Ringback		0.6	V	4.2	Absolute Value [1]
V6′	T_{line} Ledge Voltage	0.7	1.8	V	4.2	
V7′	T_{line} Ledge Oscillation		0.1	V	4.2	

NOTE:

1. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the $V_{IH,BCLK}$ (rising) or $V_{IL,BCLK}$ (falling) voltage limits.

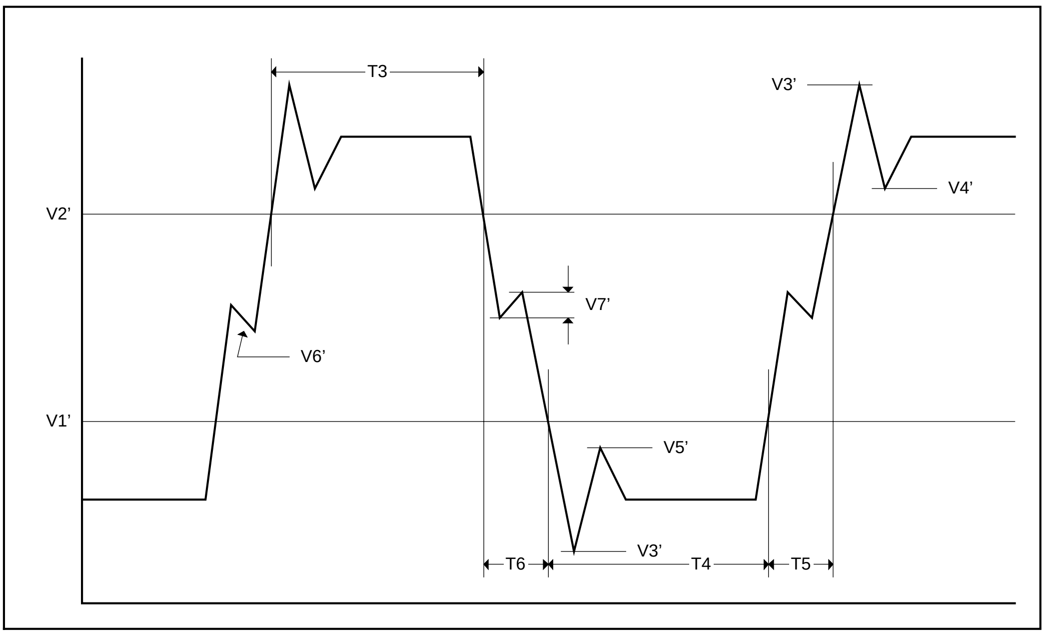

Figure 4.2 BCLK Generic Clock Waveform at the Processor Connector

Table 4.3 Low Power GTL+ Signal Group Ringback Specification at the Processor Core

Symbol	Parameter	Min	Unit	Figure	Notes
α	Overshoot	100	mV	4.3	2, 3
τ	Minimum Time at High	1	ns	4.3	2, 3
ρ	Amplitude of Ringback	-100	mV	4.3	2, 3, 4
ϕ	Final Settling Voltage	100	mV	4.3	2, 3
δ	Duration of Sequential Ringback	N/A	ns	4.3	2, 3

NOTES:

1. Specified for the edge rate of 0.3 – 0.8 V/ns. See Figure 4.3 for the generic waveform.
2. All values determined by design/characterization.
3. Ringback below V_{REF} +100 mV is not authorized during low-to-high transitions. Ringback above V_{REF} -100 mV is not authorized during high-to-low transitions.

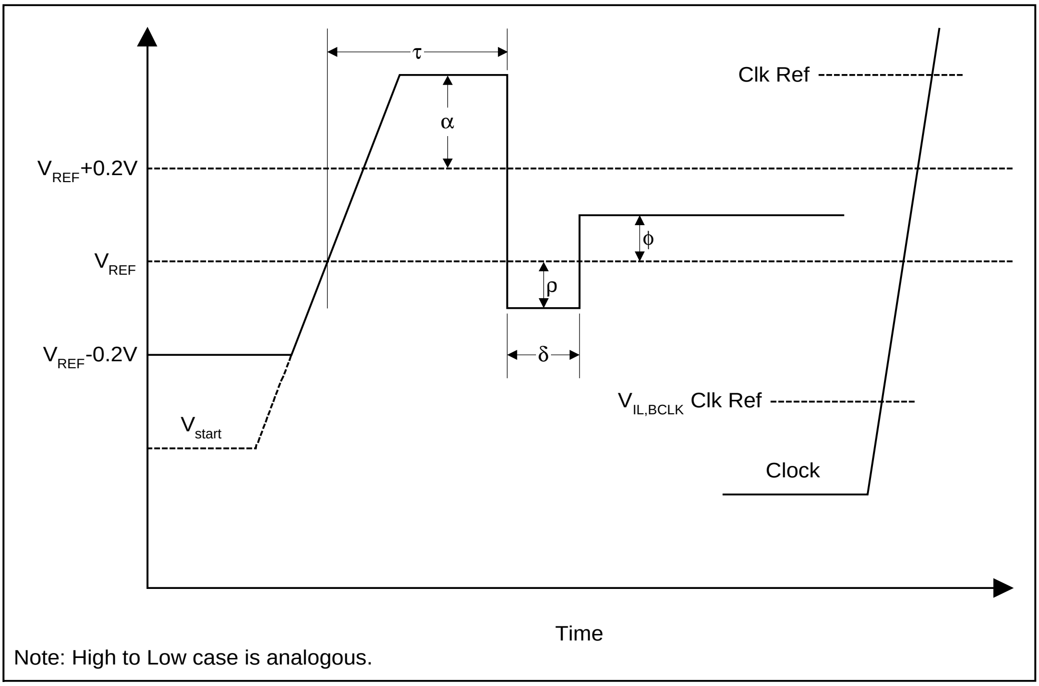

Figure 4.3 Low-to-High, Low Power GTL+ Receiver Ringback Tolerance

Table 4.4 Low Power GTL+ Signal Group Ringback Guideline at the Processor Connector

Symbol	Parameter	Min	Unit	Figure [1]	Notes
α′	Overshoot	100	mV	4.3	2, 3
τ′	Minimum Time at High	1.5	ns	4.3	2, 3
ρ′	Amplitude of Ringback	-250	mV	4.3	2, 3, 4
φ′	Final Settling Voltage	250	mV	4.3	2, 3
δ′	Duration of Sequential Ringback	N/A	ns	4.3	2, 3

NOTES:

1. Greek letter symbols in Figure 4.3 refer to the values in Table 4.3 and Table 4.4.
2. Specified for the edge rate of 0.3 – 0.8 V/ns. See Figure 4.3 for the generic waveform.
3. All values determined by design/characterization.
4. Ringback below V_{REF} +250 mV is not authorized during low-to-high transitions. Ringback above V_{REF} -250 mV is not authorized during high-to-low transitions.

4.3. Non-Low Power GTL+ Signal Quality Specifications

Signals driven on the Mobile Pentium® II processor system bus should meet signal quality specifications to ensure that the components read data properly and that incoming signals do not affect the long term reliability of the component. There are three signal quality parameters defined: overshoot/undershoot, ringback and settling limit. All three signal quality parameters are shown in Figure 4.4 for non-GTL+ signal groups.

4.3.1. OVERSHOOT/UNDERSHOOT GUIDELINES

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot/undershoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. (See Figure 4.4 for non-GTL+ signals.) The processor can be damaged by repeated overshoot events on 2.5V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). However, excessive ringback is the dominant detrimental system timing effect resulting from overshoot/undershoot (i.e., violating the overshoot/ undershoot guideline will make it difficult to satisfy the ringback specification). The overshoot/undershoot guideline is 0.8V and assumes the absence of diodes on the input. These guidelines should be verified in simulations without the on-chip ESD protection diodes present because the diodes will begin clamping the 2.5V tolerant signals beginning at approximately 1.25V above V_{CC} and 0.5V below V_{SS}. If the signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

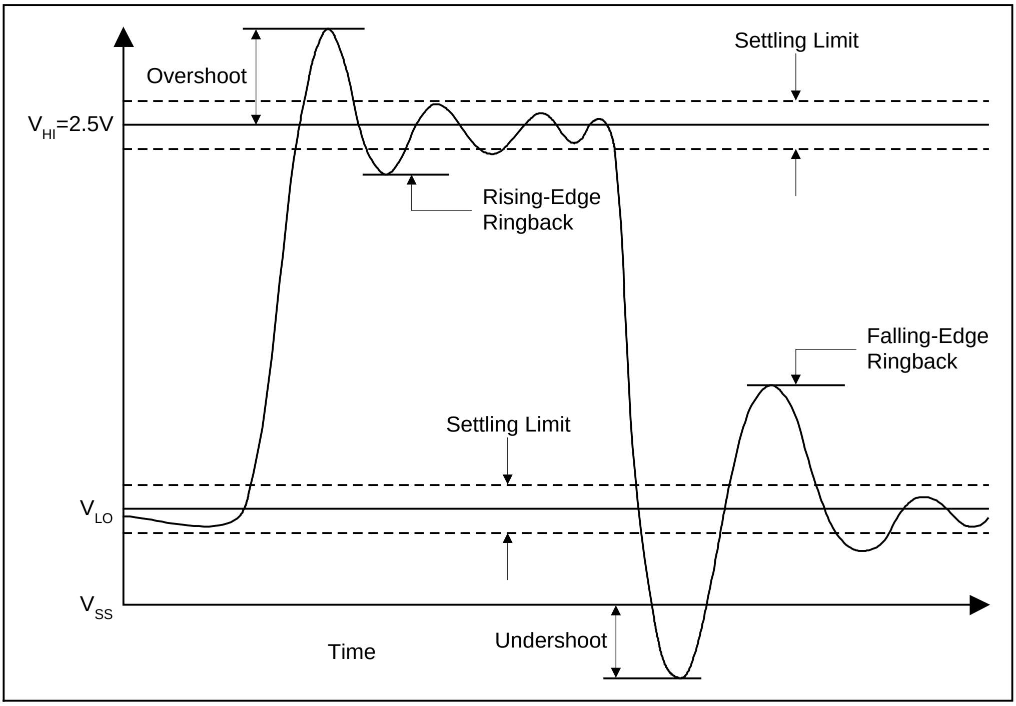

Figure 4.4 Non-GTL+ Overshoot/Undershoot and Ringback

4.3.2. RINGBACK SPECIFICATION

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is the voltage that the signal rings back to after achieving its maximum absolute value. Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal Ringback specification are not allowed under any circumstances for the non-GTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. Table 4.5 and Table 4.6 provide signal ringback specifications for non-GTL+ signals at the processor core and at the processor connector, respectively.

4.3.3. SETTLING LIMIT GUIDELINE

Settling limit defines the maximum amount of ringing at the receiving pin that a signal may reach before its next transition. The amount allowed is 10 percent of the total signal swing (V_{HI}–V_{LO}) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before its next transition.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

Table 4.5 Signal Ringback Specifications for Non-GTL+ Signals at the Processor Core

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Figure
Non-GTL+ Signals	0 → 1	1.7 V	4.4
Non-GTL+ Signals	1 → 0	0.7 V	4.4

Table 4.6 Signal Ringback Guidelines for Non-GTL+ Signals at the Processor Connector

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Figure
Non-GTL+ Signals	0 → 1	1.7 V	4.4
Non-GTL+ Signals	1 → 0	0.7 V	4.4

5. MECHANICAL SPECIFICATIONS

5.1. Connector Mechanical Specifications

The Mobile Pentium® II processor board-to-board stacking connector consists of the plug and the receptacle. The plug surface mounts to the processor and mates to the receptacle, which surface mounts to the motherboard. Each half of the connector uses ball grid array (BGA) technology for surface mount. The processor connector has 240 pins in an 8 x 30 array. A solder ball is attached to the tail of each contact for surface mount and the center-to-center distance between solder balls (pitch) is 1.27 mm.

The plug to be mounted on the processor will be available in one height. The receptacle to be mounted on the motherboard will be available from an outside vendor in two heights to allow for component placement flexibility within the package keepout line on the system electronics. The board-to-board spacing is defined as the spacing between the processor substrate and the system electronics substrate after both halves of the connector are reflowed onto their respective boards and mated. The board-to-board spacing is not to be confused with the bottom clearance which is the space below the cartridge. For the Mobile Pentium II processor the available board-to-board spacings are 3.4 and 4 mm. These spacings are dependent on the height of the receptacle, which is a function of the system manufacturer's mounting technique. The system manufacturer chooses the board-to-board spacing to use for a particular system design.

5.2. Mechanical Specification of the Mobile Pentium® II Processor

The Mobile Pentium® II processor is enclosed by stainless steel (300-series) covers; however, the connector and the processor die are exposed in order to accommodate installation into a system. As shown in Figure 5.1, the overall footprint of the area reserved for the processor is 56.00 mm by 60.00 mm. Note that the bottom cover is metallic, so caution should be taken to prevent shorting when placing components under the processor. Components placed within the package keepout line should not contact the processor. The receptacle and cap outline is shown in Figure 5.1 so that it can be silk screened onto the system electronics substrate, to assist in manual placement of the receptacle. The actual shape of the receptacle and cap assembly is more complicated than a rectangle, but a rectangle is sufficient for the purpose of manual placement. The large and small rectangles in Figure 5.1 show the position of the large and small keys of the connector.

The processor should be securely mounted to the system board to prevent potential damage due to shock and vibration. Four mounting holes are provided in order to facilitate mounting fasteners (M2 screws are recommended) through the processor and into the standoffs on the system board. Due to EMI concerns, a mounting system that provides a low impedance ground between the processor and the system board is recommended.

As noted previously, the processor die is exposed in order to accommodate system thermal interface. Table 5.2 contains the specification for bond-line thickness, which is the distance between the top surface of the die and the top surface of the processor. To facilitate this solution, the top cover is recessed around the die (see Figure 5.3). More information about EMI, mounting, stand-offs and thermal solution attachment is provided in the *Mobile Pentium® II Processor Mini-cartridge Mechanical and Thermal User's Guide*.

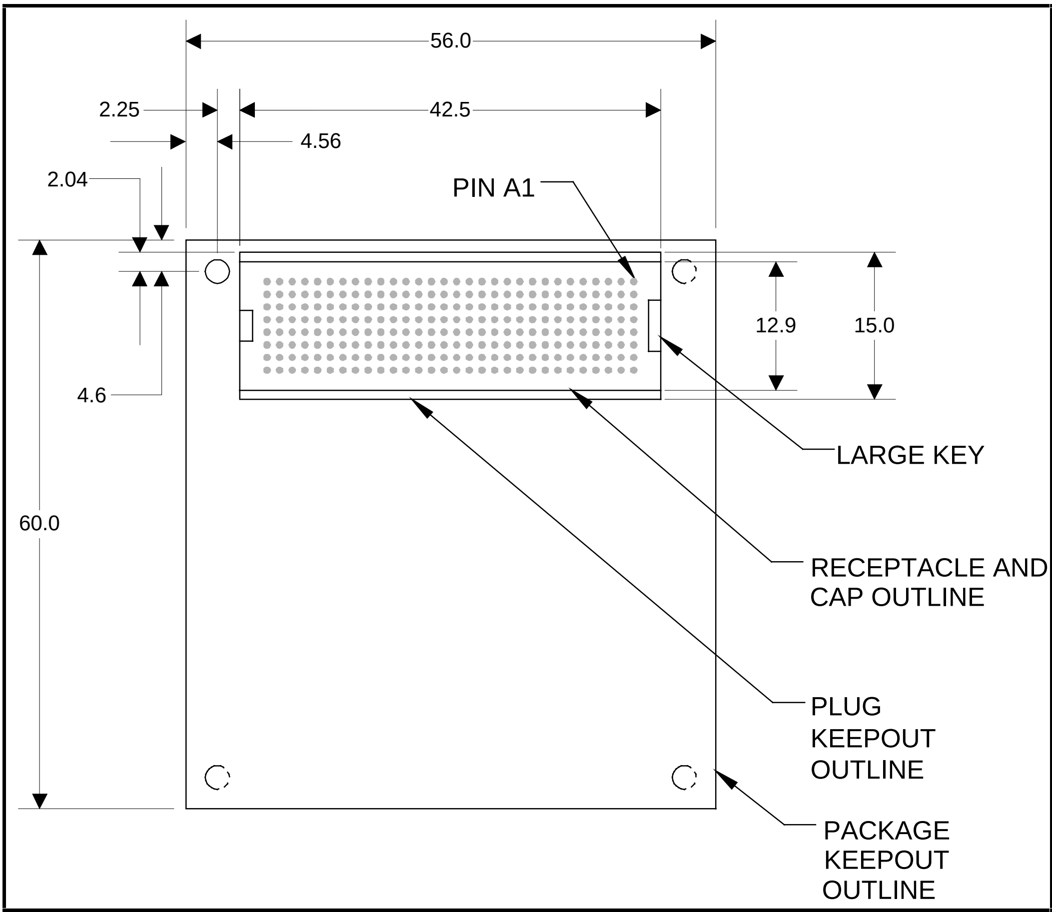

Figure 5.1 Mini-Cartridge Assembly and Connector Keepout Location, Top View (in mm)

It is important that the processor not be disassembled or permanently altered in any way (e.g., adding extra holes) in order to facilitate system thermal solution attachment. Functionality of a processor is not guaranteed if its cover has been removed. The addition of adhesives and greases to the exterior surfaces of the product is not considered to be permanent.

Figure 5.2 shows a cross-sectional view of the Mobile Pentium II processor. Figure 5.3 through Figure 5.5 illustrate the Mobile Pentium® II processor assembly top and bottom cover dimensions and standoff locations.

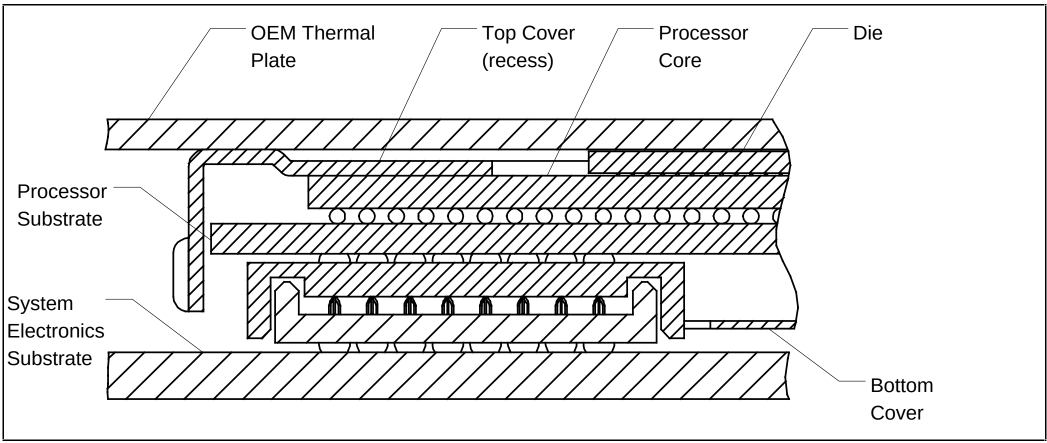

Figure 5.2 Mobile Pentium® II Processor Cross-sectional View

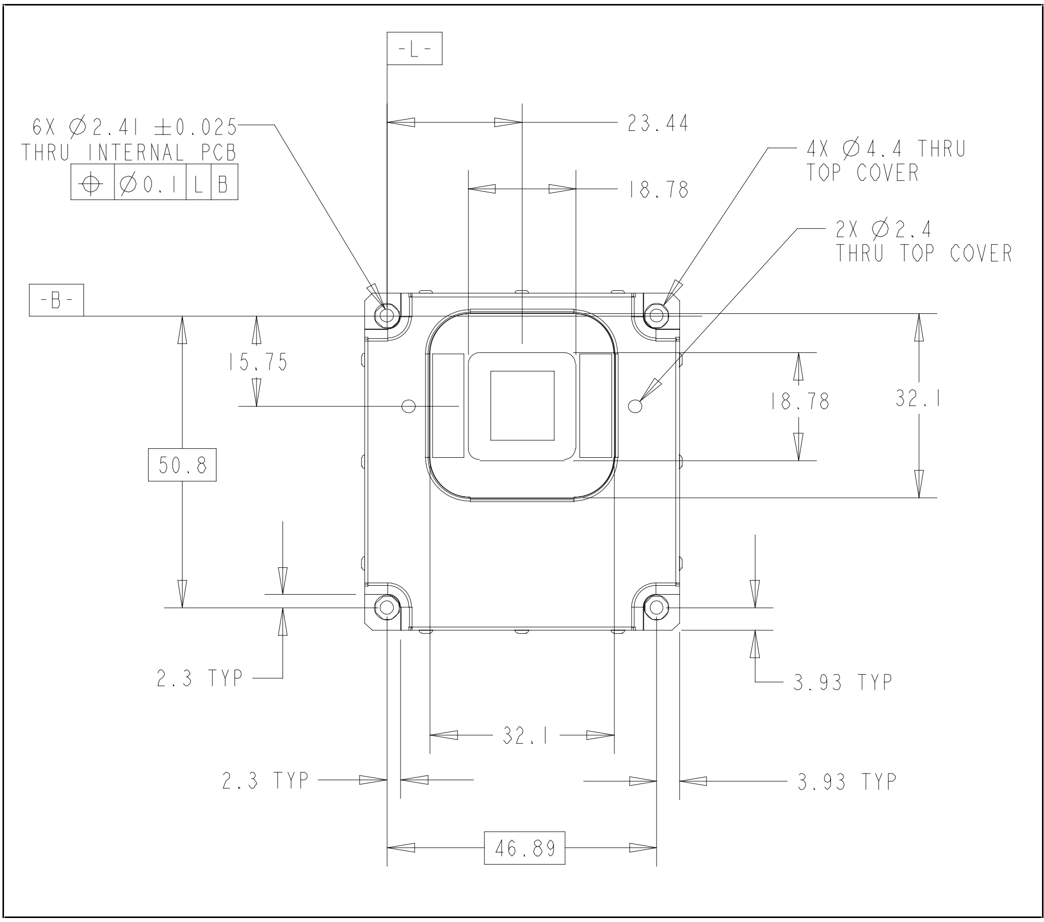

Figure 5.3 Mini-Cartridge Assembly, Top Cover (in mm)

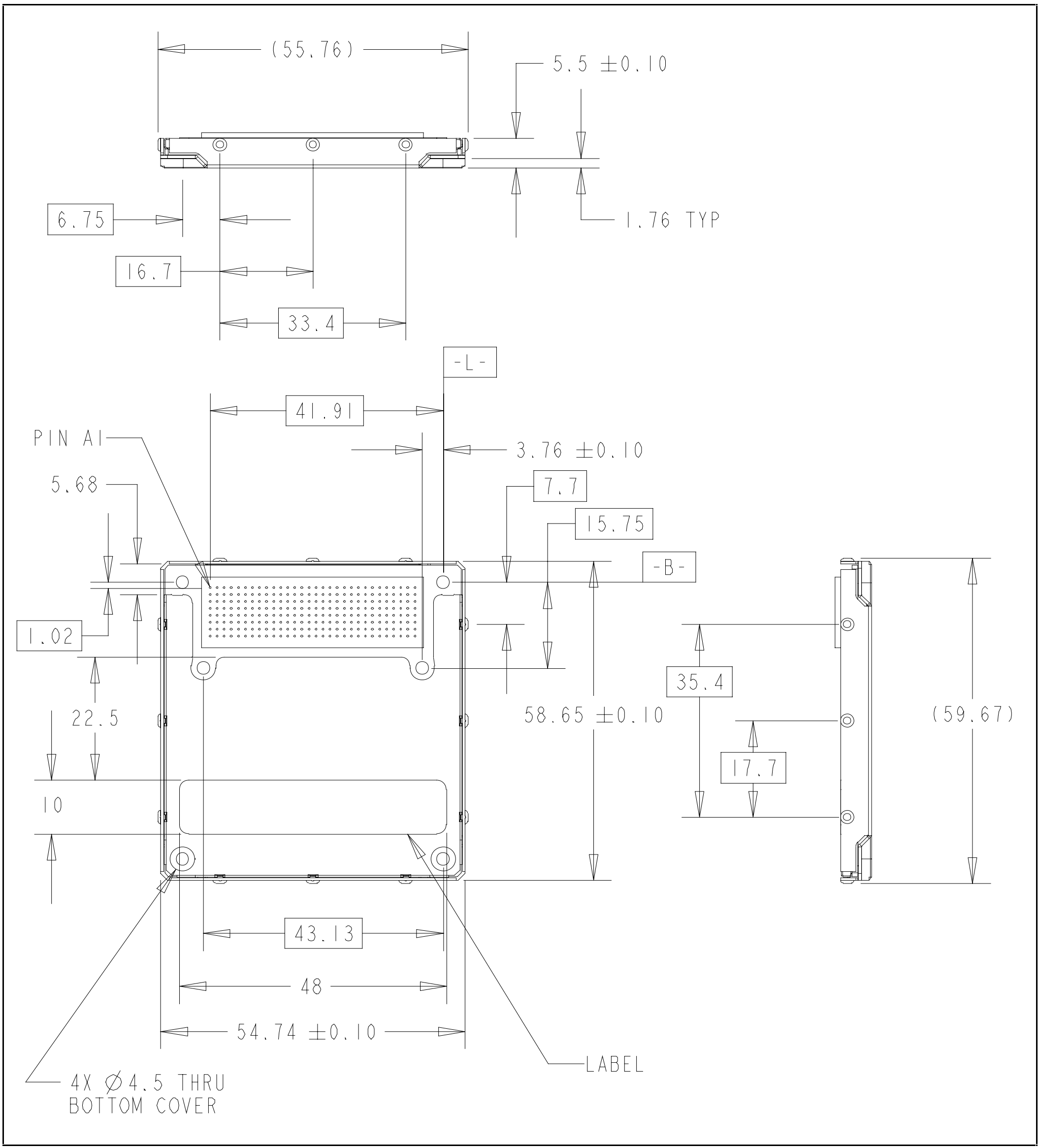

Figure 5.4 Mini-Cartridge Assembly, Bottom Cover and Sides (in mm)

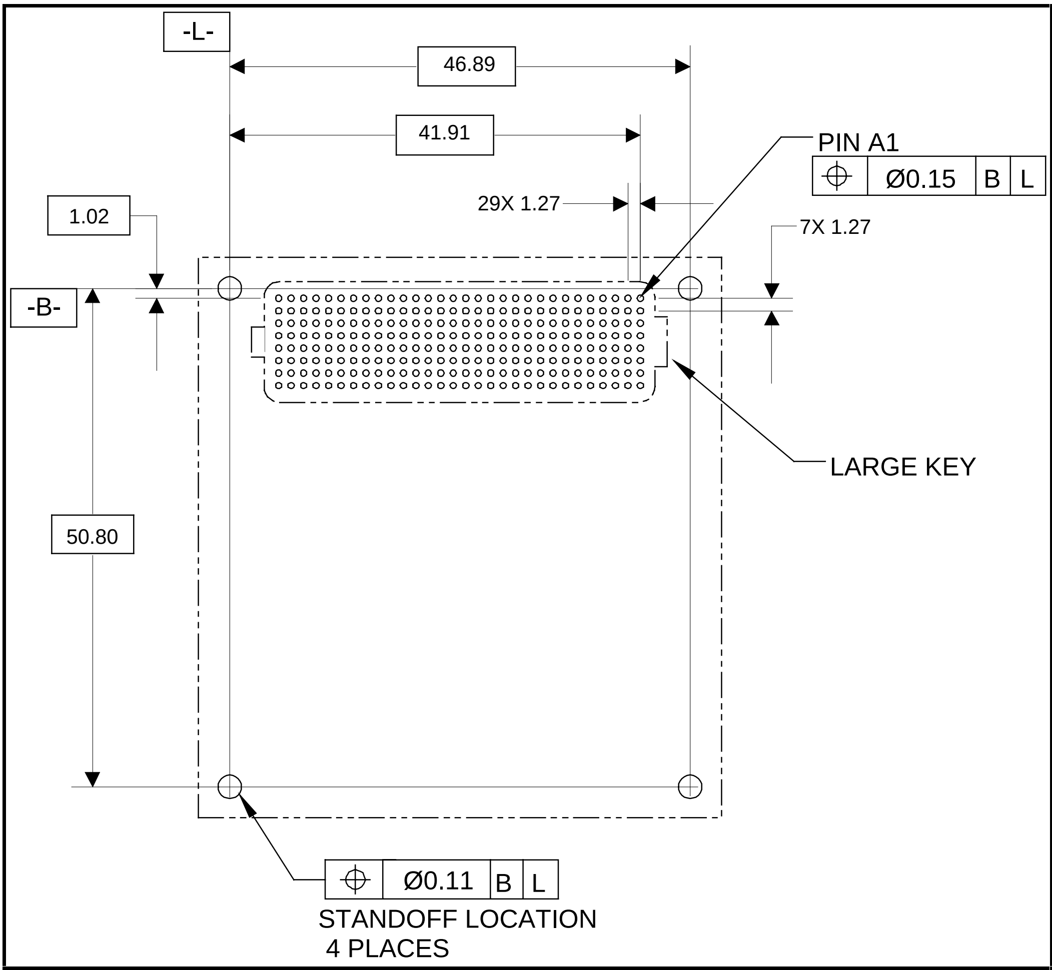

Figure 5.5 Standoff and Connector Location, Top View (in mm)

Table 5.1 Mobile Pentium® II Processor Mechanical Specifications

Symbol	Parameter		Max	Unit	Notes
X,Y_{DIE}	Processor Core Die Dimensions		10.84, 11.97	mm	1, 2
F_{INS}	Processor Insertion Force		133	N	
F_{EXT}	Processor Extraction Force		100	N	
P_{DIE}	Allowable Pressure On Die For Thermal Attach Plate (TAP)		411	kPa	
P_{TOP}	Allowable Pressure on Recessed Part of the Top Cover		411	kPa	
Shock	Mechanical Shock Under Nonoperating Conditions		50	G	Mil Std 810E Method 516
Vibration	Mechanical Vibration Under Nonoperating Conditions	Sine Sweep Random	1.0 3.1	G rms G rms	Mil Std 810E Method 514

NOTES:

1. The long edge of processor core die is parallel to the long edge of the processor enclosure. These distances are approximate and will change from stepping to stepping of the processor core.
2. Die dimensions are approximate and are likely to change.

Table 5.2 Mobile Pentium® II Processor Vertical Dimensions [1,2]

Symbol	Parameter	Min	Nom	Max	Units	Figure
H	Processor Height	4.40	4.55	4.70	mm	5.6
M	Plug Height	0.91	1.03	1.15	mm	5.6
P	Bottom Cover Height[3]		2.81 REF		mm	5.6
BLT	Bond-Line Thickness	0.01	0.12	0.23	mm	5.6

NOTES:

1. See Table 5.3 and Figure 5.6 for the definitions and illustration of processor height, plug height, bottom cover height and bond-line thickness.
2. Processor height, plug height, and bond-line thickness are the only guaranteed vertical dimensions. The other dimensions shown in Figure 5.6 are dependent on the receptacle height. Refer to the *Mobile Pentium® II Processor Mini-cartridge Mechanical and Thermal User's Guide* for information on the effect of receptacle mounting technique on these dimensions.
3. Bottom Cover Height is for reference proposes only.

Table 5.3 defines the Mobile Pentium II processor dimensions illustrated in Figure 5.6. The assembly stack height (SH), board-to-board spacing (BS) and bottom clearance (BC) dimensions are dependent on the receptacle height. Refer to the *Mobile Pentium® II Processor Mini-cartridge Mechanical and Thermal User's Guide* for information on the effect of receptacle mounting technique on these dimensions.

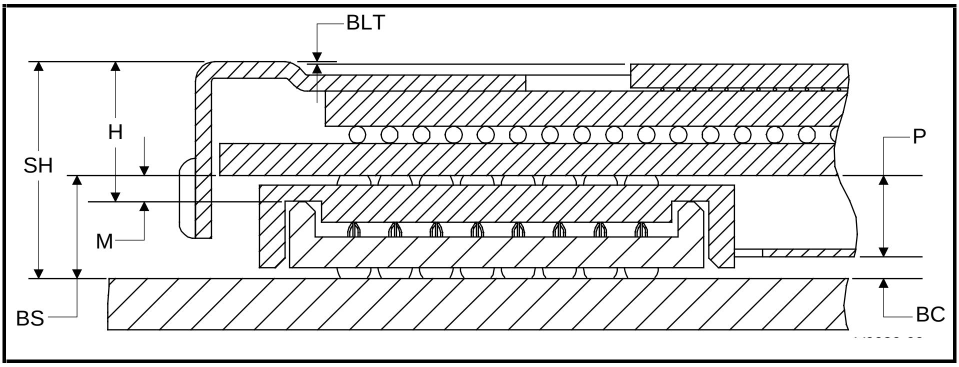

Figure 5.6 Cross Sectional View with Vertical Dimensions

Table 5.3 Mobile Pentium® II Processor Dimension Definitions

Symbol	Parameter	Definition
H	Processor Height	Distance from the top surface of the processor to the mating surface of the plug.
M	Plug Height	Distance from the bottom of the processor substrate to the mating surface of the plug.
P	Bottom Cover Height	Distance from the bottom side of the processor substrate to the bottom outer surface of the processor.
BLT	Bond-Line Thickness	Distance between the top surface of the die and the top surface of the processor.
SH	Assembly Stack Height	Distance from the top surface of the processor to the system electronics substrate.
BS	Board-to-Board Spacing	Distance from the processor substrate to the system electronics substrate.
BC	Bottom Clearance	Distance from the bottom surface of the processor to the system electronics substrate.

5.3. Mobile Pentium® II Processor Pin Lists

Table 5.4 shows the Mobile Pentium® II processor signals by pin location. Table 5.5 lists the signals by pin name.

Table 5.4 Mobile Pentium® II Processor Pinout

	A	B	C	D	E	F	G	H
1	VSS	VCC3	PREQ#	VSS_S	PRDY#	BP2#	BPM0#	VSS
2	VCC3	VCC3	SMBALERT#	VSS	VCC_S	VSS	PICD0	PICCLK
3	BINIT#	BP3#	BPM1#	VID0	VSS	INTR	VSS	VCC
4	VCC	VSS	VCCP_S	D49#	D57#	D55#	DEP6#	VID1
5	VSS	D41#	D42#	VSS	D53#	VSS	D56#	DEP2#
6	D40#	D52#	D45#	D46#	D51#	D62#	D63#	DEP1#
7	D34#	D39#	D47#	D48#	D54#	D59#	D58#	DEP4#
8	VSS	D44#	D36#	VSS	D37#	VSS	D61#	DEP7#
9	D38#	D33#	D35#	D43#	DEP0#	VCC	D60#	DEP3#
10	VCC	D31#	D26#	D27#	D32#	D28#	D50#	DEP5#
11	VSS	D25#	D22#	D19#	D29#	VSS	D30#	VCC
12	D17#	D16#	D20#	D21#	D18#	D24#	PICD1	VSS
13	D14#	D12#	D10#	D15#	D23#	D11#	D13#	VCC
14	VSS	RSVD	D4#	D8#	D9#	D6#	D7#	VSS
15	VID3	D3#	RSVD	D1#	D0#	D5#	D2#	VCC
16	RSVD	RSVD	RSVD	RSVD	PWRGOOD	TRST#	TDO	VSS
17	RSVD	TMS	TDI	SLP#	IGNNE#	TCK	FLUSH#	VCC
18	FERR#	STPCLK#	A20M#	INIT#	RESET#	RS0#	RS1#	VSS
19	IERR#	SMI#	BERR#	VCC	A35#	A33#	RP#	VCC
20	VSS	A32#	A34#	VSS	A29#	VSS	VCC	VSS
21	VCC	A26#	A30#	A31#	A25#	BPRI#	A3#	BNR#
22	A24#	A27#	A22#	A15#	RSVD	VCC	A5#	REQ2#
23	VSS	A28#	A23#	VSS	LOCK#	VSS	A6#	REQ0#
24	A20#	A21#	VSS	A17#	A13#	A10#	A9#	RSVD
25	VCC	A19#	REQ4#	A16#	A11#	A8#	A4#	ADS#
26	VSS	VSS	RSP#	VSS	A12#	VSS	TRDY#	DEFER#
27	DBSY#	VCC	VCC	A18#	A14#	A7#	RSVD	REQ1#
28	REQ3#	AERR#	VSS	DRDY#	VSS	RS2#	VCC	VCC
29	AP0#	SMBDATA	VID2	VSS	BR0#	VSS	BCLK	VCCP
30	VSS	SMBCLK	NMI	AP1#	HITM#	HIT#	VCCP	VSS

Table 5.5 Mobile Pentium® II Processor Pin Listing

Pin Name	Pin	Signal Type	Pin Name	Pin	Signal Type
A3#	G21	Low Power GTL+ I/O	A32#	B20	Low Power GTL+ I/O
A4#	G25	Low Power GTL+ I/O	A33#	F19	Low Power GTL+ I/O
A5#	G22	Low Power GTL+ I/O	A34#	C20	Low Power GTL+ I/O
A6#	G23	Low Power GTL+ I/O	A35#	E19	Low Power GTL+ I/O
A7#	F27	Low Power GTL+ I/O	A20M#	C18	CMOS Input
A8#	F25	Low Power GTL+ I/O	ADS#	H25	Low Power GTL+ I/O
A9#	G24	Low Power GTL+ I/O	AERR#	B28	Low Power GTL+ I/O
A10#	F24	Low Power GTL+ I/O	AP0#	A29	Low Power GTL+ I/O
A11#	E25	Low Power GTL+ I/O	AP1#	D30	Low Power GTL+ I/O
A12#	E26	Low Power GTL+ I/O	BCLK	G29	System Bus Clock
A13#	E24	Low Power GTL+ I/O	BERR#	C19	Low Power GTL+ I/O
A14#	E27	Low Power GTL+ I/O	BINIT#	A3	Low Power GTL+ I/O
A15#	D22	Low Power GTL+ I/O	BNR#	H21	Low Power GTL+ I/O
A16#	D25	Low Power GTL+ I/O	BP2#	F1	Low Power GTL+ I/O
A17#	D24	Low Power GTL+ I/O	BP3#	B3	Low Power GTL+ I/O
A18#	D27	Low Power GTL+ I/O	BPM0#	G1	Low Power GTL+ I/O
A19#	B25	Low Power GTL+ I/O	BPM1#	C3	Low Power GTL+ I/O
A20#	A24	Low Power GTL+ I/O	BPRI#	F21	Low Power GTL+ Input
A21#	B24	Low Power GTL+ I/O	BR0#	E29	Low Power GTL+ I/O
A22#	C22	Low Power GTL+ I/O	D0#	E15	Low Power GTL+ I/O
A23#	C23	Low Power GTL+ I/O	D1#	D15	Low Power GTL+ I/O
A24#	A22	Low Power GTL+ I/O	D2#	G15	Low Power GTL+ I/O
A25#	E21	Low Power GTL+ I/O	D3#	B15	Low Power GTL+ I/O
A26#	B21	Low Power GTL+ I/O	D4#	C14	Low Power GTL+ I/O
A27#	B22	Low Power GTL+ I/O	D5#	F15	Low Power GTL+ I/O
A28#	B23	Low Power GTL+ I/O	D6#	F14	Low Power GTL+ I/O
A29#	E20	Low Power GTL+ I/O	D7#	G14	Low Power GTL+ I/O
A30#	C21	Low Power GTL+ I/O	D8#	D14	Low Power GTL+ I/O
A31#	D21	Low Power GTL+ I/O	D9#	E14	Low Power GTL+ I/O

Table 5.5 Mobile Pentium® II Processor Pin Listing (Continued)

Pin Name	Pin	Signal Type	Pin Name	Pin	Signal Type
D10#	C13	Low Power GTL+ I/O	D40#	A6	Low Power GTL+ I/O
D11#	F13	Low Power GTL+ I/O	D41#	B5	Low Power GTL+ I/O
D12#	B13	Low Power GTL+ I/O	D42#	C5	Low Power GTL+ I/O
D13#	G13	Low Power GTL+ I/O	D43#	D9	Low Power GTL+ I/O
D14#	A13	Low Power GTL+ I/O	D44#	B8	Low Power GTL+ I/O
D15#	D13	Low Power GTL+ I/O	D45#	C6	Low Power GTL+ I/O
D16#	B12	Low Power GTL+ I/O	D46#	D6	Low Power GTL+ I/O
D17#	A12	Low Power GTL+ I/O	D47#	C7	Low Power GTL+ I/O
D18#	E12	Low Power GTL+ I/O	D48#	D7	Low Power GTL+ I/O
D19#	D11	Low Power GTL+ I/O	D49#	D4	Low Power GTL+ I/O
D20#	C12	Low Power GTL+ I/O	D50#	G10	Low Power GTL+ I/O
D21#	D12	Low Power GTL+ I/O	D51#	E6	Low Power GTL+ I/O
D22#	C11	Low Power GTL+ I/O	D52#	B6	Low Power GTL+ I/O
D23#	E13	Low Power GTL+ I/O	D53#	E5	Low Power GTL+ I/O
D24#	F12	Low Power GTL+ I/O	D54#	E7	Low Power GTL+ I/O
D25#	B11	Low Power GTL+ I/O	D55#	F4	Low Power GTL+ I/O
D26#	C10	Low Power GTL+ I/O	D56#	G5	Low Power GTL+ I/O
D27#	D10	Low Power GTL+ I/O	D57#	E4	Low Power GTL+ I/O
D28#	F10	Low Power GTL+ I/O	D58#	G7	Low Power GTL+ I/O
D29#	E11	Low Power GTL+ I/O	D59#	F7	Low Power GTL+ I/O
D30#	G11	Low Power GTL+ I/O	D60#	G9	Low Power GTL+ I/O
D31#	B10	Low Power GTL+ I/O	D61#	G8	Low Power GTL+ I/O
D32#	E10	Low Power GTL+ I/O	D62#	F6	Low Power GTL+ I/O
D33#	B9	Low Power GTL+ I/O	D63#	G6	Low Power GTL+ I/O
D34#	A7	Low Power GTL+ I/O	DBSY#	A27	Low Power GTL+ I/O
D35#	C9	Low Power GTL+ I/O	DEFER#	H26	Low Power GTL+ Input
D36#	C8	Low Power GTL+ I/O	DEP0#	E9	Low Power GTL+ I/O
D37#	E8	Low Power GTL+ I/O	DEP1#	H6	Low Power GTL+ I/O
D38#	A9	Low Power GTL+ I/O	DEP2#	H5	Low Power GTL+ I/O
D39#	B7	Low Power GTL+ I/O	DEP3#	H9	Low Power GTL+ I/O

Table 5.5 Mobile Pentium® II Processor Pin Listing (Continued)

Pin Name	Pin	Signal Type	Pin Name	Pin	Signal Type
DEP4#	H7	Low Power GTL+ I/O	RSP#	C26	Low Power GTL+ Input
DEP5#	H10	Low Power GTL+ I/O	RSVD	A16	Reserved
DEP6#	G4	Low Power GTL+ I/O	RSVD	A17	Reserved
DEP7#	H8	Low Power GTL+ I/O	RSVD	B14	Reserved
DRDY#	D28	Low Power GTL+ I/O	RSVD	B16	Reserved
FERR#	A18	CMOS Output	RSVD	C15	Reserved
FLUSH#	G17	CMOS Input	RSVD	C16	Reserved
HIT#	F30	Low Power GTL+ I/O	RSVD	D16	Reserved
HITM#	E30	Low Power GTL+ I/O	RSVD	E22	Reserved
IERR#	A19	CMOS Output	RSVD	G27	Reserved
IGNNE#	E17	CMOS Input	RSVD	H24	Reserved
INIT#	D18	CMOS Input	SLP#	D17	CMOS Input
INTR	F3	CMOS Input	SMBALERT#	C2	Thermal Alert
LOCK#	E23	Low Power GTL+ I/O	SMBCLK	B30	SMBus Clock
NMI	C30	CMOS Input	SMBDATA	B29	SMBus I/O
PICCLK	H2	APIC Clock Input	SMI#	B19	CMOS Input
PICD0	G2	CMOS I/O	STPCLK#	B18	CMOS Input
PICD1	G12	CMOS I/O	TCK	F17	TAP Clock Input
PRDY#	E1	Low Power GTL+ Output	TDI	C17	TAP Input
PREQ#	C1	CMOS Input	TDO	G16	TAP Output
PWRGOOD	E16	CMOS Input	TMS	B17	TAP Input
REQ0#	H23	Low Power GTL+ I/O	TRDY#	G26	Low Power GTL+ Input
REQ1#	H27	Low Power GTL+ I/O	TRST#	F16	TAP Input
REQ2#	H22	Low Power GTL+ I/O	VCC	A4	Core V_{CC}
REQ3#	A28	Low Power GTL+ I/O	VCC	A10	Core V_{CC}
REQ4#	C25	Low Power GTL+ I/O	VCC	A21	Core V_{CC}
RESET#	E18	Low Power GTL+ Input	VCC	A25	Core V_{CC}
RP#	G19	Low Power GTL+ I/O	VCC	B27	Core V_{CC}
RS0#	F18	Low Power GTL+ Input	VCC	C27	Core V_{CC}
RS1#	G18	Low Power GTL+ Input	VCC	D19	Core V_{CC}
RS2#	F28	Low Power GTL+ Input	VCC	F9	Core V_{CC}

Table 5.5 Mobile Pentium® II Processor Pin Listing (Continued)

Pin Name	Pin	Signal Type	Pin Name	Pin	Signal Type
VCC	F22	Core V_{CC}	VSS	B4	Ground
VCC	G20	Core V_{CC}	VSS	B26	Ground
VCC	G28	Core V_{CC}	VSS	C24	Ground
VCC	H3	Core V_{CC}	VSS	C28	Ground
VCC	H11	Core V_{CC}	VSS	D2	Ground
VCC	H13	Core V_{CC}	VSS	D5	Ground
VCC	H15	Core V_{CC}	VSS	D8	Ground
VCC	H17	Core V_{CC}	VSS	D20	Ground
VCC	H19	Core V_{CC}	VSS	D23	Ground
VCC	H28	Core V_{CC}	VSS	D26	Ground
VCC_S	E2	Core V_{CC} Sense	VSS	D29	Ground
VCC3	A2	Cache Core V_{CC}	VSS	E3	Ground
VCC3	B1	Cache Core V_{CC}	VSS	E28	Ground
VCC3	B2	Cache Core V_{CC}	VSS	F2	Ground
VCCP	G30	Cache I/O V_{CC}	VSS	F5	Ground
VCCP	H29	Cache I/O V_{CC}	VSS	F8	Ground
VCCP_S	C4	Cache I/O V_{CC} Sense	VSS	F11	Ground
VID0	D3	Voltage Identification	VSS	F20	Ground
VID1	H4	Voltage Identification	VSS	F23	Ground
VID2	C29	Voltage Identification	VSS	F26	Ground
VID3	A15	Voltage Identification	VSS	F29	Ground
VSS	A1	Ground	VSS	G3	Ground
VSS	A5	Ground	VSS	H1	Ground
VSS	A8	Ground	VSS	H12	Ground
VSS	A11	Ground	VSS	H14	Ground
VSS	A14	Ground	VSS	H16	Ground
VSS	A20	Ground	VSS	H18	Ground
VSS	A23	Ground	VSS	H20	Ground
VSS	A26	Ground	VSS	H30	Ground
VSS	A30	Ground	VSS_S	D1	Ground Sense

6. THERMAL SPECIFICATIONS

The Mobile Pentium® II processor contains an enclosure which allows for a number of different thermal management solutions for the system manufacturer. This section contains the thermal characteristics of the processor.

In order to achieve proper cooling of the processor, a thermal solution (e.g., heat spreader, heat pipe, or other heat transfer system) must be securely attached to the processor's top cover. Since the processor die is exposed, all thermal solutions must attach to the top cover and the exposed die of the processor. The processor die must be clean before the thermal solution is attached or the processor may be damaged.

During all operational environments, the processor core temperature, T_{PROC}, must be within the range of 0 °C to 100 °C. The thermal sensor can be used to measure the processor core temperature. See Section 3.1.4 for a description of the thermal sensor. The thermal sensor measures the temperature of the processor core with an accuracy of ±3 °C. Note that this measurement is not 100% tested and is specified by design/characterization.

Table 6.1 Mobile Pentium® II Processor Power Specifications

Symbol	Parameter		Typ[1]	Max	Unit	Notes
TDP_{PROC}	Thermal Design Power (Processor)	@ 300 MHz @ 266 MHz @ 233 MHz	—	11.6 10.3 9.0	W W W	Processor (core & L2 cache)[2]
TDP_{TT}	Thermal Transfer Power	@ 300 MHz @ 266 MHz @ 233 MHz	—	N/A N/A N/A	W W W	Core only
P_{SGNT}	Stop Grant and Auto Halt power			1.2	W	Processor, at 50°C
P_{QS}	Quick Start and Sleep power			500	mW	Processor, at 50°C
P_{DSLP}	Deep Sleep power			100	mW	Processor, at 50°C[3]

NOTES:

1. $TDP_{PROC,TYP}$ and $TDP_{TT,TYP}$ are recommendations based on the power dissipation of the processor and processor core, respectively, while executing publicly-available software under normal operating conditions at nominal voltages. Contact your Intel Field Sales Representative for further information.
2. $TDP_{PROC,MAX}$ is a specification of the total power dissipation of the processor while executing a worst-case instruction mix under normal operating conditions at nominal voltages. It includes the power dissipated by all of the components within the processor. Not 100% tested. Specified by design/characterization.
3. Not 100% tested or guaranteed. The Deep Sleep power specification is composed of the leakage current of the various components of the processor on the V_{CC}, V_{CCP} and V_{CC3} voltage planes. These leakages are measured and specified at high temperatures. This 50 °C Deep Sleep power specification is determined by characterization of the component leakage currents at higher temperatures.

7. PROCESSOR INITIALIZATION AND CONFIGURATION

7.1. Description

The Mobile Pentium® II processor has some configuration options that are determined by hardware and some that are determined by software. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET#. Most of the configuration options for the Mobile Pentium II processor are identical to those of the Pentium II processor. The *Pentium® II Processor Developer's Manual* describes these configuration options. New configuration options for the Mobile Pentium II processor are described in the remainder of this section.

7.1.1. QUICK START ENABLE

The processor normally enters the Stop Grant state when the STPCLK# signal is asserted but it will enter the Quick Start state instead if A15# is sampled active on the RESET# signal's active-to-inactive transition. The Quick Start state supports snoops from the bus priority device like the Stop Grant state but it does not support symmetric master snoops nor is the latching of interrupts supported. A '1' in bit position 5 of the Power-On Configuration register indicates that the Quick Start state has been enabled.

7.1.2. SYSTEM BUS FREQUENCY

The current generation Mobile Pentium® II processor will only function with a system bus frequency of 66 MHz. Bit position 19 of the Power-On Configuration register indicates at which speed a processor will run. A '0' in bit 19 indicates a 66-MHz bus frequency and a '1' indicates a 100-MHz bus frequency.

7.1.3. APIC ENABLE

If the PICD0 pin is sampled low on the active-to-inactive transition of the RESET# signal then the PICCLK pin can be tied to V_{SS}. Otherwise the PICD[1:0] pins must be pulled up to 2.5V and PICCLK must be supplied. Driving PICD0 low at reset also has the effect of clearing the APIC Global Enable bit in the APIC Base MSR. This bit is normally set when the processor is reset, but when it is cleared the APIC is completely disabled until the next reset.

7.2. Clock Frequencies and Ratios

The Mobile Pentium® II processor uses a clock design in which the bus clock is multiplied by a ratio to produce the processor's internal (or "core") clock. The ratio used is programmed into the processor when it is manufactured.

APPENDIX A. SIGNAL REFERENCE

A.1 Alphabetical Signal Reference

A[35:3]# (I/O - Low Power GTL+)

The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction information. These signals must be connected to the appropriate pins of both agents on the Mobile Pentium® II processor system bus. The A[35:24]# signals are protected with the AP1# parity signal, and the A[23:3]# signals are protected with the AP0# parity signal.

On the active-to-inactive transition of RESET#, each processor bus agent samples A[35:3]# signals to determine its power-on configuration. See Section 8 for details.

A20M# (I - 2.5V tolerant)

If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.

A20M# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, A20M# must be valid with the TRDY# assertion of the corresponding I/O Write bus transaction.

ADS# (I/O - Low Power GTL+)

The ADS# (Address Strobe) signal is asserted to indicate the validity of a transaction address on the A[35:3]# pins. Both bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus.

AERR# (I/O - Low Power GTL+)

The AERR# (Address Parity Error) signal is observed and driven by both Mobile Pentium® II processor system bus agents, and if used, must be connected to the appropriate pins of both agents on the Mobile Pentium II processor system bus. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction.

If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.

AP[1:0]# (I/O - Low Power GTL+)

The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]# and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should be connected to the appropriate pins on both agents on the Mobile Pentium II processor system bus.

BCLK (I - 2.5V tolerant)

The BCLK (Bus Clock) signal determines the system bus frequency. Both Mobile Pentium® II processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge.

All external timing parameters are specified with respect to the BCLK signal.

BERR# (I/O - Low Power GTL+)

The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by either Mobile Pentium II processor system bus agents, and must be connected to the appropriate pins of both agents, if used. However, Mobile Pentium® II processors do not observe assertions of the BERR# signal.

BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:

- Enabled or disabled
- Asserted optionally for internal errors along with IERR#
- Asserted optionally by the request initiator of a bus transaction after it observes an error
- Asserted by any bus agent when it observes an error in a bus transaction

BINIT# (I/O - Low Power GTL+)

The BINIT# (Bus Initialization) signal may be observed and driven by both Mobile Pentium® II processor system bus agents, and must be connected to the appropriate pins of both agents, if used. If the BINIT# driver is enabled during the power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

If BINIT# is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the Machine Check Architecture (MCA) of the system.

BNR# (I/O - Low Power GTL+)

The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent that is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents may need to request a bus stall simultaneously, BNR# is a wired-OR signal which must be connected to the appropriate pins of both agents on the Mobile Pentium® II processor system bus. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.

BP[3:2]# (I/O - Low Power GTL+)

The BP[3:2]# (Breakpoint) signals are the System Support group Breakpoint signals. They are outputs from the processor that indicate the status of breakpoints.

BPM[1:0]# (I/O - Low Power GTL+)

The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.

BPRI# (I - Low Power GTL+)

The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the Mobile Pentium® II processor system bus. It must be connected to the appropriate pins on both agents on the system bus. Observing BPRI# active (as asserted by the priority agent) causes the processor to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, and then releases the bus by deasserting BPRI#.

BR0# (I/O - Low Power GTL+)

The BR0# (Bus Request) signal is the processor Arbitration Bus signal. The Mobile Pentium® II processor indicates that it wants ownership of the system bus by asserting the BR0# signal.

During power-up configuration, the central agent must assert the BR0# bus signal. The processor samples BR0# on the active-to-inactive transition of RESET#.

D[63:0]# (I/O - Low Power GTL+)

The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between both Mobile Pentium® II processor system bus agents, and must be connected to the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

DBSY# (I/O - Low Power GTL+)

The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the Mobile Pentium II processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must be connected to the appropriate pins on both agents on the system bus.

DEFER# (I - Low Power GTL+)

The DEFER# (Defer) signal is asserted by an agent to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. This signal must be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus.

DEP[7:0]# (I/O - Low Power GTL+)

The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus if they are used. During power-on configuration, DEP[7:0]# signals can be enabled for ECC checking or disabled for no checking.

DRDY# (I/O - Low Power GTL+)

The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# can be deasserted to insert idle clocks. This signal must be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus.

FERR# (O - 2.5V tolerant open-drain)

The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel387 coprocessor, and is included for compatibility with systems using DOS-type floating-point error reporting.

FLUSH# (I - 2.5V tolerant)

When the FLUSH# (Flush) input signal is asserted, the processor writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the processor issues a Flush Acknowledge transaction to. The processor stops caching any new data while the FLUSH# signal remains asserted.

FLUSH# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, FLUSH# must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.

On the active-to-inactive transition of RESET#, each processor bus agent samples FLUSH# to determine its power-on configuration.

HIT# (I/O - Low Power GTL+),
HITM# (I/O - Low Power GTL+)

The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus. Either bus agent can assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

IERR# (O - 2.5V tolerant open-drain)

The IERR# (Internal Error) signal is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the Mobile Pentium® II processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until it is handled in software or with the assertion of RESET#, BINIT or INIT#.

IGNNE# (I - 2.5V tolerant)

The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor freezes on a non-control floating-point instruction if a previous instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set.

IGNNE# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, IGNNE# must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.

INIT# (I - 2.5V tolerant)

The INIT# (Initialization) signal is asserted to reset integer registers inside the processor without affecting the internal (L1 or L2) caches or the floating-point registers. The processor begins execution at the power-on reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous input.

If INIT# is sampled active on RESET#'s active-to-inactive transition, then the processor executes its built-in self test (BIST).

INTR (I - 2.5V tolerant)

The INTR (Interrupt) signal indicates that an external interrupt has been generated. INTR becomes the LINT0 signal when the APIC is enabled. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the processor vectors to the interrupt handler after completing the current instruction execution. Upon recognizing the interrupt request, the processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.

INTR is sampled on every rising BCLK edge. INTR is an asynchronous input but recognition of INTR is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. INTR must be deasserted for a minimum of two clocks to guarantee its inactive recognition. If APIC is enabled at Reset, then LINT[1:0] is the default configuration.

LINT[1:0] (I - 2.5V tolerant)

The LINT[1:0] (Local APIC Interrupt) signals must be connected to the appropriate pins of all APIC bus agents, including the processor and the core logic or I/O APIC component. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs.

Both of these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. If the APIC is enabled at reset, then LINT[1:0] is the default configuration.

LOCK# (I/O - Low Power GTL+)

The LOCK# (Lock) signal indicates to the system that a sequence of transactions must occur atomically. This signal must be connected to the appropriate pins on both agents on the Mobile Pentium II processor system bus. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction through the end of the last transaction.

When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables the processor to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock.

NMI (I - 2.5V tolerant)

The NMI (Non-Maskable Interrupt) indicates that an external interrupt has been generated. NMI becomes the LINT1 signal when the APIC is enabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending.

NMI is rising-edge sensitive. Recognition of NMI is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. If asserted asynchronously, active and inactive pulse widths must be a minimum of two clocks.

PICCLK (I - 2.5V tolerant)

The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC that is required for operation of the processor, core logic and I/O APIC components on the APIC bus.

PICD[1:0] (I/O - 2.5V tolerant open-drain)

The PICD[1:0] (APIC Data) signals are used for bi-directional serial message passing on the APIC bus. They must be connected to the appropriate pins of all APIC bus agents, including the processor and the core logic or I/O APIC components. If the PICD0 signal is sampled low on the active-to-inactive transition of the RESET# signal, then the APIC is hardware disabled.

PRDY# (O - Low Power GTL+)

The PRDY# (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness. See Section 7 for instructions on how to use this signal.

PREQ# (I - 2.5V tolerant)

The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processor. See Section 7 for instructions on how to use this signal.

PWRGOOD (I - 2.5V tolerant)

PWRGOOD (Power Good) is a 2.5V tolerant input. The processor requires this signal to be a clean indication that clocks and the power supplies (Vcc, Vccp, etc.) are stable and within their specifications. Clean implies that the signal will remain low, (capable of sinking leakage current) without glitches, from the time that the power supplies are turned on, until they come within specification. The signal will then transition monotonically to a high (2.5V) state. Figure A.1 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before the rising edge of PWRGOOD. It must also meet the minimum inactive pulse width specified in Table 3.11 (Section 3.6) and be followed by a 1 ms RESET# pulse.

The PWRGOOD signal, which must be supplied to the processor, is used to protect internal circuits against voltage sequencing issues. The PWRGOOD signal should be driven high throughout boundary scan operation.

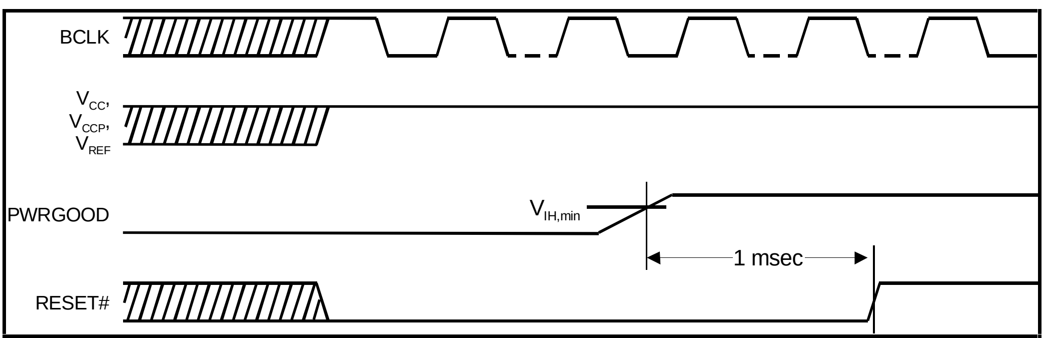

Figure A.1 PWRGOOD Relationship at Power-On

REQ[4:0]# (I/O - Low Power GTL+)

The REQ[4:0]# (Request Command) signals must be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus. They are asserted by the current bus owner when it drives A[35:3]# to define the currently active transaction type.

RESET# (I - Low Power GTL+)

Asserting the RESET# signal resets the processor to a known state and invalidates the L1 and L2 caches without writing back Modified (M state) lines. RESET# must remain active for one millisecond for a “warm” reset. For a power-on type reset, RESET# must stay active for at least one millisecond after Vcc and BCLK have reached their proper DC and AC specifications and after PWRGOOD has been asserted. When observing active RESET#, all bus agents will deassert their outputs within two clocks.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in Section 8 and in every signal description in this appendix.

Unless its outputs are tristated during power-on configuration, after an active-to-inactive transition of RESET#, the processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 0_000F_FFF0H or 0_FFFF_FFF0H. RESET# must be connected to the appropriate pins on both agents on the Mobile Pentium II processor system bus.

RP# (I/O - Low Power GTL+)

The RP# (Request Parity) signal is driven by the request initiator, and provides parity protection on ADS# and REQ[4:0]#. RP# should be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

RS[2:0]# (I - Low Power GTL+)

The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must be connected to the appropriate pins on both agents on the Mobile Pentium II processor system bus.

RSP# (I - Low Power GTL+)

The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#. RSP# should be connected to the appropriate pins on both agents on the Mobile Pentium II processor system bus.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.

SLP# (I - 2.5V tolerant)

The SLP# (Sleep) signal, when asserted in the Stop Grant state, causes the processor to enter the Sleep state. During the Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still running. The processor will not recognize snoops and interrupts in the Sleep state. The processor will only recognize changes in the SLP#, STPCLK# and RESET# signals while in the Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to the Stop Grant state in which it restarts its internal clock to the bus and APIC processor core units.

SMBALERT# (O - 5V tolerant)

The SMBALERT# (SMBus Alert) signal is used by the thermal sensor on the processor to indicate that it requires attention. It is compliant with the SMBALERT# signal of the *System Management Bus Specification*. To use the processor’s thermal sensor, this pin must be connected to the appropriate pin on an SMBus host controller.

SMBCLK (I/O - 5V tolerant)

The SMBCLK (SMBus Clock) signal is compliant with the SMBCLK signal of the *System Management Bus Specification*. To use the processor’s thermal sensor, this pin must be connected to the appropriate pin on an SMBus host controller.

SMBDATA (I/O - 5V tolerant)

The SMBDATA (SMBus Data) signal is compliant with the SMBDATA signal of the *System Management Bus Specification*. To use the processor's thermal sensor, this pin must be connected to the appropriate pin on an SMBus host controller.

SMI# (I - 2.5V tolerant)

The SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.

SMI# is an asynchronous input. However, to guarantee recognition of this signal following an I/O instruction, SMI# must be valid two system bus clocks before the RS[2:0]# assertion of the corresponding I/O bus transaction.

STPCLK# (I - 2.5V tolerant)

The STPCLK# (Stop Clock) signal, when asserted, causes the processor to enter a low-power Stop Grant state. The processor issues a Stop Grant Acknowledge special transaction, and stops providing internal clock signals to all units except the bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in the Stop Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock.

STPCLK# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, STPCLK# must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.

TCK (I - 2.5V tolerant)

The TCK (Test Clock) signal provides the clock input for the test bus (also known as the test access port).

TDI (I - 2.5V tolerant)

The TDI (Test Data In) signal transfers serial test data to the processor. TDI provides the serial input needed for JTAG support.

TDO (O - 2.5V tolerant open-drain)

The TDO (Test Data Out) signal transfers serial test data from the processor. TDO provides the serial output needed for JTAG support.

TMS (I - 2.5V tolerant)

The TMS (Test Mode Select) signal is a JTAG support signal used by debug tools.

TRDY# (I - Low Power GTL+)

The TRDY# (Target Ready) signal is asserted by the target to indicate that the target is ready to receive write or implicit writeback data transfer. TRDY# must be connected to the appropriate pins on both agents on the Mobile Pentium® II processor system bus.

TRST# (I - 2.5V tolerant)

The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. Mobile Pentium® II processors self-reset during power-on; therefore, it is not necessary to drive this signal during power-on reset.

VID[3:0] (O - open drain)

The VID[3:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to Vss on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification changes on Mobile Pentium® II processors. These pins (VID3 through VID0) are defined in Table A.1. A '1' in this table refers

to an open pin and '0' refers to a short to ground. The power supply must supply the voltage that is requested or disable itself.

To use these pins, attach pull-up resistors to each one connected to a power supply that is guaranteed to be stable when the supply to the core power supply is stable. The pull-up voltage and resistance are not specified, but the current through the pins must not exceed the value shown in Table 3.3.

Table A.1 Voltage Identification Pin Definition

VID[3:0]	Vcc (V)	VID[3:0]	Vcc (V)	VID[3:0]	Vcc (V)	VID[3:0]	Vcc (V)
0000	2.00	0100	1.80	1000	1.60	1100	1.40
0001	1.95	0101	1.75	1001	1.55	1101	1.35
0010	1.90	0110	1.70	1010	1.50	1110	1.30
0011	1.85	0111	1.65	1011	1.45	1111	No CPU

A.2 Signal Summaries

Tables A.2 through A.5 list the attributes of the processor input, output, and I/O signals.

Table A.2 Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	PC compatibility	Always[1]
BCLK	High	—	System Bus	Always
BPRI#	Low	BCLK	System Bus	Always
DEFER#	Low	BCLK	System Bus	Always
FLUSH#	Low	Asynch	PC compatibility	Always[1]
IGNNE#	Low	Asynch	PC compatibility	Always[1]
INIT#	Low	Asynch	System Bus	Always[1]
INTR	High	Asynch	PC compatibility	APIC disabled mode
LINT[1:0]	High	Asynch	APIC	APIC enabled mode
NMI	High	Asynch	PC compatibility	APIC disabled mode
PICCLK	High	—	APIC	Always
PREQ#	Low	Asynch	Implementation	Always
PWRGOOD	High	Asynch	Implementation	Always
RESET#	Low	BCLK	System Bus	Always
RS[2:0]#	Low	BCLK	System Bus	Always
RSP#	Low	BCLK	System Bus	Always
SLP#	Low	Asynch	Implementation	Stop Grant state
SMI#	Low	Asynch	PC compatibility	Always[2]
STPCLK#	Low	Asynch	Implementation	Always
TCK	High	—	JTAG	Always
TDI	High	TCK	JTAG	Always
TMS	High	TCK	JTAG	Always
TRDY#	Low	BCLK	System Bus	Response phase
TRST#	Low	Asynch	JTAG	Always

NOTES:

1. Synchronous assertion with active TRDY# guarantees synchronization.
2. Synchronous assertion two bus clocks before active RS[2:0]# guarantees synchronization and I/O instruction trapping.

Table A.3 Output Signals

Name	Active Level	Clock	Signal Group
FERR#	Low	Asynch	PC compatibility
IERR#	Low	Asynch	Implementation
PRDY#	Low	BCLK	Implementation
SMBALERT#	Low	Asynch	Implementation
TDO	High	TCK	JTAG
VID[3:0]	—	Asynch	Implementation

Table A.4 Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:3]#	Low	BCLK	System Bus	ADS#, ADS#+1
ADS#	Low	BCLK	System Bus	Always
AP[1:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
BR0#	Low	BCLK	System Bus	Always
BP[3:2]#	Low	BCLK	System Bus	Always
BPM[1:0]#	Low	BCLK	System Bus	Always
D[63:0]#	Low	BCLK	System Bus	DRDY#
DBSY#	Low	BCLK	System Bus	Always
DEP[7:0]#	Low	BCLK	System Bus	DRDY#
DRDY#	Low	BCLK	System Bus	Always
LOCK#	Low	BCLK	System Bus	Always
REQ[4:0]#	Low	BCLK	System Bus	ADS#, ADS#+1
RP#	Low	BCLK	System Bus	ADS#, ADS#+1

Table A.5 Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	System Bus	ADS#+3
BERR#	Low	BCLK	System Bus	Always
BINIT#	Low	BCLK	System Bus	Always
BNR#	Low	BCLK	System Bus	Always
HIT#	Low	BCLK	System Bus	Always
HITM#	Low	BCLK	System Bus	Always
PICD[1:0]	High	PICCLK	APIC	Always
SMBCLK	High	—	SMBus	Always
SMBDATA	High	SMBCLK	SMBus	Always

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