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VIDEO SYNC-STRIPPER AND DECODER
RSS-102

ENGINEERING DATA

DESCRIPTION

The RSS-102 provides DC restoration of incoming composite video signals and provides DC restored composite video output. The 102 also detects the sync pulses and provides a composite sync output with TTL and CMOS compatible level.

Sync pulses are also decoded by the 102 and true Horizontal and true Vertical sync pulses are provided with TTL and CMOS levels.

Standard video input levels of 0.7 to 1.4 Volt Peak-to-Peak, White positive (negative going sync pulses) must be applied to the input. Acquisition of the input video will take place as long as the input video back porch level is within ±1.0 volt of analog common.

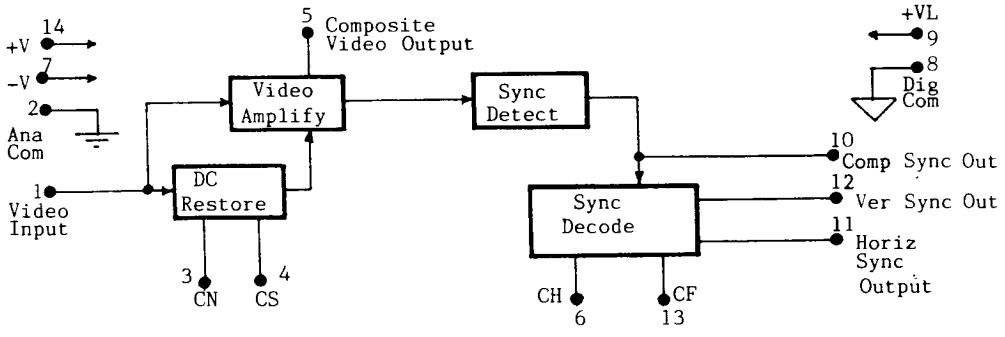
Separate Analog and Digital commons provide common-mode noise rejection to "isolate" digital noise from the video signal.

The RSS-102 is a single chip bipolar monolithic integrated circuit.

FEATURES

* COMPATIBLE WITH RS-170, RS-330, RS-343, RS-420, PAL AND OTHER FORMATS
* PROVIDES DC RESTORATION
* PROVIDES HORIZONTAL SYNC
* PROVIDES VERTICAL SYNC
* PROVIDES COMPOSITE SYNC
* MAY BE USED WITH ANY SCAN RATE

BLOCK DIAGRAM

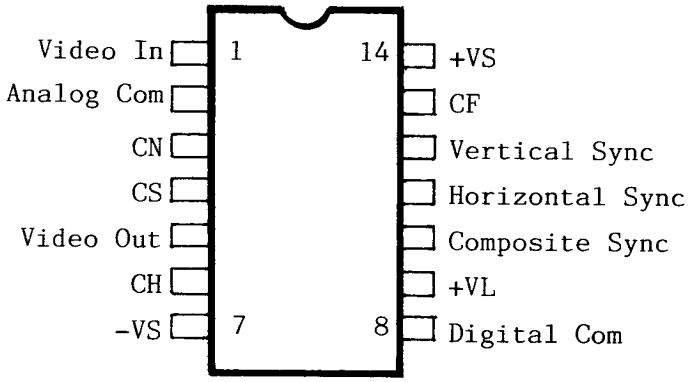


ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (Pin 14 to 7)	18 Volts
Digital Supply Voltage (Pin 9 to 8)	7 Volts
Analog-to-Digital Common Differential Voltage (Pin 2 to 8)	±1.0 Volt
Video Input Voltage (Pin 1 to 2)	± VS Volts
Output Current (Pin 5)	±40 milliamps
Output Current (Pins 10, 11 or 12)	50 milliamps
Operating Temperature Range -CD	0°C to +70°C
-MD	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note: Absolute maximum ratings are those voltage, current and temperature levels above which permanent damage may result. Consult Specifications and Applications sections of this data sheet for conditions for normal operation.

CONNECTIONS:



Note: Refer to the Block Diagram, Circuit Description and Applications sections of this data sheet for exact use of the pin connections.

PART NUMBERS

Order:	RSS-102-CD	for 0°C to +70°C	operation
	RSS-102-MD	-55°C to +125°C	

Note: Packaging is a 14 pin Ceramic Dual in-line (CERDIP), hermetically sealed.

SPECIFICATIONS

(±VS = ±5 Volts, +VL = +5 Volts, T_A = +25 °C)

PARAMETER	MIN	TYP	MAX	UNITS
VIDEO INPUT				
Minimum Input Signal Level		0.21	0.40	Volts P-P
Nominal Input Signal Level		1.00		Volts P-P
Maximum Input Signal Level	1.50	1.80		Volts P-P
Input Resistance	2.7	3.5	5.0	k Ohms
DC Input Level (Backporch)	-1.0		+1.0	Volts
VIDEO OUTPUT				
Voltage Gain	0.87	0.91	1.0	X
Bandwidth	20	30		MHz
Total Throughput Delay		15	20	nS
Differential Phase Error		0.3		degrees
Differential Gain Error		0.3		dB
Load Resistance	75			Ohms
Dynamic Output Resistance		0.3	2.0	Ohms
SYNC OUTPUT [TTL Level]				
High Level Output Voltage	2.5	3.6		Volts
Low Level Output Voltage		0.2	0.4	Volts
High Level Output Current			-400	uA
Low Level Output Current			4	mA
Transition Time				
Low-to-High		15	25	nS
High-to-Low		20	30	nS
TIMING				
Composite Sync Output				
Leading Edge Delay		610	1000	nS
Trailing Edge Delay		160	250	nS
Horizontal Sync Output				
Leading Edge Delay		940	1250	nS
Output Pulse Width (CH = 1 nF)	5.0	6.85	8.0	uS
Vertical Sync Output				
Leading Edge Delay		7		uS
Trailing Edge Delay		7		uS
Timing Jitter		4		nS
POWER				
Analog/Digital Common Voltage			±1.0	Volt
Analog Supply Voltage				
+VS	+4.75	+5.0	+8.0	Volts
-VS	-2.50	-5.0	-8.0	Volts
Digital Supply Voltage	+4.25	+5.0	+6.0	Volts
Analog Supply Current				
+VS		35.5	45.0	mA
-VS		32.0	40.0	mA
Digital Supply Current		8.9	12.0	mA
Total Dissipation		382	485	mW

Specifications are subject to change without notice

CIRCUIT DESCRIPTION and APPLICATIONS

The RSS-102 performs three basic operations; (A) DC Restoration of the incoming video signal, (B) Sync Pulse stripping and (C) Sync Decoding.

DC Restoration takes place by sensing the negative tips of the input sync pulses. This voltage level is stored in an external capacitor, CN.

An external offset voltage is applied to the external capacitor, CS. This voltage represents the sync pulse amplitude of the input signal and may be used to set the back porch voltage level to precisely 0.0 volts at the DC Restored Composite Video Output. If the input sync pulse amplitude changes this voltage will have to be re-adjusted to maintain a zero voltage back porch.

Sync pulses are internally stripped, converted to TTL voltage levels and presented at the Composite Sync Output.

Sync Decoding takes place internally and uses two timing circuits. Horizontal sync output pulse width is set with an external capacitor, CH. The width of the Horizontal Sync Output pulse can be trimmed with an optional adjustment circuit shown below.

A second timing circuit uses the external capacitor, CF. The purpose of this circuit is to allow the decoding process to detect equalization and serration pulses, in order to produce a valid Horizontal Output pulse during the Vertical interval.

Non-standard scan rates can be accommodated by scaling the external timing capacitors accordingly and with the optional trimming circuits.

Note: U.S. Patent Pending