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SP5668

2.7GHz 3-Wire Bus Controlled Synthesiser

Preliminary Information

DS4538 ISSUE 1.6 January 1997

The SP5668 is a single chip frequency synthesiser designed for tuning systems up to 2.7GHz.

The RF preamplifer contains a divide by two prescaler which can be disabled for applications up to 2GHz so enabling a step size equal to the comparison frequency up to 2GHz and twice the comparison frequency up to 2.7GHz.

Comparison frequencies are obtained either from a crystal controlled on–chip oscillator or from an external source.

The device contains three switching ports, P0 – P2, together with an 'in–lock' flag output. Various test modes including varactor disable and charge pump disable are also included.

Features

- Complete 2.7GHz single chip system
- Optimised for low phase noise
- Selectable divide by two prescaler
- Selectable reference division ratio
- Charge pump disable
- Varactor line disable
- 'In–lock' flag
- Two selectable charge pump currents
- Three switching ports
- Reference frequency output
- ESD protection (Normal ESD handling procedures should be observed)

Ordering Information

SP5668/KG/MP1S (Tubes)

SP5668/KG/MP1T Tape and Reel)

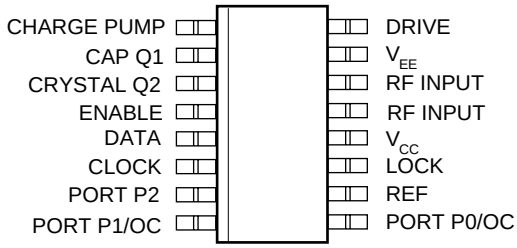


Figure 1 - Pin connections - top view

Applications

- SAT, TV, VCR and Cable tuning systems
- Communications systems

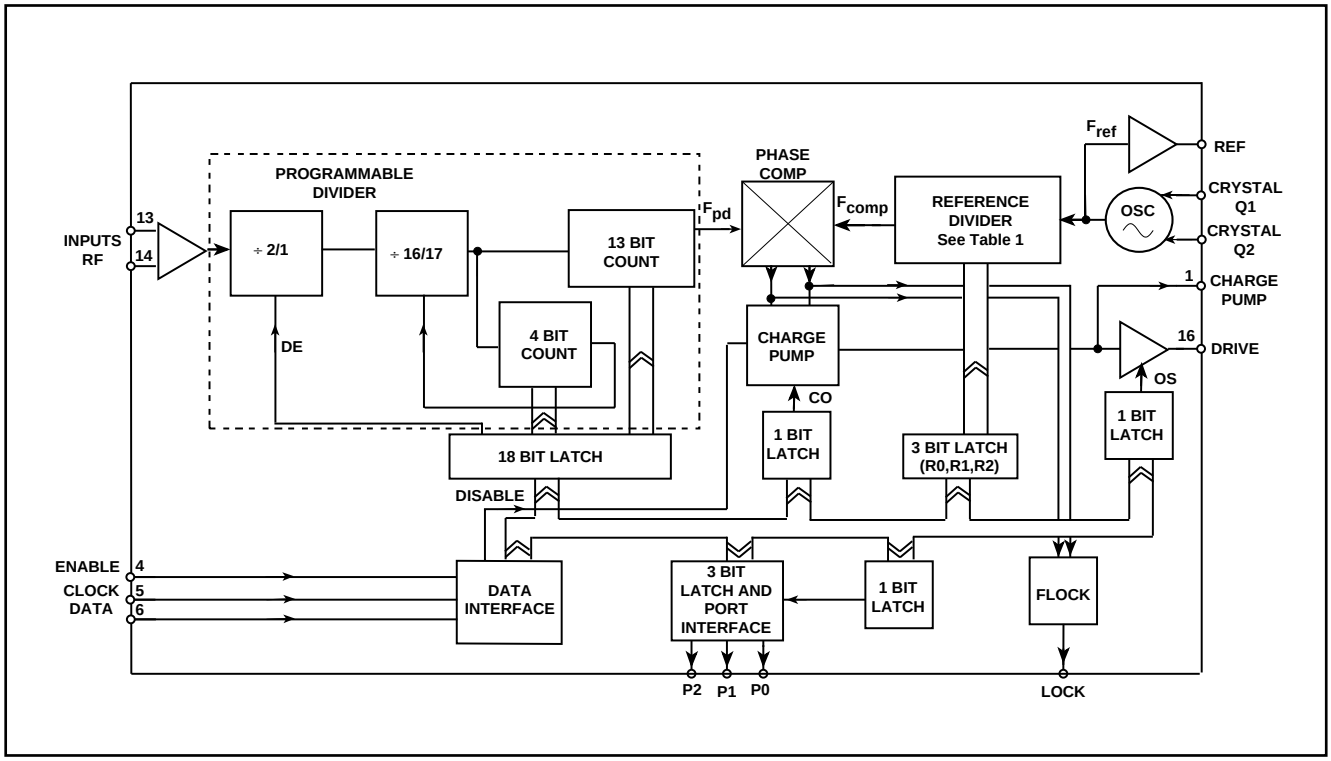


Figure 2 - SP5668 block diagram

Electrical Characteristics

T_{AMB} = 120°C to +80°C, V_{CC} = +4.5 to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current, Icc	12		65	81	mA	Vcc = 5V Prescaler enabled, PE = 1
			58	72	mA	Vcc = 5V Prescaler disabled, PE = 0
RF input voltage	13, 14	100		300	mV_{rms}	100MHz Prescaler enabled, PE = 1 See Fig. 5b.
	13, 14	40		300	mV_{rms}	300MHz - 2.7GHz Prescaler enabled, PE = 1, See Fig. 5b.
	13,14	40		300	mV_{rms}	100MHz to 2.0GHz Prescaler disabled, PE = 0, See Fig. 5a
RF input impedance	13, 14					See Fig. 4.
Data, Clock, Enable	4,5,6					
Input high voltage		3		V_{CC}	V	
Input low voltage		0		0.7	V	
Input high current				10	µA	Input voltage = V_{CC}
Input low current				-10	µA	Input voltage = V_{EE}
Hysteresis			400		mV	
Clock Rate	6			500	kHz	

Electrical Characteristics (continued)

T_{AMB} = 120°C to +80°C, V_{CC} = +4.5 to +5.5V. Reference frequency = 4MHz. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Bus timing	4, 5, 6					
Data set up , t_{SU}		300			ns	See Fig. 3
Data hold, t_{HD}		600			ns	See Fig. 3
Enable set up, t_{ES}		300			ns	See Fig. 3
Enable hold , t_{EH}		600			ns	See Fig. 3
Clock to enable, t_{CE}		300			ns	See Fig. 3
Charge pump output Current	1					See Table 3, V_{pin1} =2V
Charge pump output leakage	1			±10	nA	V_{pin1} = 2V
Drive output current	16	1			mA	V_{PIN16} = 0.7V
Drive output saturation Voltage when disabled	16			350	mV	OS = 1
External reference input frequency	3	2		20	MHz	AC coupled sinewave
External reference input amplitude	3	200		500	mVp-p	AC coupled sinewave
Crystal frequency	3	4		12	MHz	
Recommended crystal Series resistance		10		200	Ω	Applies to 4MHz crystal only. "Parallel resonant" crystal. Figure quoted is under all conditions including start up.
Reference oscillator bias current	3	200			µA	See Fig. 11
REF output voltage*	10		350		mVp-p	AC coupled, 4MHz reference frequency, See Fig.
Phase detector comparison frequency				4	MHz	
Equivalent phase noise at phase detector					dBc/Hz	See **Note
RF division ratio		240		131071		PE = 0, Prescaler disabled
		480		262142		PE = 1, Prescaler enabled
Reference division ratio						See Table 1
Output ports P0-P2	7-9					
Sink current		10			mA	V_{PORT} = 0.7V
Leakage current				10	µA	V_{PORT} = 13.2V
Lock output						
Sink current		1			mA	V_{PIN10} = 0.7V, 'out of lock'
Leakage current				10	µA	'in lock'

* REF output should be connected to V_{CC} if unused

** Note: 1. -148dBc/Hz @ 1KHz offset with 1MHz comparison frequency measured at the phase comparator.
2. When external reference is used, a high signal level is required for low phase noise.

Absolute Maximum Ratings

All voltages are referred to V_{EE} at 0V

Charateristics	Pin	Min	Max	Units	Conditions
Supply voltage, V_{CC}	12	-0.3	7	V	
RF input voltage	13, 14		2.5	Vp-p	
RF input offset	13, 14	-0.3	V_{CC}+0.3	V	
Port output voltage	7-9	-0.3	14	V	Port in off state
	7-9	-0.3	6	V	Port in on state
Total port current	7-9		50	mA	
REFoutput DC offset	10	-0.3	V_{CC}+0.3	V	
Lock output DC offset	11	-0.3	V_{CC}+0.3	V	
Lock output current	11		10	mA	
Charge pump DC offset	1	-0.3	V_{CC}+0.3	V	
Drive DC offset	16	-0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2, 3	-0.3	V_{CC}+0.3	V	
Data, Clock & inputs	4,5,6	-0.3	V_{CC}+0.3	V	
Storage temperature		-55	+150	°C	
Junction temperature			+150	°C	
MP16 Thermal resistance					
Chip to ambient			111	°C/W	
Chip to case			41	°C/W	
Power consumption at V_{CC} = 5.5V			407	mV	All ports off, prescaler enabled
ESD protection	ALL	2		kV	MIL-STD 883 TM3015

Functional Description

The SP5668 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. The RF preamplifier contains a selectable divide by two for operation above 2.0GHz. Up to 2GHz the RF input interfaces directly with the programmable divider, so eliminating degradation in phase noise due to the prescaler action. The block diagram is shown in Fig.2.

The SP5668 is controlled by a standard 3–wire bus comprising data, clock and enable inputs. The programming word contains 27 bits. P0 - P2 are used for port selection, 2^{17} - 2^{0} set the programmable divider ratio R2 - R0 select the reference division ratio (Table1). C0 sets the charge pump current (Table 3) and the remaining two bits T0, OS access test modes and disable the varactor drive (Table 2).The programming format is shown in Fig. 3.

The clock input is disabled by an enable low signal, data is therefore only clocked into the internal shift registers during an enable high and is loaded into the controlling buffers by an enable high to low transition. This load is also synchronised with the programmable divider so giving smooth fine tuning.

The RF signal is fed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier is fed to the ÷ 2/1 selectable prescaler and then to the 17 bit fully programmable divider, which is of MN+A architecture. The M counter is 13 bit and the A counter 4. If bit PE is set to a 0 the prescaler is disabled; the control function PE cannot be used dynamically. The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on board crystal controlled oscillator or from an external source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 8 ratios as described in Table 1.

The output of the phase comparator feeds the charge pump and loop amplifier section, which when used with an external high voltage transistor and loop filter integrates the current pulses into the varactor line voltage. The charge pump current is selected by bit C0 as described in Table 3.

The phase comparator also drives the lock detect circuit which generates a lock flag. 'In-lock' is indicated by a high impedance state on the lock output.

The crystal frequency Fref is available at the REF output. This may be used as the reference for a second synthesiser as shown in Fig. 6. The REF output is disabled by connecting the output, pin 3, to V_{CC}.

Phase Noise

The SP5668 has been designed to offer good phase noise performance even when operated with a standard low profile 4MHz crystal and a high comparison frequency, e.g. 2MHz.

The typical phase noise performance measured in the standard application is contained in Table 4. It has been demonstrated that even higher levels of performance will be achieved in a tuner application.

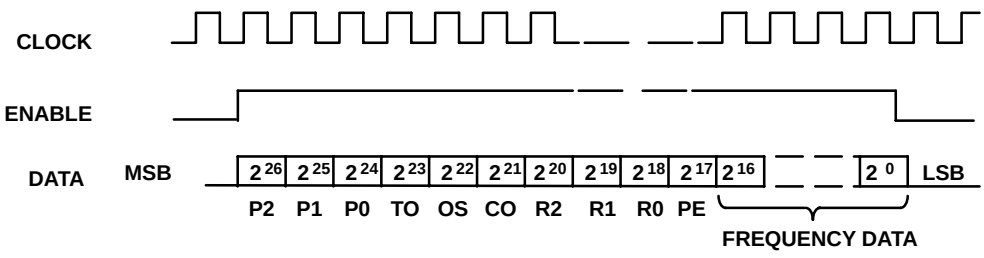
Test Modes

The programmable divider output divided by two Fpd/2 and the comparison frequency Fcomp, can be switched to ports P0 and P1 respectively.

The charge pump can be forced to either source or sink current, and may be disabled to high impedance state.

The varactor DRIVE output can be disabled by the OS bit within the data word, so switching the external transistor 'OFF' and allowing an external voltage to be written to the varactor line for tuner alignment purposes.

The test modes are described in Table 2.



2^{16} to 2^{0} : Programmable divider ratio control bits
PE : ÷2 Prescaler (Enable = 1, Disable = 0)
R2 , R1 , R0 : Reference divider ratio control bits (see Table 1)
P2, P1, P0 : Port control bits
CO : Charge Pump current select (see Table 3)
OS : Drive output disable switch
T0 : Test mode enable (see Table 2)

Figure 3 - Data format and timing

R2	R1	R0	RATIO	Comparison Frequency with a 4MHz external reference
0	0	0	2	2MHz
0	0	1	4	1MHz
0	1	0	8	500kHz
0	1	1	16	250kHz
1	0	0	32	125kHz
1	0	1	64	62.5kHz
1	1	0	128	31.25kHz
1	1	1	256	15.625kHz

Table 1 - Reference division ratio

P1	P0	T0	FUNCTIONAL DESCRIPTION
X	X	0	Normal operation
0	0	1	Charge pump sink. LOCK output = Lo Z
0	1	1	Charge pump source. LOCK output = Hi Z
1	0	1	Charge pump disable. LOCK output = Lo Z
1	1	1	Port P1 = Fcomp: Port 0 = Fpd/2
X = Don't care			

Table 2 - Test modes

C0	CURRENT IN mA		
	MIN	TYP	MAX
0	0.23	0.30	0.37
1	0.68	0.90	1.12

Table 3 - Charge pump

F_{LO}	F_{comp} (4MHz XTAL)	RF Division RATIO	VCO PHASE NOISE @1kHZ OFFSET (dBc/Hz)	EQUIVALENT PHASE NOISE PHASE DETECTOR (dBc/Hz)
2GHz	1MHz	2000	-84	-146
2GHz	2MHz	1000	-80	-144

Table 4 - Typical phase noise

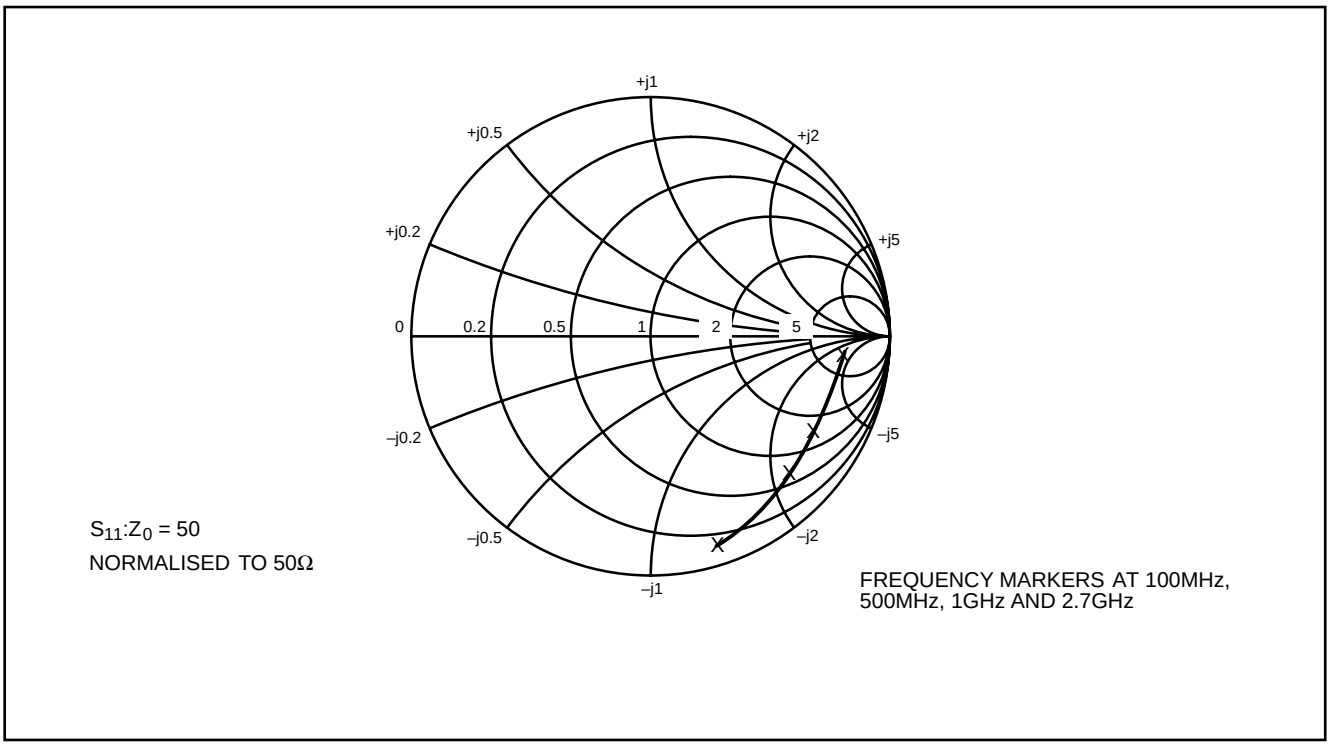


Figure 4 - Typical input impedance

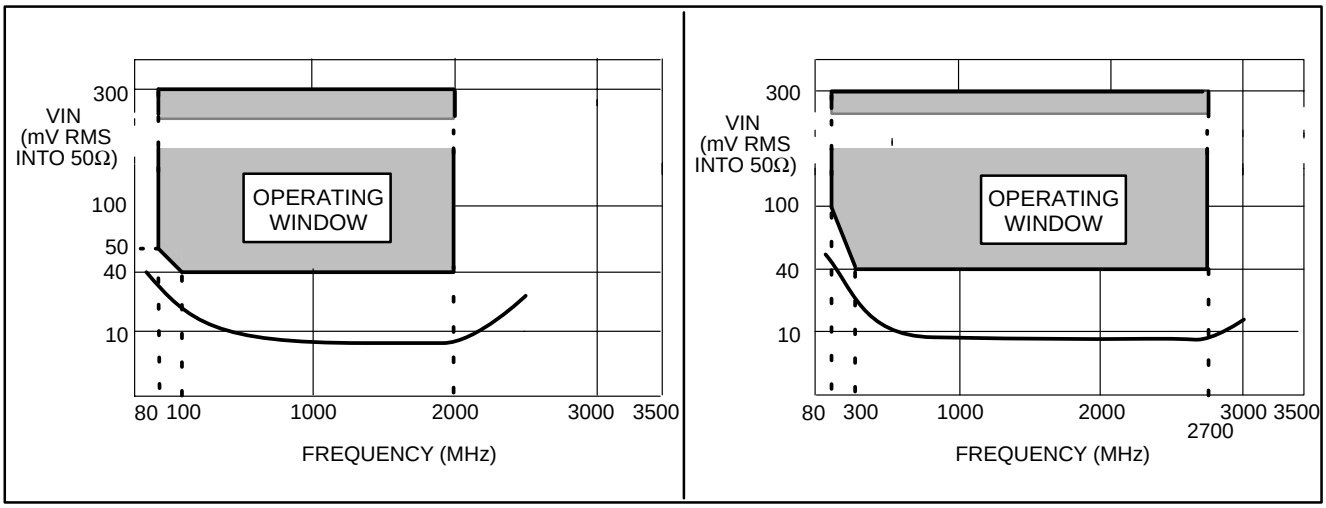


Figure 5a - Typical input sensitivity
(Prescaler disabled, PE=0)

Figure 5b - Typical input sensitivity
(Prescaler enabled, PE=1)

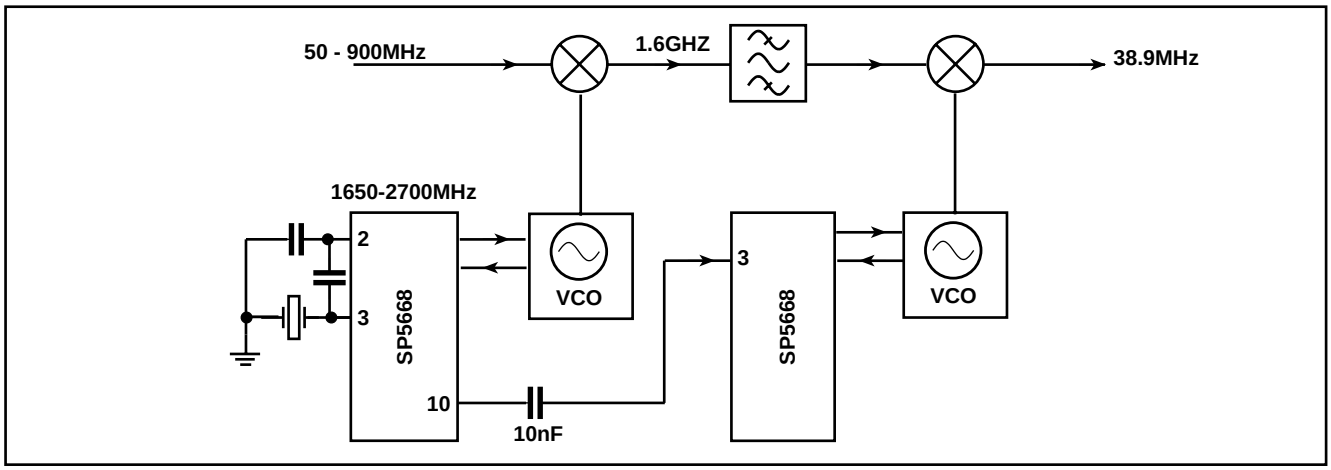


Figure 6 - Example of double conversion from VHF/UHF frequencies to TV IF

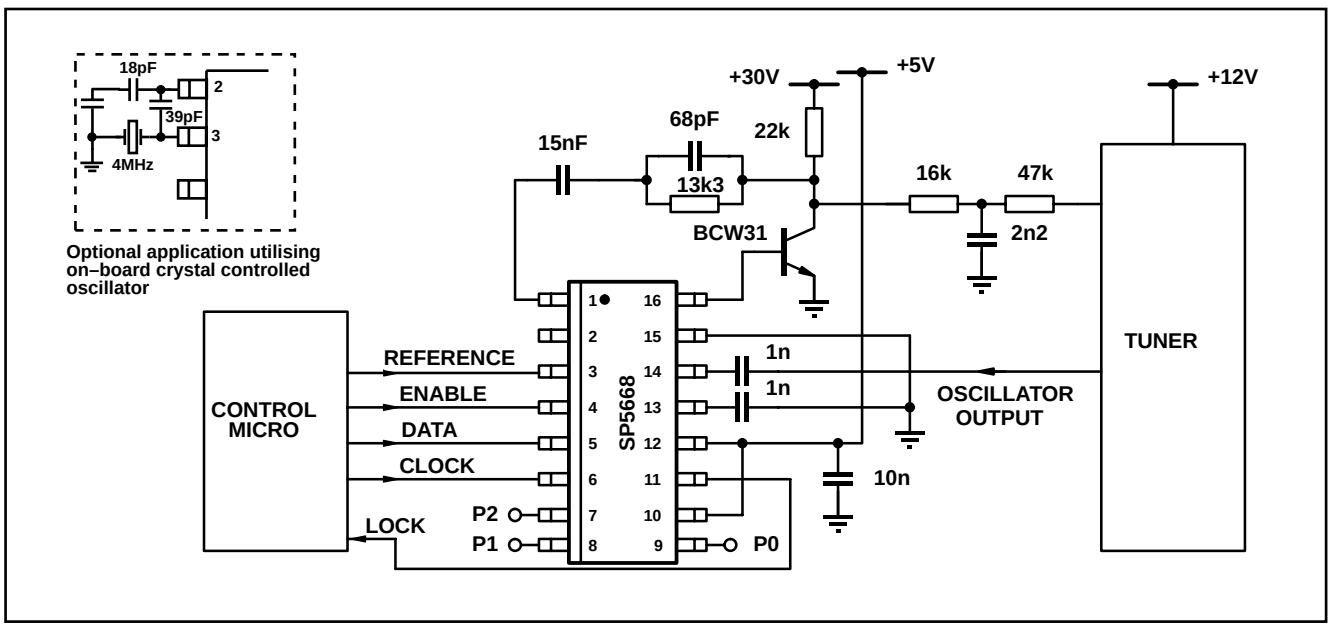


Figure 7 - Typical application, SP5668

Application Notes

A generic set of application notes AN168 for designing with synthesisers such as the SP5668 has been written. This covers aspects such as loop filter design and decoupling. This application note is also featured in the Media IC Handbook.

A generic test/demo board has been produced which can be used for the SP5668. A circuit diagram is shown in Fig. 8.

The board can be used for the following purposes:

(A) Measuring RF sensitivity performance.
(B) Indicating port function
(C) Synthesising a voltage controlled oscillator
(D) Testing of external reference sources

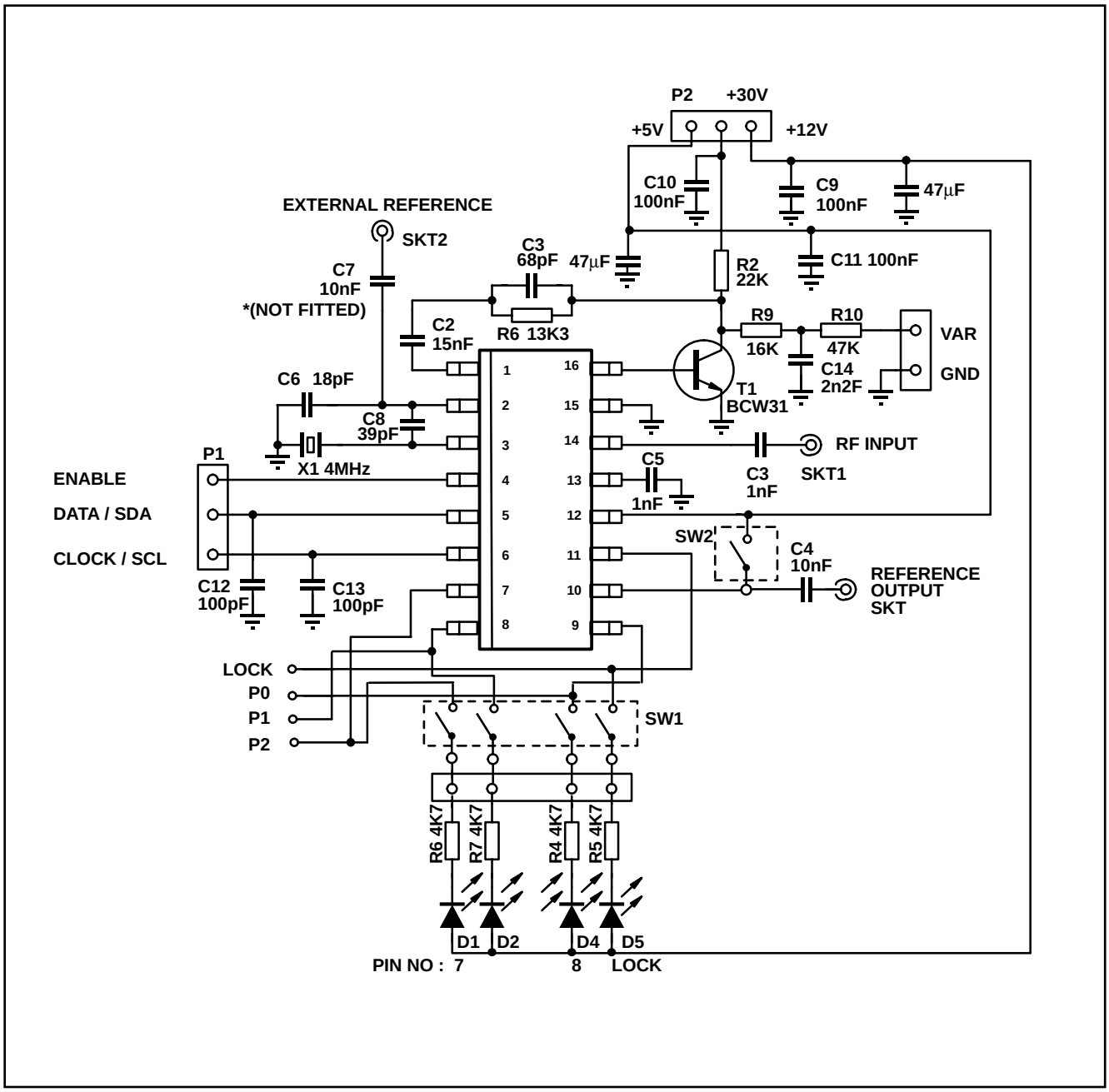


Figure 8 - Evaluation board

Loop Bandwidth

The majority of applications for which the SP5668 is intended require a loop filter bandwidth of between 2kHz and 10kHz.

Typically the VCO phase noise will be specified at both 1kHz and10kHz offset. It is common practice to arrange the loop filter bandwidth such that the 1kHz figure lies within the loop bandwidth. Thus the phase noise depends on the synthesiser comparator noise floor, rather than the VCO.

The 10kHz offset figure should depend on the VCO providing the loop is designed correctly, and is not underdamped.

Reference Source

The SP5668 offers optimal LO phase noise performance when operated with a large step size. This is due to the fact that the LO phase noise within the loop bandwidth is:

$$\text{phase comparator noise floor} + 20 \log \left(\frac{\text{LO frequency}}{\text{phase comparator frequency}} \right)$$

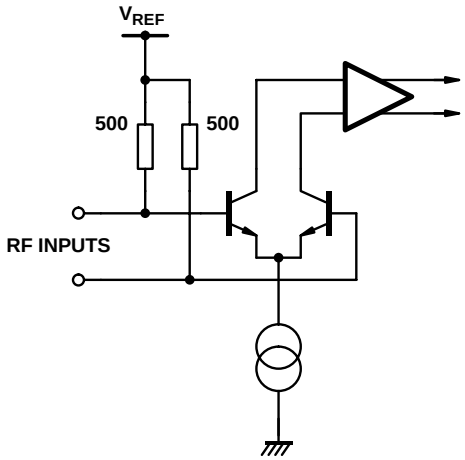
Assuming the phase comparator noise floor is flat irrespective of sampling frequency, this means that the best performance will be achieved when the overall LO to phase comparator division ratio is a minimum.

There are two ways of achieving a higher phase comparator sampling frequency:–

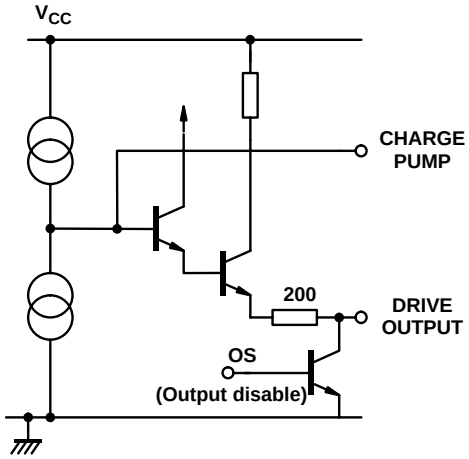
A) reduce the division ratio between the reference source and the phase comparator

B) use a higher reference source frequency.

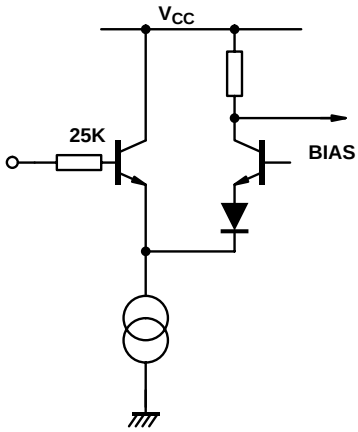
Approach B) may be preferred for best performance since it is possible that the noise floor of the reference oscillator may degrade the phase comparator performance if the reference division ratio is very small.



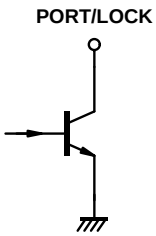
RF inputs



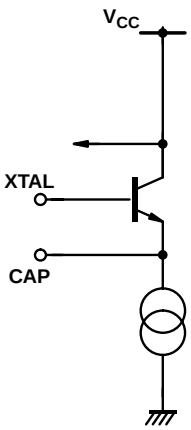
Loop amplifier



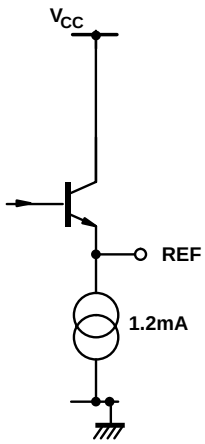
Disable, Enable, Data and Clock inputs



Output Ports and Lock Output

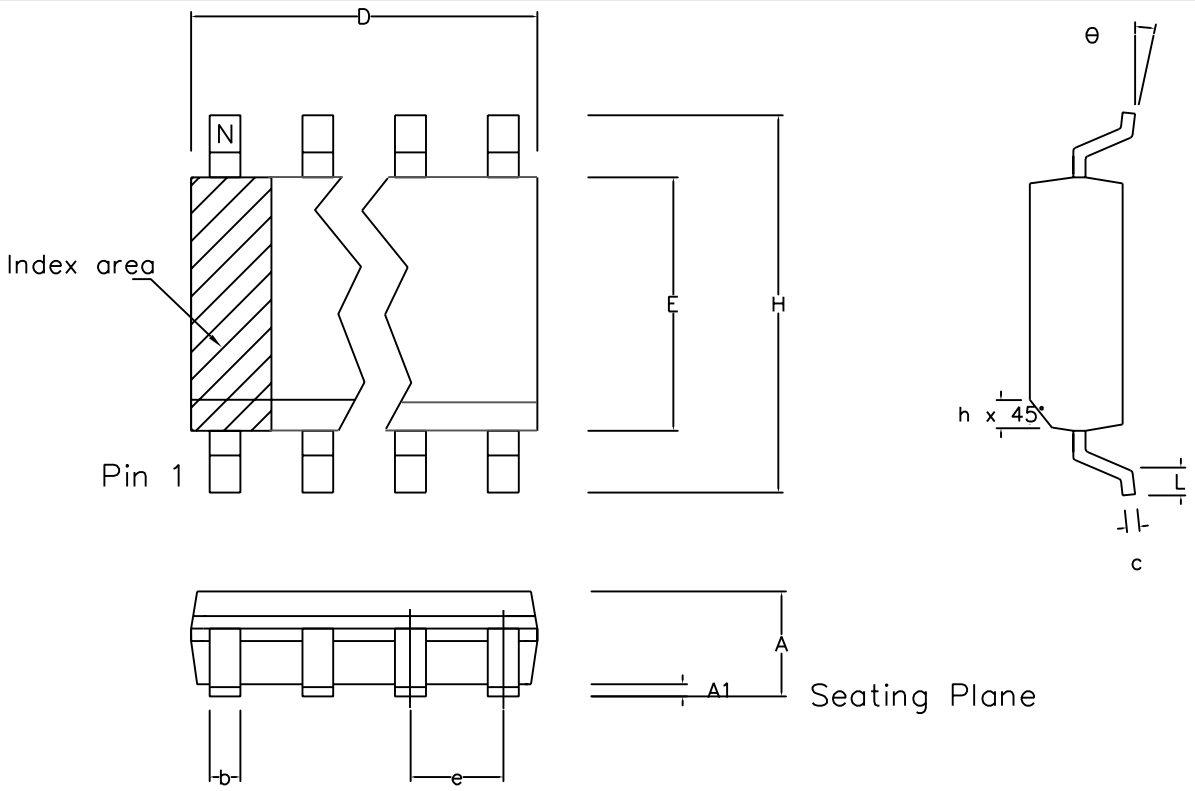


Reference oscillator



Reference output

Figure 9 - Input/Output interface circuits



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
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APPRD.					

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Package Code DC

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