

Serial Input Hex/Quad "Clickless" Volume Control with Master Attenuation

SSM2160/SSM2161

FEATURES

Digitally-Controlled "Clickless" Level Adjustment

SSM2160: Six Channels SSM2161: Four Channels

Master Control Has 128 1 dB Steps

Each Channel Has 32 1 dB Steps Plus Mute

Step Sizes Can Be Changed Using External Resistors

High Gain Accuracy

100 dB Gain Range

Excellent Audio Characteristics:

 $-100 \text{ dBu SNR } (0 \text{ dBu } = 0.775 \text{ V rms, } V_S = \pm 5 \text{ V})$

+10 dBu Headroom (Vs = ±5 V)

0.008% THD+N (@ 1 kHz, V_{IN} = -10 dBu, Unity Gain)

-80 dB Crosstalk (@ 1 kHz)

Single or Dual Supply Operation

24-Pin Plastic DIP and SOIC Packages (SSM2160)

20-Pin Plastic DIP and SOIC Packages (SSM2161)

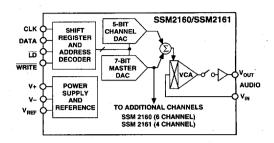
APPLICATIONS

Dolby* Pro-Logic Master Volume Control Home THX† System DSP Soundfield Processors Automotive Audio Systems HDTV Audio Systems

GENERAL DESCRIPTION

The SSM2160 and SSM2161 allow digital control of volume for six and four channels, respectively, with a master level control. In order to avoid "clicking," the device uses high performance voltage controlled amplifiers (VCAs) for the audio signal path. The VCA control port effectively isolates DAC charge injection from the audio path, which is the major contributor to clicking in resistor-ladder type attenuators. Each channel is controlled by a dedicated 5-bit DAC, providing 32 steps of adjustment, plus

FUNCTIONAL BLOCK DIAGRAM



mute. In addition, a master 7-bit DAC feeds every control port, with 128 steps. Therefore, a balance can be achieved among all channels over a 32-step range, and the master control allows adjustment over its entire range while maintaining the desired channel-to-channel balance. Step sizes are defaulted to 1 dB, but channel sizes can be increased or master sizes decreased by the addition of external resistors. Approximately 80 dB of attenuation and up to 20 dB of gain is possible.

The SSM2160/SSM2161 can operate either single or dual supply, with a total supply voltage range of 8 V to 36 V. An on-chip voltage reference is provided for single-supply, applications.

*Dolby is a registered trademark of Dolby Laboratories Licensing Corporation. +Home THX is a registered trademark of Lucasfilm, Ltd.

This is a preliminary data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

14-30 AUDIO COMPONENTS

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SPECIFICATIONS

SSM2160/SSM2161

ELECTRICAL SPECIFICATIONS ($V_S=\pm 5$ V, $A_V=0$ dB, 0 dBu = 0.775 V rms, $V_{IK}=-10$ dBu, $f_{AUDI0}=1$ kHz, $f_{CLK}=250$ kHz, $R_L=100$ k Ω , $-40^{\circ}C < T_A < +85^{\circ}C$, unless otherwise noted. Typical specifications apply at $T_A=+25^{\circ}C$.)

Parameter	Conditions	Min	Тур	Max	Units
AUDIO PERFORMANCE Noise Headroom Total Harmonic Distortion Plus Noise	V _{IN} = GND, 20 kHz Bandwidth Clip Point = 1% THD+N 2nd and 3rd Harmonics Only A _V = 0 dB A _V = -20 dB		-100 +10 0.008 0.02	TBD TBD TBD	dBu dBu %
Channel Separation	$A_V = 0 \text{ dB}, V_{IN} = +10 \text{ dBu}$ Any Channel to Another		0,8 80	1.0	% dB
ANALOG INPUT Input Offset Voltage Input Impedance			10 14		mV kΩ
GAIN CONTROL ELEMENTS Default Step Size—Master Default Step Size—Channel Gain Error Gain Match Error	A _V MASTER = 0 dB to -60 dB. A _V CHANNEL = 0 dB to +20 dB Relative to Same Channel A _V MASTER = 0 dB A _V MASTER = -20 dB A _V MASTER = -40 dB A _V MASTER = -60 dB Channel-to-Channel; Same Level Setting A _V MASTER = 0 dB A _V MASTER = -20 dB A _V MASTER = -20 dB A _V MASTER = -20 dB A _V MASTER = -40 dB A _V MASTER = -40 dB A _V MASTER = -40 dB A _V MASTER = -60 dB	TBD TBD	1.0	TBD TBD 0.25 0.25 1 2 0.25 0.25 0.25 1 2	dB dB dB dB dB dB dB
Mute Attenuation			-105		dB
ANALOG OUTPUT Output Impedance Mute Output Impedance Output Sink Current Minimum Resistive Load Drive Maximum Capacitive Drive Offset Voltage	Channel Muted		TBD TBD TBD TBD TBD 20		Ω Ω mA Ω pF mV
CONTROL SECTION Logic Input LO Logic Input HI Logic Input Current Maximum Clock Frequency Timing Characteristics	Logic LO or HI See Timing Diagram	2.0	1 2	0.8	V V μA MHz
REFERENCE Output Voltage Output Impedance Load Regulation	$V_S = +10 \text{ V (Single Supply)}$ -10 mA \le I _L \le +10 mA	4.9	5.0 TBD 0.1	5.1	V Ω %
POWER SUPPLIES Supply Voltage Range Supply Current Power Supply Rejection Ratio	Dual Supply Single Supply Positive Negative Dual Supply	±4 +8	TBD 20 TBD	±15 +30 TBD 30	V V mA mA dB

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AUDIO COMPONENTS

SSM2160/SSM2161

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage
Dual Supply±18 V
Single Supply+36 V
Analog Input Voltage $\pm V_S$
Logic Input Voltage ±V _S
Operating Temperature Range40°C to +85°C
Storage Temperature65°C to +150°C
Junction Temperature (T ₁)+150°C
Lead Temperature (Soldering, 60 sec) +300°C

THERMAL CHARACTERISTICS Thermal Resistance ² 24-Pin Plastic DIP (SSM2160)	
θ _{τΑ}	. TBD°C/W
$\theta_{ m JC}$. TBD°C/W
24-Pin SOIC (SSM2160)	
$ heta_{ exttt{JA}}$. TBD°C/W
θ_{IC}	. TBD°C/W
20-Pin Plastic DIP (SSM2161)	
$ heta_{ ext{IA}}$	TBD°C/W
θ _{IC}	
20-Pin SOIC (SSM2161)	
θ _{1A}	TBD°C/W
θ _{IC}	TBD°C/W
•	

TRANSISTOR COUNT

	- 995	ire 1	
Number of Transistors	ari.	TI	16

ESD RATINGS

883 (Human Body) Model	TBD kV
EIAJ Model	. TBD 🕅
NOTES	

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. $^{2}\theta_{1A}$ is specified for worst-case conditions, i.e., θ_{1A} is specified for device in socket

ORDERING GUIDE

for P-DIP and device soldered in circuit board for SOIC package.

Model	Temperature Range	Package Option*		
SSM2160N	-40°C to +85°C	N-24		
SSM2160R	-40°C to +85°C	R-24		
SSM2161N	-40°C to +85°C	N-20		
SSM2161R	-40°C to +85°C	R-20		

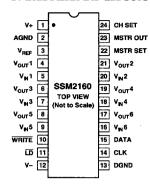
^{*}N = Plastic DIP; R = SOIC. For outline information see Package Information section.

CAUTION.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2160/SSM2161 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



24-Lead Plastic DIP and SOIC



SSM2161 PIN CONFIGURATION

20-Lead Plastic DIP and SOIC

V4. 1 AGND 2 V _{REF} 3 V _{OUT} 4 V _N 1 5 V _{OUT} 3 6 V _N 3 7 VNRTE 8 UD 9 V- 10	SSM2161 TOP VIEW (Not to Scale)	20 19 18 17 16 15 14 13 12	CH SET MSTR OU MSTR SE V _{OUT} ² V _N ² V _{OUT} ⁴ V _N ⁴ DATA CLK DGND



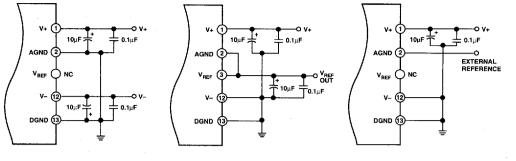
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SSM2160 POWER SUPPLY CONNECTIONS

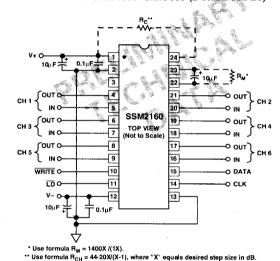


Dual Supply

Single Supply

Single Supply Using External Reference

TYPICAL APPLICATION CIRCUIT (DUAL SUPPLY)



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