

# JFET Input Operational Amplifiers

These low-cost JFET input operational amplifiers combine two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

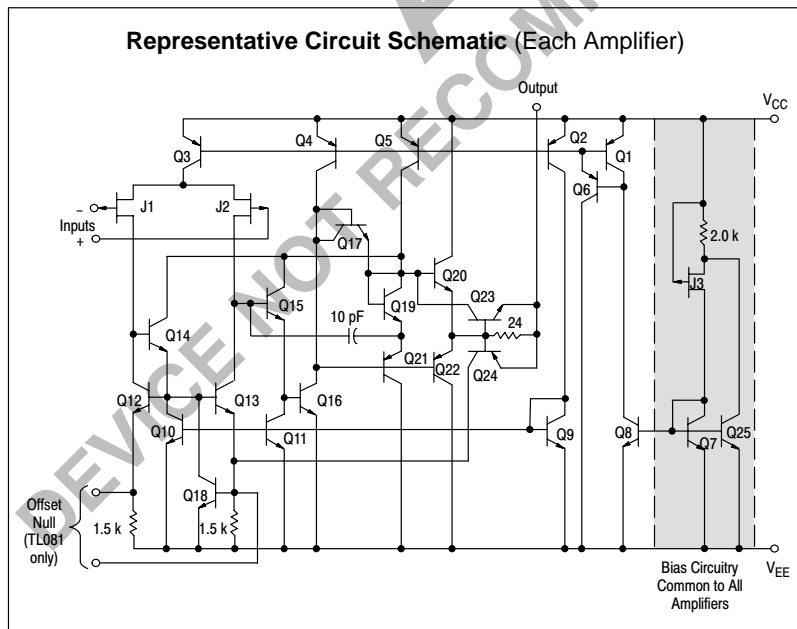
These devices are available in single, dual and quad operational amplifiers which are pin-compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

- Input Offset Voltage Options of 6.0 mV and 15 mV Max
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 5.0 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/ $\mu$ s
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance:  $10^{12} \Omega$

### ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	TL081CD	$T_A = 0^\circ$ to $+70^\circ\text{C}$	SO-8
	TL081ACP		Plastic DIP
Dual	TL082CD	$T_A = 0^\circ$ to $+70^\circ\text{C}$	SO-8
	TL082ACP		Plastic DIP
Quad	TL084CN, ACN	$T_A = 0^\circ$ to $+70^\circ\text{C}$	Plastic DIP

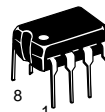
### Representative Circuit Schematic (Each Amplifier)



# TL081C,AC TL082C,AC TL084C,AC

## JFET INPUT OPERATIONAL AMPLIFIERS

### SEMICONDUCTOR TECHNICAL DATA

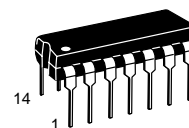
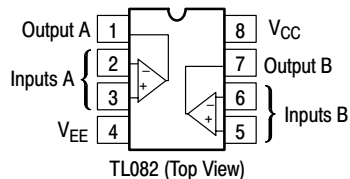
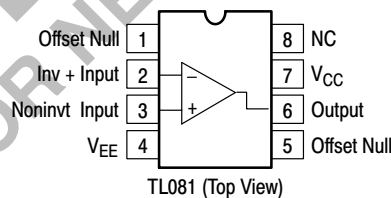


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626



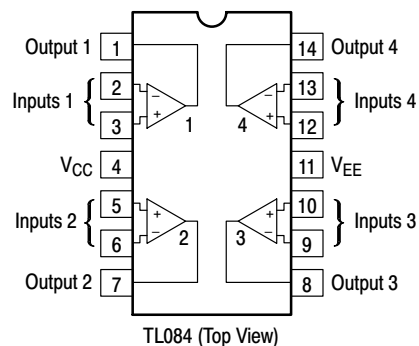
**D SUFFIX**  
PLASTIC PACKAGE  
CASE 751  
(SO-8)

### PIN CONNECTIONS



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646

### PIN CONNECTIONS



# TL081C,AC TL082C,AC TL084C,AC

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC}$	18	V
	$V_{EE}$	-18	
Differential Input Voltage	$V_{ID}$	$\pm 30$	V
Input Voltage Range (Note 1)	$V_{IDR}$	$\pm 15$	V
Output Short Circuit Duration (Note 2)	$t_{SC}$	Continuous	
Power Dissipation Plastic Package (N, P) Derate above $T_A = +47^\circ\text{C}$	$P_D$	680	mW
	$1/\theta_{JA}$	10	mW/ $^\circ\text{C}$
Operating Ambient Temperature Range	$T_A$	0 to +70	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +150	$^\circ\text{C}$

- NOTES:**
- The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.
  - The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.
  - ESD data available upon request.

## ELECTRICAL CHARACTERISTICS ( $V_{CC} = 15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = T_{low}$ to $T_{high}$ [Note 1].)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ( $R_S \leq 10\text{ k}$ , $V_{CM} = 0$ ) TL081C, TL082C TL084C TL08_AC	$V_{IO}$	-	-	20	mV
		-	-	20	
		-	-	7.5	
		-	-	-	
Input Offset Current ( $V_{CM} = 0$ ) (Note 2) TL08_C TL08_AC	$I_{IO}$	-	-	5.0	nA
		-	-	3.0	
		-	-	-	
Input Bias Current ( $V_{CM} = 0$ ) (Note 2) TL08_C TL08_AC	$I_{IB}$	-	-	10	nA
		-	-	7.0	
		-	-	-	
Large-Signal Voltage Gain ( $V_O = \pm 10\text{ V}$ , $R_L \geq 2.0\text{ k}$ ) TL08_C TL08_AC	$A_{VOL}$	15	-	-	V/mV
		25	-	-	
		-	-	-	
Output Voltage Swing (Peak-to-Peak) ( $R_L \geq 10\text{ k}$ ) ( $R_L \geq 2.0\text{ k}$ )	$V_O$	24	-	-	V
		20	-	-	

- NOTES:**
- $T_{low} = 0^\circ\text{C}$  for TL081AC,C TL082AC,C TL084AC,C  
 $T_{high} = 70^\circ\text{C}$  for TL081AC TL082AC,C TL084AC,C

- Input Bias currents of JFET input op amps approximately double for every  $10^\circ\text{C}$  rise in Junction Temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 1. Unity Gain Voltage Follower

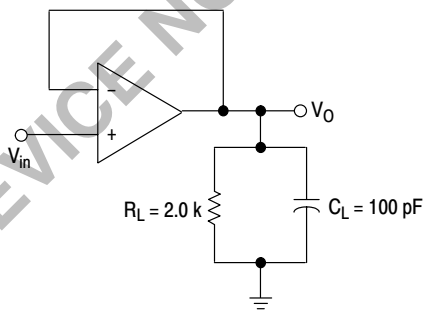
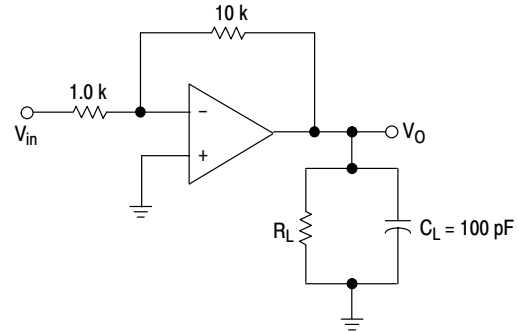


Figure 2. Inverting Gain of 10 Amplifier



# TL081C,AC TL082C,AC TL084C,AC

## ELECTRICAL CHARACTERISTICS ( $V_{CC} = 15\text{ V}$ , $V_{EE} = -15\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ( $R_S \leq 10\text{ k}$ , $V_{CM} = 0$ ) TL081C, TL082C TL084C TL08_AC	$V_{IO}$	–	5.0 5.0 3.0	15 15 6.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 50\ \Omega$ , $T_A = T_{low}$ to $T_{high}$ (Note 1)	$\Delta V_{IO}/\Delta T$	–	10	–	$\mu\text{V}/^\circ\text{C}$
Input Offset Current ( $V_{CM} = 0$ ) (Note 2) TL08_C TL08_AC	$I_{IO}$	–	5.0 5.0	200 100	pA
Input Bias Current ( $V_{CM} = 0$ ) (Note 2) TL08_C TL08_AC	$I_{IB}$	–	30 30	400 200	pA
Input Resistance	$r_i$	–	$10^{12}$	–	$\Omega$
Common Mode Input Voltage Range TL08_C TL08_AC	$V_{ICR}$	$\pm 10$ $\pm 11$	15, –12 15, –12	– –	V
Large Signal Voltage Gain ( $V_O = \pm 10\text{ V}$ , $R_L \geq 2.0\text{ k}$ ) TL08_C TL08_AC	$A_{VOL}$	25 50	150 150	– –	V/mV
Output Voltage Swing (Peak-to-Peak) ( $R_L = 10\text{ k}$ )	$V_O$	24	28	–	V
Common Mode Rejection Ratio ( $R_S \leq 10\text{ k}$ ) TL08_C TL08_AC	CMRR	70 80	100 100	– –	dB
Supply Voltage Rejection Ratio ( $R_S \leq 10\text{ k}$ ) TL08_C TL08_AC	PSRR	70 80	100 100	– –	dB
Supply Current (Each Amplifier)	$I_D$	–	1.4	2.8	mA
Unity Gain Bandwidth	BW	–	4.0	–	MHz
Slew Rate (See Figure 1) $V_{in} = 10\text{ V}$ , $R_L = 2.0\text{ k}$ , $C_L = 100\text{ pF}$	SR	–	13	–	V/ $\mu\text{s}$
Rise Time (See Figure 1)	$t_r$	–	0.1	–	$\mu\text{s}$
Overshoot ( $V_{in} = 20\text{ mV}$ , $R_L = 2.0\text{ k}$ , $C_L = 100\text{ pF}$ )	OS	–	10	–	%
Equivalent Input Noise Voltage $R_S = 100\ \Omega$ , $f = 1000\text{ Hz}$	$e_n$	–	25	–	$\text{nV}/\sqrt{\text{Hz}}$
Channel Separation $A_V = 100$	CS	–	120	–	dB

**NOTES:** 1.  $T_{low} = 0^\circ\text{C}$  for TL081AC,C TL082AC,C TL084AC,C  
 $T_{high} = 70^\circ\text{C}$  for TL081AC TL082AC,C TL084AC,C

2. Input Bias currents of JFET input op amps approximately double for every  $10^\circ\text{C}$  rise in Junction Temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 3. Input Bias Current versus Temperature

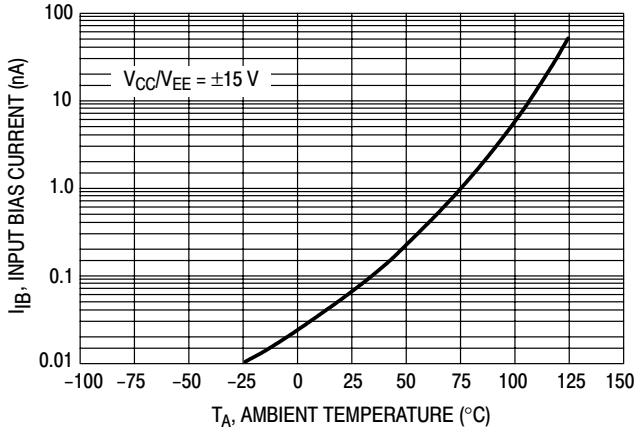


Figure 4. Output Voltage Swing versus Frequency

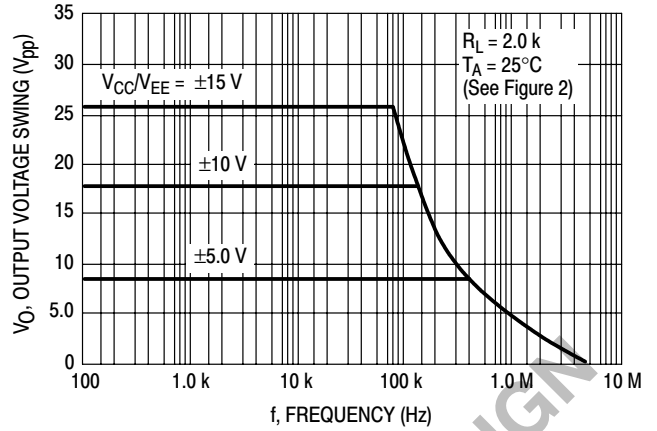


Figure 5. Output Voltage Swing versus Load Resistance

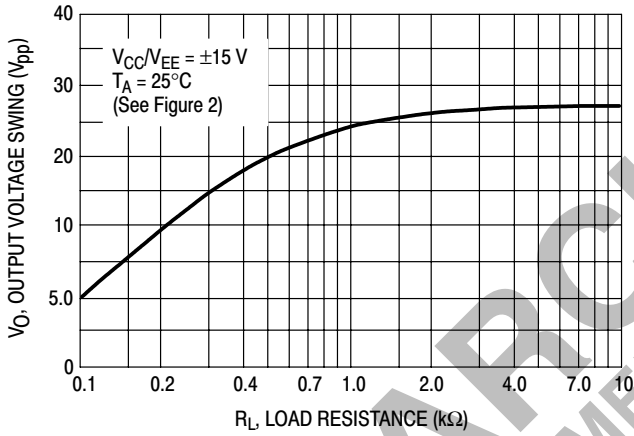


Figure 6. Output Voltage Swing versus Supply Voltage

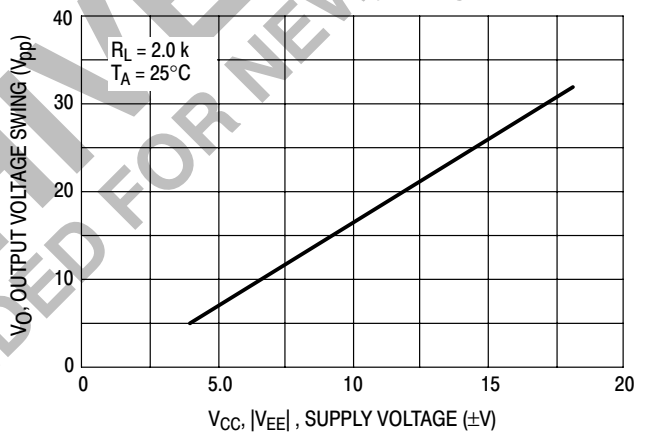


Figure 7. Output Voltage Swing versus Temperature

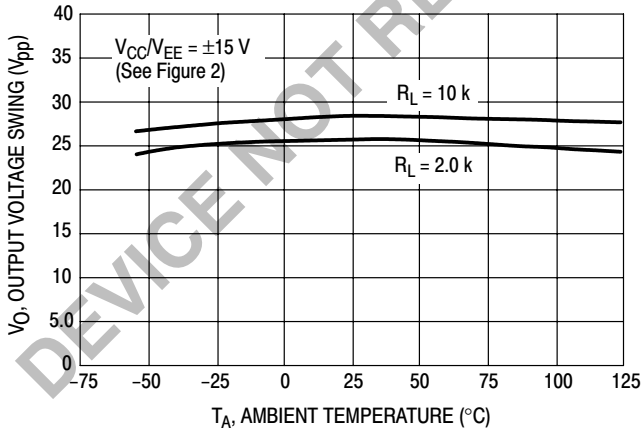


Figure 8. Supply Current per Amplifier versus Temperature

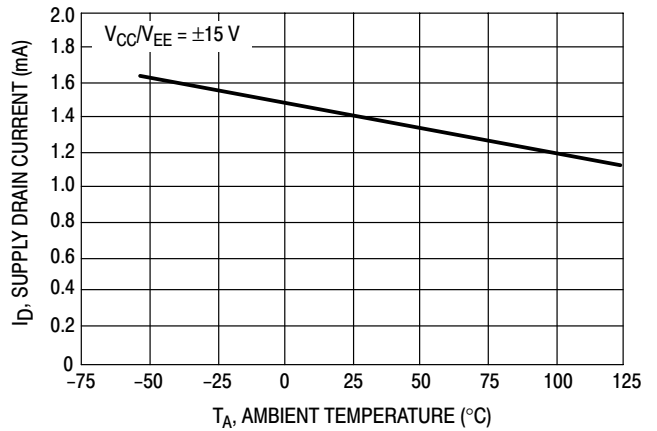


Figure 9. Large Signal Voltage Gain and Phase Shift versus Frequency

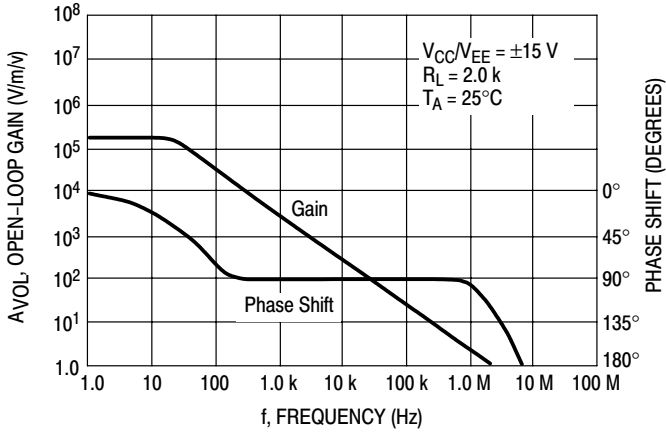


Figure 10. Large Signal Voltage Gain versus Temperature

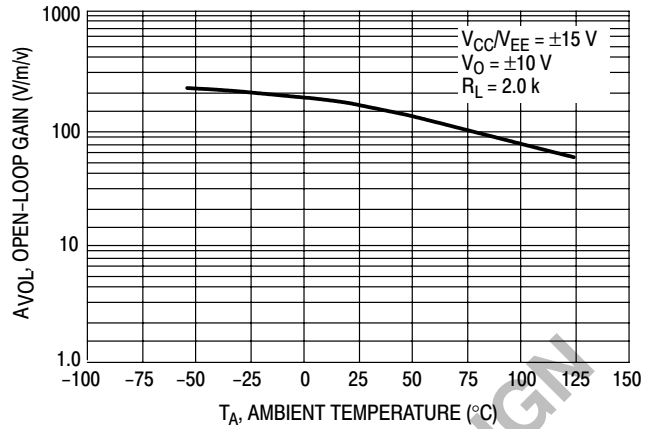


Figure 11. Normalized Slew Rate versus Temperature

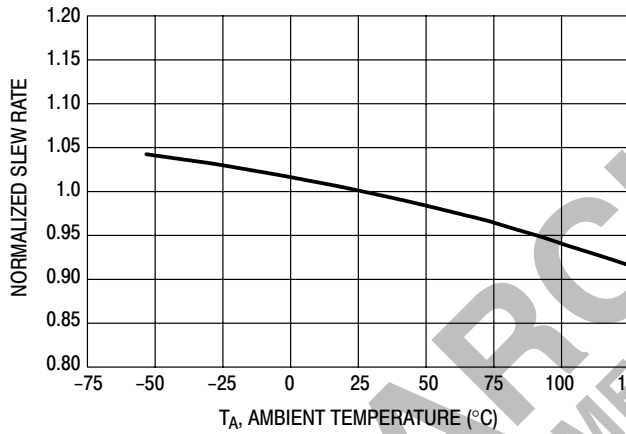


Figure 12. Equivalent Input Noise Voltage versus Frequency

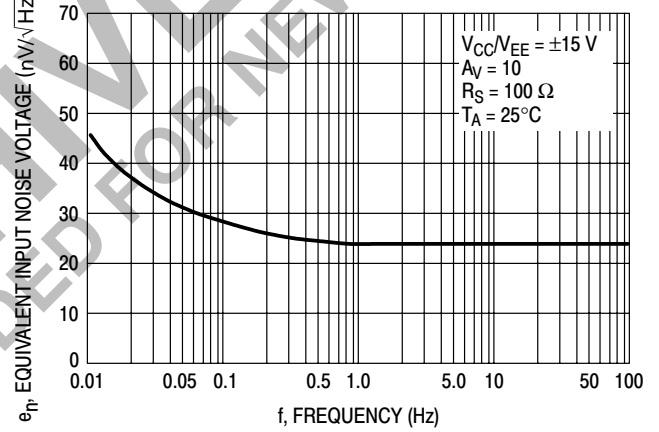
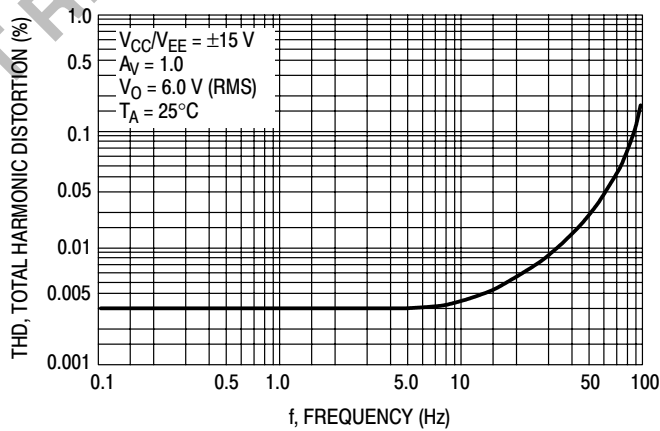


Figure 13. Total Harmonic Distortion versus Frequency



# TL081C,AC TL082C,AC TL084C,AC

Figure 14. Positive Peak Detector

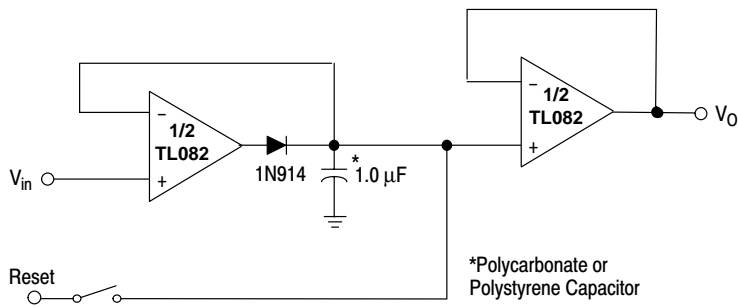


Figure 15. Voltage Controlled Current Source

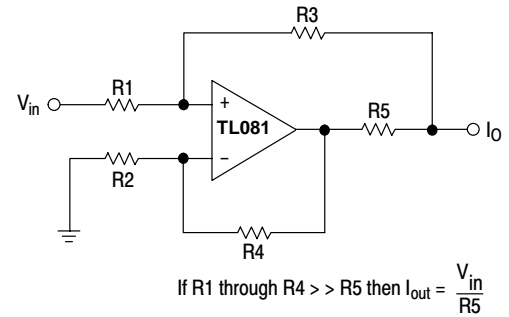
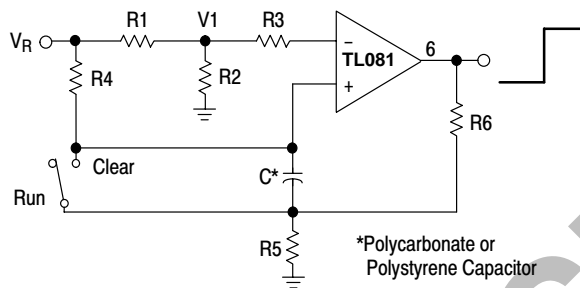


Figure 16. Long Interval RC Timer

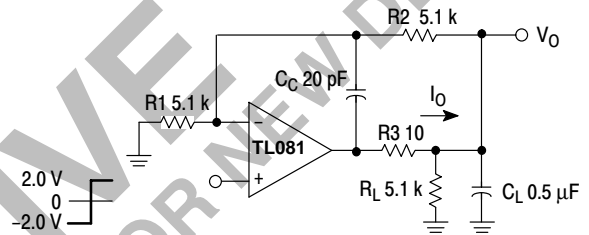


$$\text{Time (t)} = R4 C \ln \left( \frac{V_R}{V_R - V_i} \right), R3 = R4, R5 = 0.1 R6$$

If  $R1 = R2$ :  $t = 0.693 R4 C$

Design Example: 100 Second Timer  
 $V_R = 10 \text{ V}$     $C = 1.0 \text{ mF}$     $R3 = R4 = 144 \text{ M}$   
 $R6 = 20 \text{ k}$     $R5 = 2.0 \text{ k}$     $R1 = R2 = 1.0 \text{ k}$

Figure 17. Isolating Large Capacitive Loads



- Overshoot < 10%
- $t_s = 10 \mu\text{s}$
- When driving large  $C_L$ , the  $V_O$  slew rate is determined by  $C_L$  and  $I_{O(max)}$ :

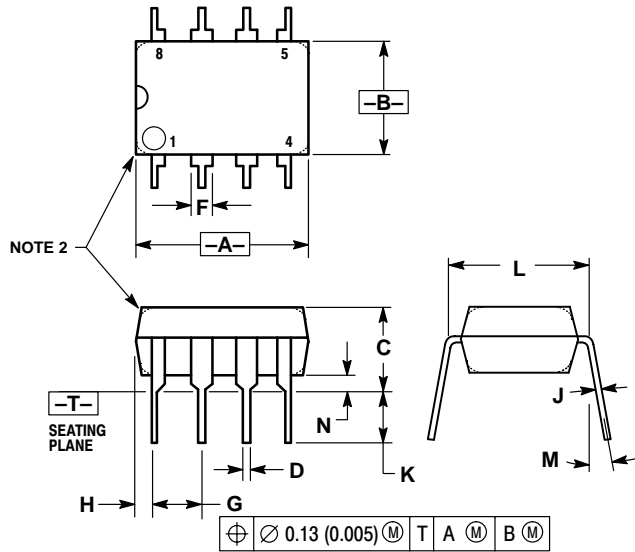
$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} \cong \frac{0.02}{0.5} \text{ V}/\mu\text{s} = 0.04 \text{ V}/\mu\text{s} \text{ (with } C_L \text{ shown)}$$

ARCHIVE FOR NEW DESIGN  
 DEVICE NOT RECOMMENDED

# TL081C,AC TL082C,AC TL084C,AC

## OUTLINE DIMENSIONS

**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 626-05  
 ISSUE K

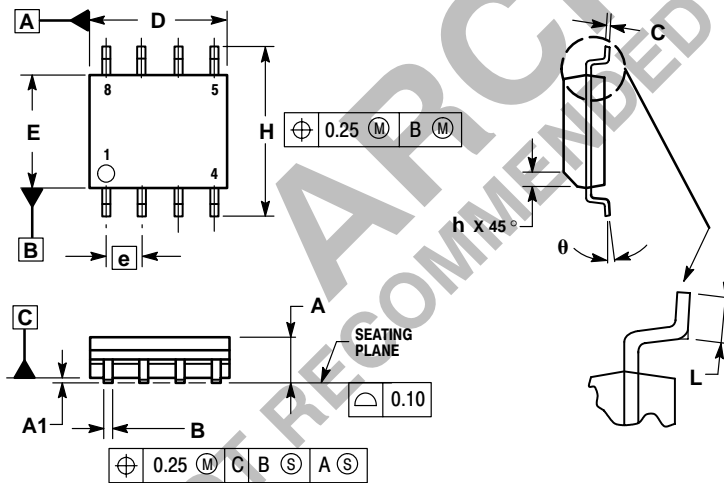


**NOTES:**

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

**D SUFFIX**  
 PLASTIC PACKAGE  
 CASE 751-05  
 (SO-8)  
 ISSUE S



**NOTES:**

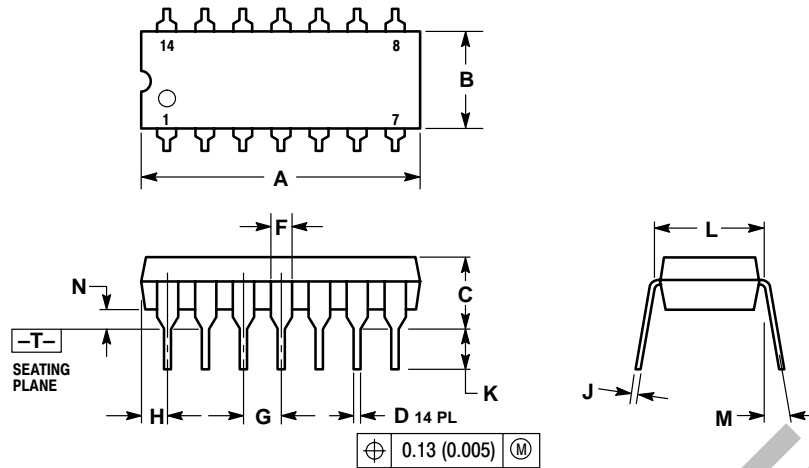
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
$\theta$	0°	7°

# TL081C,AC TL082C,AC TL084C,AC

## OUTLINE DIMENSIONS

**N SUFFIX**  
**PLASTIC PACKAGE**  
 CASE 646-06  
 ISSUE M



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---		10°	
N	0.015	0.039	0.38	1.01

**ON Semiconductor** is a trademark and **ON** is a registered trademark of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

### PUBLICATION ORDERING INFORMATION

#### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.