Preliminary

T-75-15

Am2091

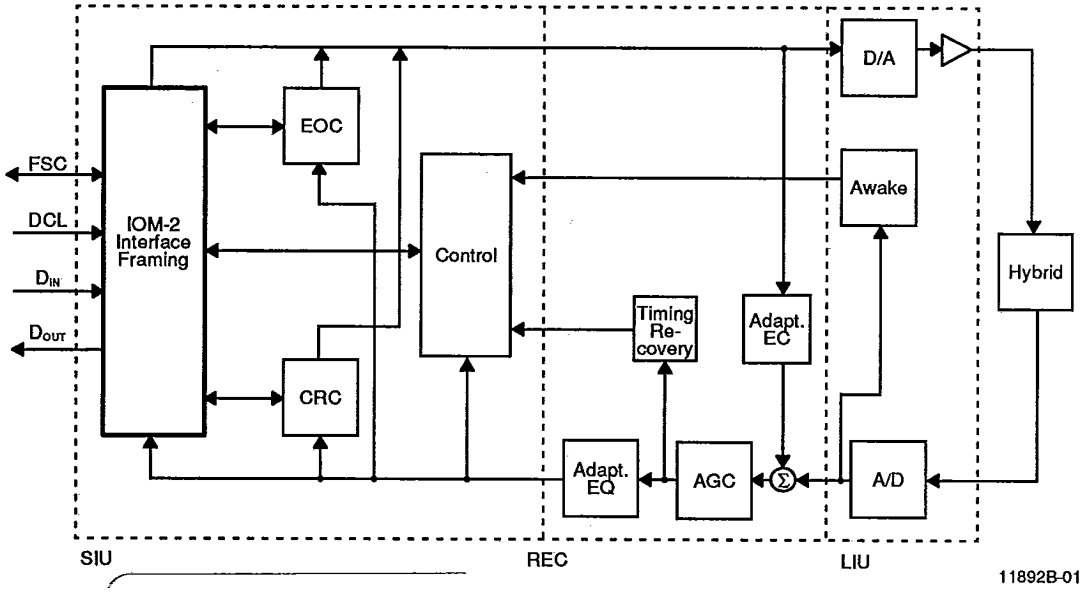
ISDN Echocancellation Circuit (IEC-Q)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Full duplex data transmission and reception at the U reference point according to the Layer 1 Specification of the American National Standard Institute ANSI® T1.601-1988**
  - –144 kb/s user bit rate over a two-wire subscriber loop
  - –2B1Q block code (2 binary, 1 quaternary)
  - –4 kb/s maintenance channel for execution of data loop back commands and monitoring transmission errors
  - –Activation and deactivation procedure
  - –Satisfies transmission requirements for loops 1–15 of ANSI's 15 telephone plant test loops
- **IOM-2™ Interface**
  - –Optimized for working in conjunction with SBCX™, EPIC™ and IDEC™ telecom IC's
  - –Handling of the commands and indications contained in the IOM-2 C/I channel for deactivation, activation, supervision of power supply unit and equipment for testing
  - –Data available via Monitor channel:
    CRC transmission errors
    Measurement value of the loop current
    Echo Canceller coefficients and internal status values
  - –Switching test loops
  - –Generation of synchronized 7.68-MHz clock for SBCX in NT mode
- **Adaption of internal interfaces to the current signal direction by programmable operational modes:**
  - –LT: Line termination in public or private exchange
  - –TE: Terminal mode
  - –NT: Network termination connected to SBCX
  - –NT-PABX: Trunk module (TDM)
- **Built in wake-up unit for activation from power-down state**
- **Adaptive echocancellation**

SIMPLIFIED BLOCK DIAGRAM



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DISTINCTIVE CHARACTERISTICS (continued)

- **Adaptive equalization**
- **Automatic polarity adaption**
- **Clock recovery (frame and bit synchronization) in all applications**
- **Automatic gain control**
- **Low-power consumption:**

  standby: 35 mW
  active: 290 mW (Am2091)
  150 mW (Am20911)

- **40-pin DIP package (Am20911)**
- **24-pin DIP package (Am20912)**
- **44-pin PLCC package (Am2091)**

  Note: The Am2091 is the one-chip version of the Am20911 and Am20912

GENERAL DESCRIPTION

Different hardware configurations as well as different operating modes of the IEC-Q™ are selectable to cope with the different system requirements.

Together with the EPIC, performing the control of the C/I channel, B-channel slot assignment and the Monitor channel handling and together with the IDEC, a HDLC controller for four independent D channels, an LT configuration with up to 8 IEC-Q devices can be built.

By using the SBCX (four-wire S/T bus interface) a complete NT1 Network Termination can be built with only two devices. If intelligent maintenance functions are required, the SBCX is replaced by the ISAC-S™ which provides microcontroller access to the IOM-2 control channels (MON, C/I).

With Voice/Data modules such as DSC Digital Subscriber Controller™ and ITAC™ Terminal Adapter Circuit a complete TE configuration can be built in a cost effective manner.

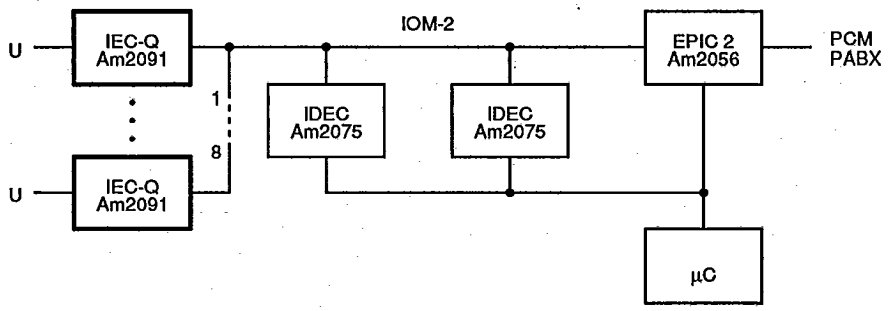

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Figure 1. LT Application

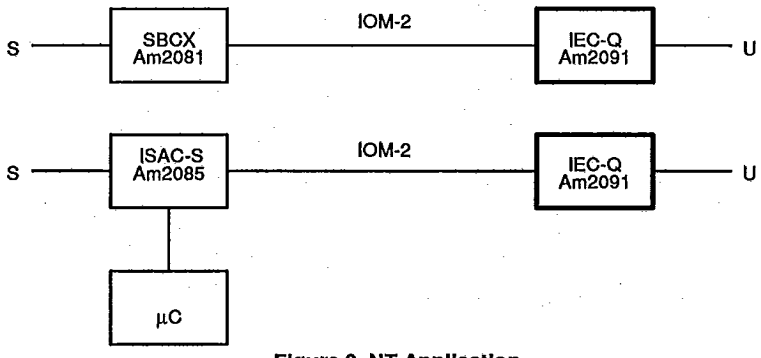

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Figure 2. NT Application

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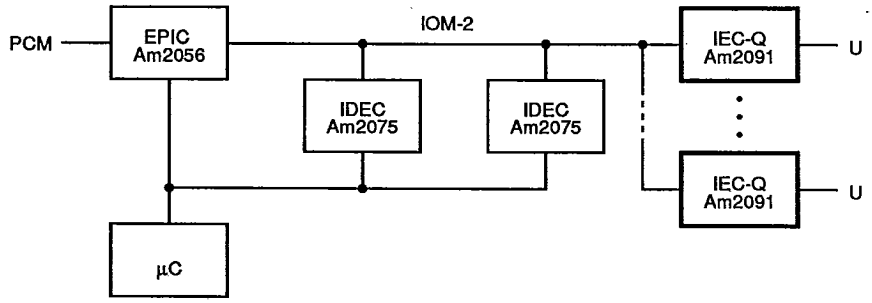

The basic timing is generated by the IEC-Q.

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Figure 3. NT-PABX Application

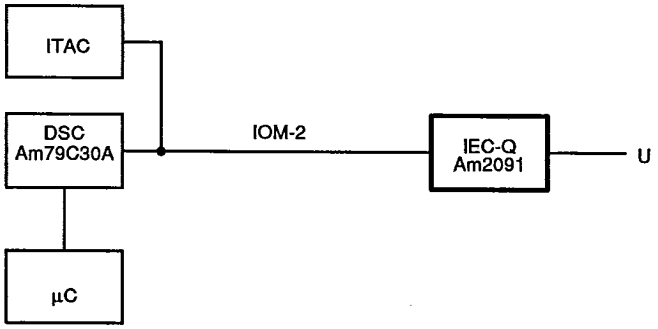

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Figure 4. TE Mode

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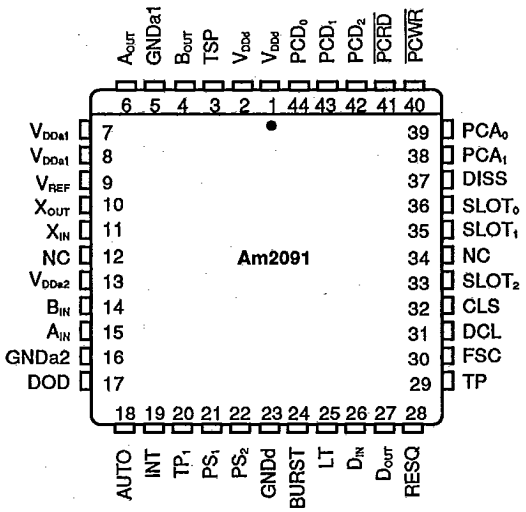
CONNECTION DIAGRAMS
Top View

44-Pin PLCC



Note: Pin 1 is marked for orientation.

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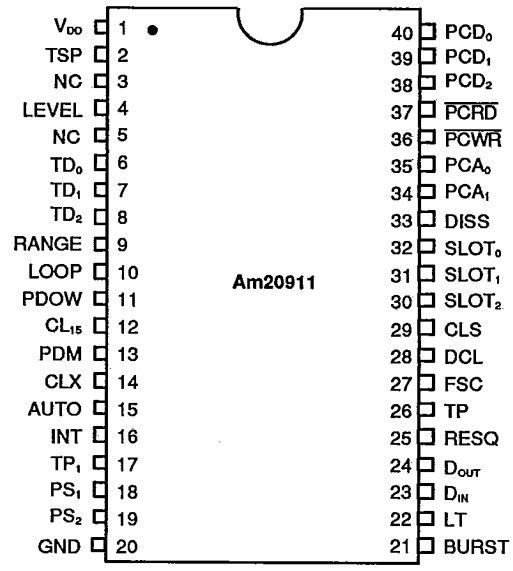
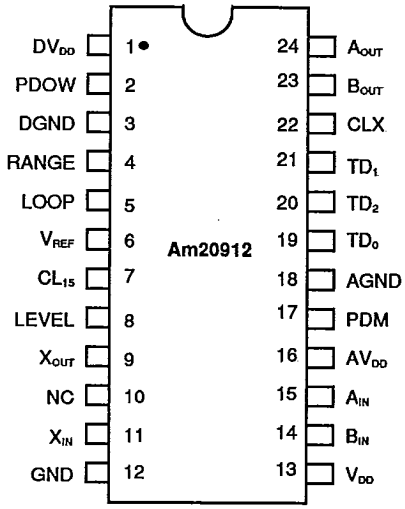
CONNECTION DIAGRAMS (continued)

40-Pin DIP



24-Pin DIP



Note: Pin 1 is marked for orientation.

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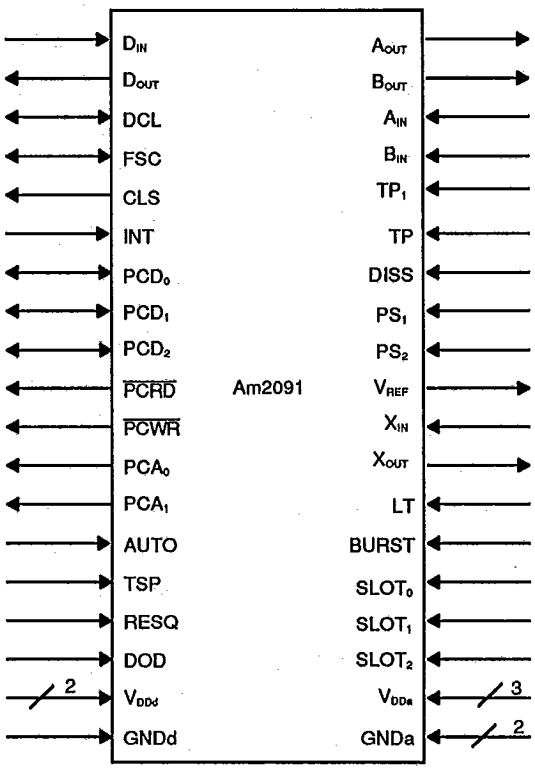
LOGIC SYMBOL



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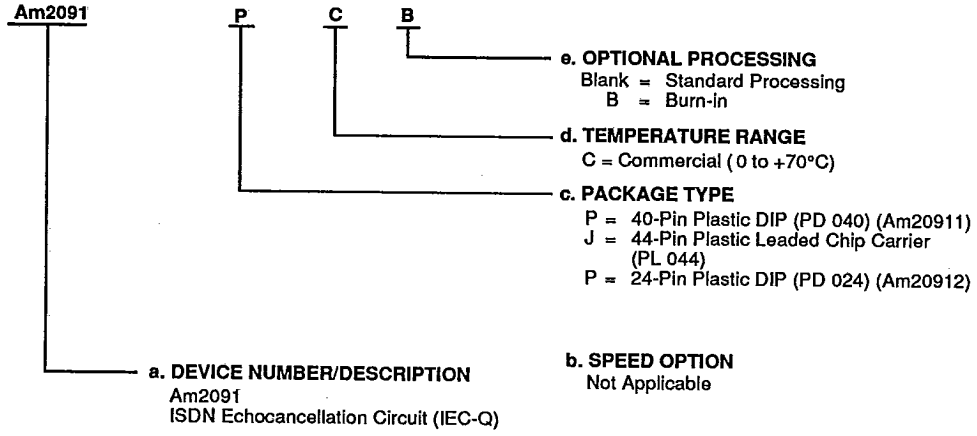
ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2091	JC, JCB
AM20911	PC, PCB
AM20912	PC, PCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

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Am2091 PIN DESCRIPTION

A_{IN}
(Input)
Received line signal to hybrid.

A_{OUT}
(Output)
Transmitted line signal to hybrid.

AUTO
(Input)
Auto/transparent mode selection of EOC (automode = High).

B_{IN}
(Input)
Received line signal to hybrid.

B_{OUT}
(Output)
Transmitted line signal to hybrid.

BURST
(Input)
NT, NT-TE mode = Low. LT, NT-PABX mode = High.

CLS
(Output)
TE/NT: 7.68-MHz clock out synchronous to line signal. NT-PABX: 512-kHz clock out synchronous to line signal.

DCL
(Input/Output)
IOM-2 device clock.

D_{IN}
(Input)
IOM-2 data input synchronous to DCL.

DISS
(Output)
Disable supply (active High).

***DOD**
(Input)
D_{OUT} open drain (High); internal pull-up resistor at D_{OUT} (Low).

D_{OUT}
(Output)
IOM-2 data output synchronous to DCL.

FSC
(Input/Output)
IOM-2 frame clock.

GNDa1
0-V analog ground.

GNDa2
0-V analog ground.

GNDd
0-V digital ground.

INT
(Input)
Controller interface interrupt must be clamped to Low during normal operation.

LT
(Input)
LT mode. (High input = LT mode; Low input = NT mode.)

NC
Not connected.

***PCA_0**
(Output)
Power Controller interface address bus.

***PCA_1**
(Output)
Power Controller interface address bus.

***PCD_0**
(Input/Output)
Power Controller interface data bus (MSB, do not connect if not used; internal pull-up).

***PCD_1**
(Input/Output)
Power Controller interface data bus (do not connect if not used; internal pull-up).

***PCD_2**
(Input/Output)
Power Controller interface data bus (LSB, do not connect if not used; internal pull-up).

***$\overline{PCRD}$**
(Output)
Power Controller interface read request (active Low).

***$\overline{PCWR}$**
(Output)
Power Controller interface write request (active Low).

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PS_1
(Input)
NT: Power Status (primary).

LT: PFOFF, Power Feed Off. Must be clamped to Low if not used.

PS_2
(Input)
NT: Power Status (secondary).

LT: Monitor Power Feed (active High). Serial data of Power Feed Current.

RESQ
(Input)
Power On Reset (active Low) must be Low at least 300 µs. The clock on the DCL pin has to be applied during RESET in the LT mode and in the NT-PABX mode. Clamp to High if not used.

$SLOT_0$
(Input)
256 kb/s modes select. Allocation of time slot for BURST mode.

$SLOT_1$
(Input)
256 kb/s modes select. Allocation of time slot for BURST mode.

$SLOT_2$
(Input)
256 kb/s modes select. Allocation of time slot for BURST mode.

TP
(Input)
Test Pin (do not connect; internal pull-down).

TP_1
(Input)
Test Pin (digital loop, do not connect; internal pull-down).

TSP
(Input)
Test Single Pulses must be clamped to Low if not used.

V_{DDa1}
5-V ±5% analog supply voltage.

V_{DDa2}
5-V ±5% analog supply voltage.

V_{DDd}
5-V ±5% digital supply voltage.

V_{REF}
(Output)
V_{REF} pin to buffer internally generated voltage with capacitor 10 nF versus GNDa.

X_{IN}
(Input)
In all NT modes, crystal connection. In all LT modes, 15.36-MHz clock input synchronized to IOM™ clocks.

X_{OUT}
(Output)
In all NT modes, crystal connection. In all LT modes, to be left open.

*Note: These pins are switched as test pins (I/O) during test condition.

For DOD = 1: D_{OUT} open drain output (external pull-up)
For DOD = 0: D_{OUT}

	Binary Equivalent D_{OUT}	D_{OUT} in SLOT Position	D_{OUT} in /SLOT Position
RESQ = 0	0	Low	Internal pull-up
	1	Internal pull-up	Internal pull-up
RESQ = 1	0	Low	High Z
	1	High	High Z

RESQ	TSP	Mode
0	0	RESET
0	1	Data Through
1	0	Normal
1	1	Test Single Pulses

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Am20911 PIN DESCRIPTIONS

The Am20911 is the digital part of the IEC-Q containing the SIU (System Interface Unit) and REC (Receiver blocks) in a 40-pin DIP package. Specified functions and timing requirements are identical to those for the one-chip (Am2091) solution.

AUTO
(Input)

Auto/transparent mode selection of EOC (automode = High).

BURST
(Input)

NT, NT-TE mode = Low. LT, NT-PABX mode = High.

CLS
(Output)

TE/NT: 7.68-MHz clock out synchronous to line signal.

NT-PABX: 512-kHz clock out synchronous to line signal.

CLX
(Output)

Transmit clock to Am20912.

CL_{15}
(Input)

15.36-MHz input clock connected to CL_{15} pin of Am20912 in proposed application.

DCL
(Input/Output)

IOM-2 device clock.

D_{IN}
(Input)

IOM-2 data input synchronous to DCL.

DISS
(Output)

Disable supply (active High).

D_{OUT}
(Output)

IOM-2 data output synchronous to DCL.

FSC
(Input/Output)

IOM-2 frame clock.

GNDd

0-V digital ground.

INT
(Input)

Controller interface interrupt pin must be clamped during normal operation.

LEVEL
(Input)

Level signal connected to LEVEL output of Am20912 during normal operation.

LOOP
(Output)

Analog loop if active High (to Am20912).

LT
(Input)

LT mode. (High input = LT mode; Low input = NT mode.)

NC

Not connected.

*PCA_0
(Output)

Power Controller interface address bus.

*PCA_1
(Output)

Power Controller interface address bus.

*PCD_0
(Input/Output)

Power Controller interface data bus (do not connect if not used; internal pull-up).

*PCD_1
(Input/Output)

Power Controller interface data bus (do not connect if not used; internal pull-up).

*PCD_2
(Input/Output)

Power Controller interface data bus (do not connect if not used; internal pull-up).

*$\overline{PCRD}$
(Output)

Power Controller interface read request (Low).

*$\overline{PCWR}$
(Output)

Power Controller interface write request (Low).

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PDM
(Input)
Output of A/D converter (15.36-MHz periods) connected to PDM pin of Am20912.

PDOW
(Output)
Power down signal active High (to Am20912).

PS_1
(Input)
NT: Power Status (primary).

LT: PFOFF, Power Feed Off. Must be clamped to Low if not used.

PS_2
(Input)
NT: Power Status (secondary).

LT: Monitor Power Feed (active High). Serial data of Power Feed Current.

RANGE
(Output)
Range signal to Am20912.

RESQ
(Input)
Power On Reset (active Low). Must be Low at least 300 µs. The clock on the DCL pin has to be applied during RESET in the LT mode and in the NT-PABX mode. Clamp to High if not used.

$SLOT_0$
(Input)
256 kb/s modes select. Allocation of time slot for BURST mode.

$SLOT_1$
(Input)
256 kb/s modes select. Allocation of time slot for BURST mode.

$SLOT_2$
(Input)
256 kb/s modes select. Allocation of time slot for BURST mode.

TD0
(Output)
Quad ternary data out.

TD_1
(Output)
Quad ternary data out.

TD_2
(Output)
Quad ternary data out. Stable with falling edge of CLX.

TP
(Input)
Test Pin (do not connect; internal pull-down).

TP_1
(Input)
Test Pin (digital loop, do not connect; internal pull-down).

TSP
(Input)
Test Single Pulses must be clamped to Low if not used.

V_{DDd}

5-V ±5% digital supply voltage.

*Note: These pins are switched as test pins (I/O) during test condition.

TD_0	TD_1	TD_2	Signal Level
0	1	0	3
0	1	1	1
0	0	1	–1
0	0	0	–3
1	x	x	0

x = 1 or 0

RESQ	TSP	Mode
0	0	RESET
0	1	Data Through
1	0	Normal
1	1	Test Single Pulses

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Am20912 PIN DESCRIPTION

AGND
(Input)
Ground pin.

A_{IN}
(Input)
Received line signal from hybrid.

A_{OUT}
(Output)
Transmitted line signal to hybrid.

AV_{DD}
(Input)
V_{DD} pin.

B_{IN}
(Input)
Received line signal from hybrid.

B_{OUT}
(Output)
Transmitted line signal to hybrid.

CLX
(Input)
80-kHz clock input. Transmitter is synchronized to this clock.

CL_{15}
(Output)
15-MHz input clock. Capacitive load should be minimized.

DGND
(Input)
Ground pin.

DV_{DD}
(Input)
V_{DD} pin.

GND
(Input)
Ground pin.

LEVEL
(Output)
Detects the 0 crossing of the differential input signal and is used to activate the IEC-D.

LOOP
(Input)
Activates the analog test loop.

NC
Not connected.

PDM
(Output)
15-MHz, 1-bit output signal of the ADC in phase with CL_{16}. Changes with rising edge of CL_{15} +2–4 ns. Capacitive load should be minimized.

PDOW
(Input)
Activates power-down mode, only oscillator and level detect are operating during power-down.

RANGE
(Input)
Activates 6-dB attenuation for the ADC input signal.

TD_0
(Input)
Digital input signal to the DAC.

TD_1
(Input)
Digital input signal to the DAC.

TD_2
(Input)
Digital input signal to the DAC. TD_{2-0} must be stable with falling edge +150 ns –150 ns of CLX.

V_{DD}
(Input)
V_{DD} pin.

V_{REF}
(Output)
V_{REF} pin to buffer internally generated voltage with capacitor 10 nF versus AGND.

X_{IN}
(Input)
In all NT modes, crystal connection. In all LT modes, 15.36-MHz clock input synchronized to IOM clocks.

X_{OUT}
(Output)
In all NT modes, crystal connection. In all LT modes, to be left open.

TD_0	TD_1	TD_2	Signal Level
0	1	0	3
0	1	1	1
0	0	1	–1
0	0	0	–3
1	x	x	0

x = 1 or 0

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OPERATIONAL DESCRIPTION

Operation Modes and Functions

Table 1. Modes of Operation

	Input Pin						Output Pin Synchronized to U		Super-Frame-Marker
Mode	Burst	LT	Slot0	Slot1	Slot2	DCL	DCL	CLS	
NT	0	0	0	0	0	—	512 kHz	7.68 MHz	No*
NT	0	0	1	0	0	—	512 kHz	7.68 MHz	Yes*
TE	0	0	0	1	0	—	1.536 MHz	7.68 MHz	No*
TE	0	0	1	1	0	—	1.536 MHz	7.68 MHz	Yes*
PABX	1	0	Slot Assignment			512 kHz–4.096 MHz	—	512 kHz	
LT	1	1	Slot Assignment			512 kHz–4.096 MHz	—	—	

*Notes: 1. DCL period High phase of FSC at superframe position.
2. DCL period High phase of FSC at normal frame position (see Timing Diagram).

Interfaces

Table 2. Slot Assignment (DCL = 4.096 MHz)

Time Slot No.	Slot0	Slot1	Slot2	Bit No.
0	0	0	0	0–31
1	0	0	1	32–63
2	0	1	0	64–95
3	0	1	1	96–127
4	1	0	0	128–159
5	1	0	1	160–191
6	1	1	0	192–223
7	1	1	1	224–255

Table 3. Embedded Operation Channel Mode (EOC)

Mode	Input Pin Auto
Transparent	0
Automatic	1

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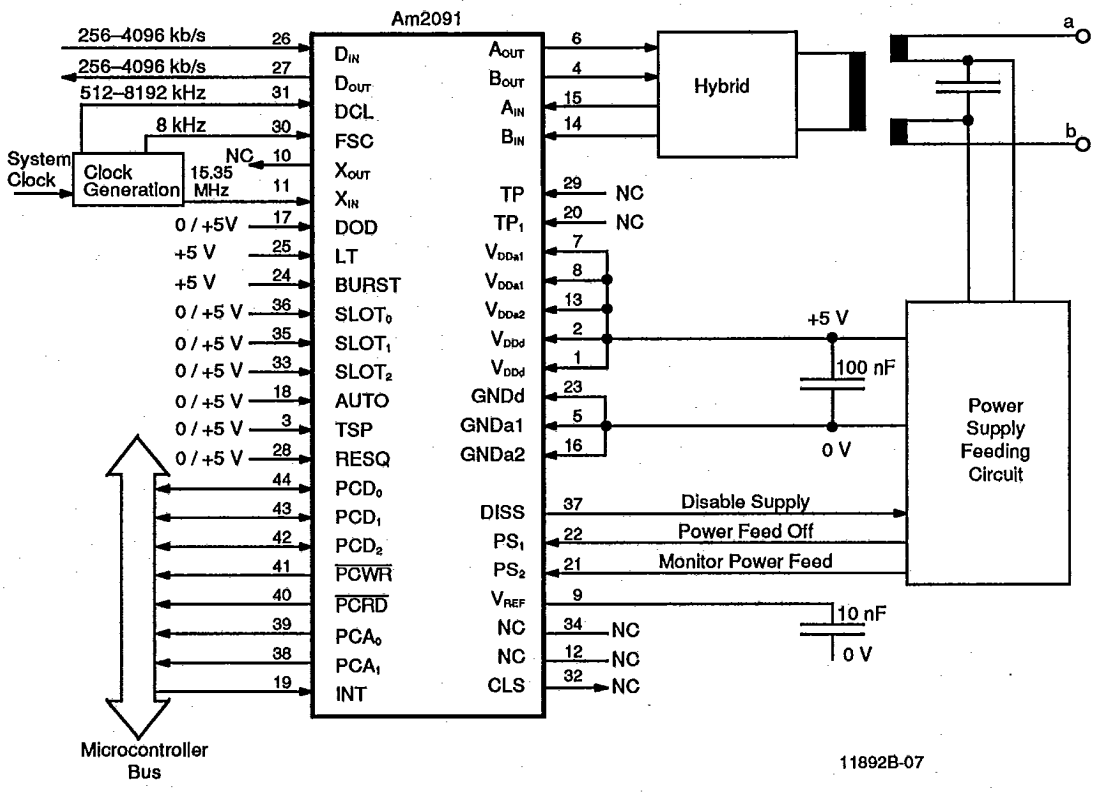

Figure 5. NT Mode

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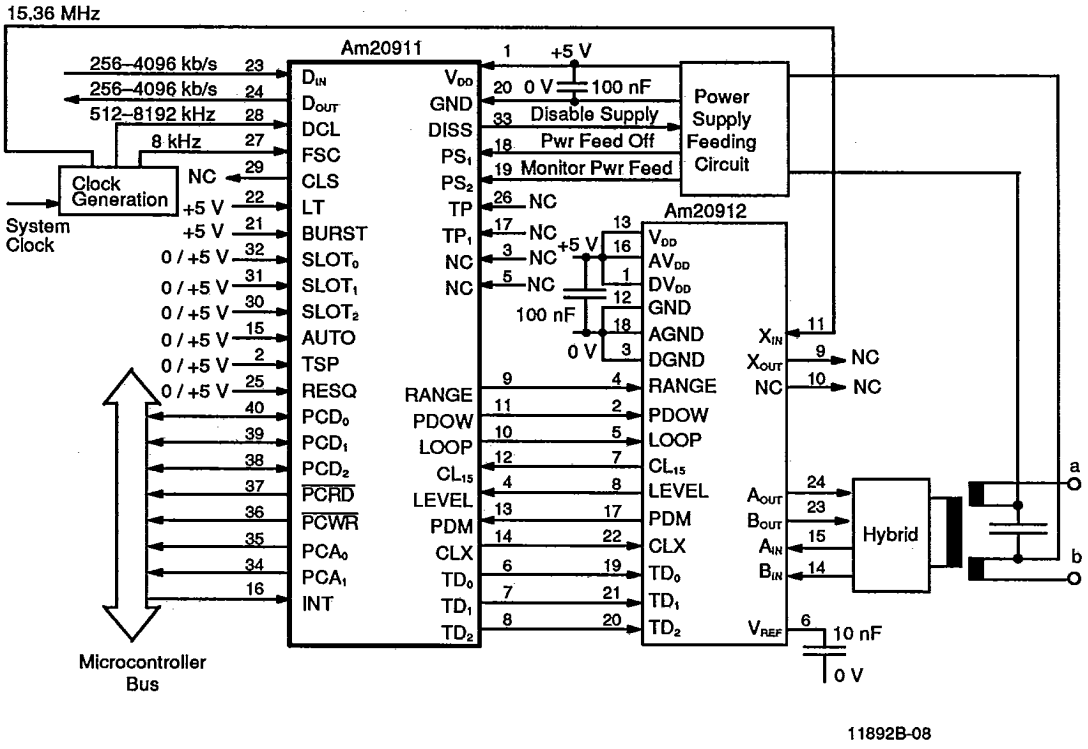

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Figure 6. NT-PABX Mode

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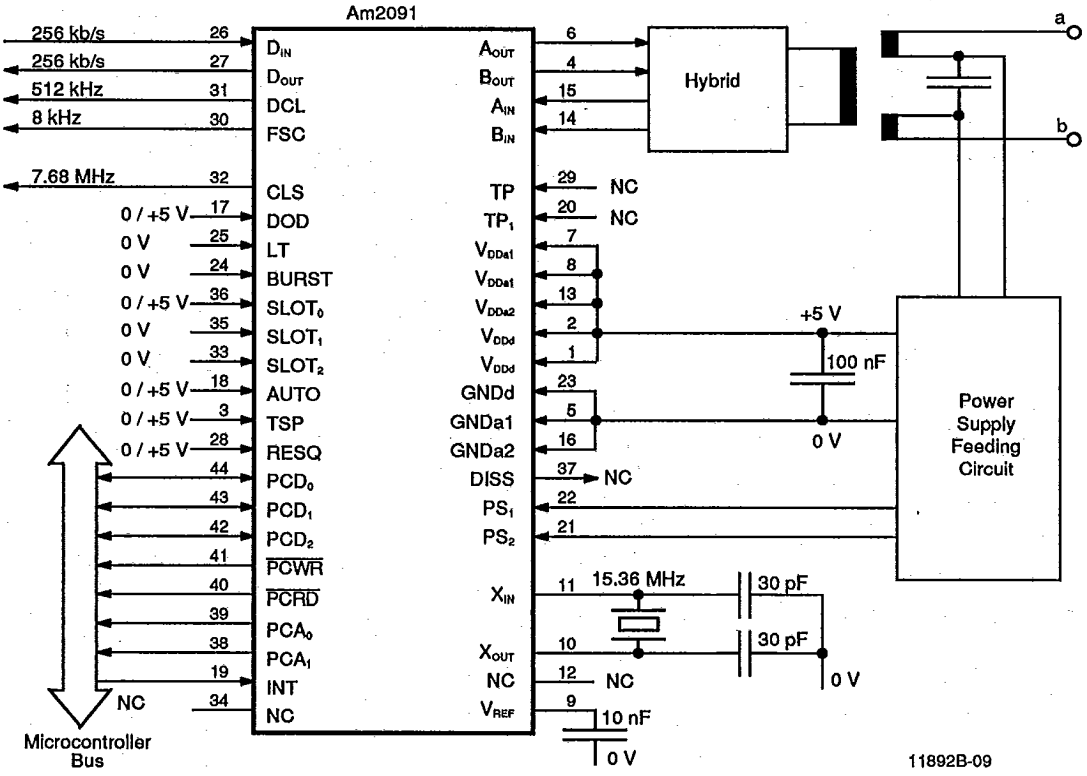

Figure 7. NT Mode

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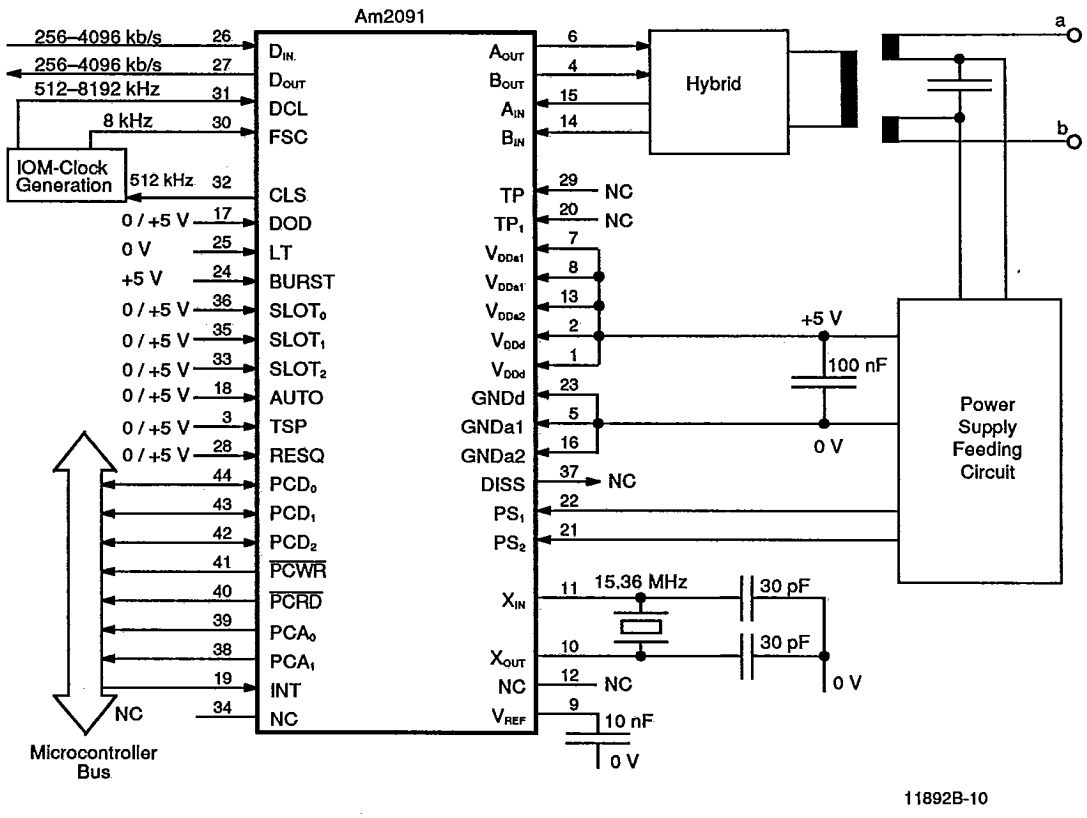

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Figure 8. NT-PABX Mode

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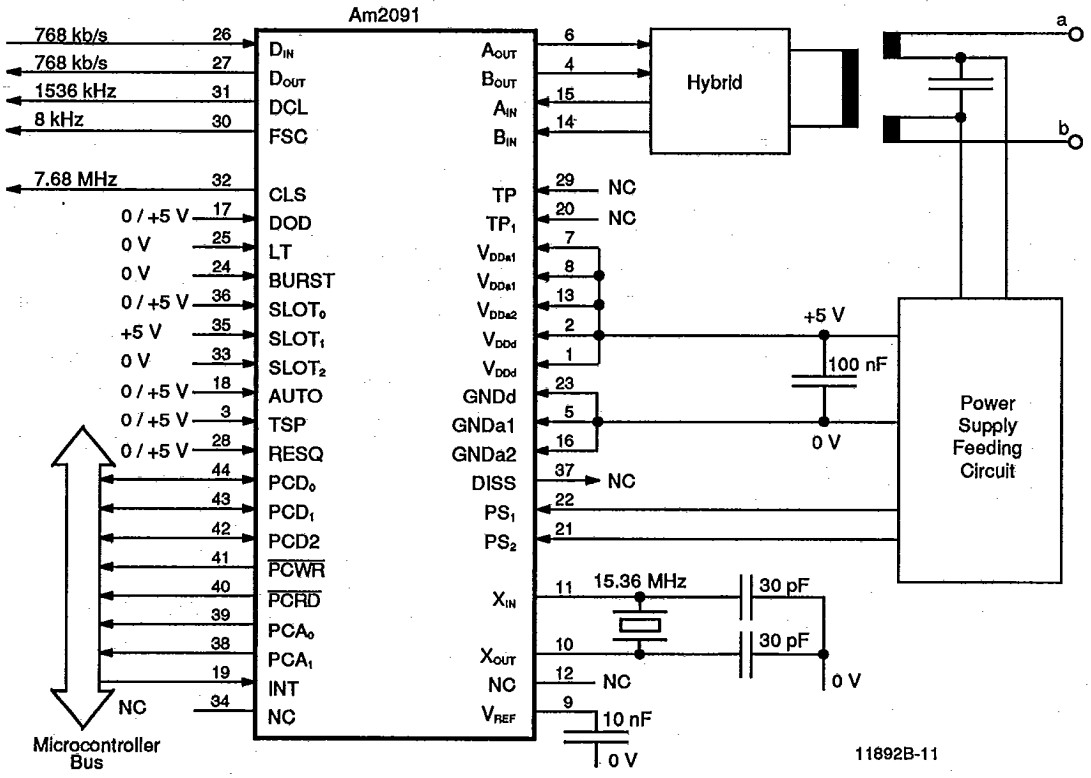

Figure 9. TE Mode

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FUNCTIONAL DESCRIPTION

The IEC-Q can be subdivided into three main blocks:

–LIU, Line Interface Unit
–SIU, System Interface Unit
–REC, Receiver

The Line Interface Unit (LIU) contains the crystal oscillator and all of the analog functions, such as the A/D converter in the receive path and the pulse-shaping D/A converter and line driver in the transmit path.

The System Interface Unit (SIU) performs the connection between the U and the IOM interface. The data channels (2B+D) are transferred after scrambling or descrambling and speed adaption to the appropriate frame. A complete activation and deactivation procedure is implemented, which is directly controlled by activation and deactivation indications from U or IOM interface. State transition of the procedure depends on the reached status of the receiver (adaption and synchronization) and timing functions to watch fault conditions.

For maintenance functions two modes can be selected. In the automode all ANSI specified EOC procedure handling and executing is performed. In the transparent mode all bits are transferred transparent to the IOM interface without any internal processing.

The Receiver block (REC) performs the filter algorithmic functions using digital signal processing techniques. Modules for echo cancellation, pre- and post-equalization, phase adaption and frame detection are implemented in a modular multi-processor concept.

The B-version of the IEC-Q is available in a One-Chip (Am2091) and a Two-Chip (Am20911 Digital, Am20912 Analog) solution.

In the first part of this data sheet the overall function of the U transceiver (One- or Two-Chip) is described.

In the second part selected information is given for the digital and analog part.

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IEC-Q INTERFACES
U Interface

Table 4. U Frame Structure

		Framing	2B+D	Overhead Bits (M1–M6)					
	Quat Positions	1–9	10–117	118s	118m	119s	119m	120s	120m
	Bit Positions	1–18	19–234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act / act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	deact. / ps1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1 / ps2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1 / ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1 / cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3 . . .									

LT-to-NT direction / NT-to-LT direction

1 = Reserve = reserve bit for future standard; set = 1
EOC = Embedded operations channel
a = Address bit
dm = Data/message indicator
i = Information (data/message)
ISW = Inverted Sync Word
SW = Sync Word

act = activation bit
ps1, ps2 = power status bits
ntm = Nt1 in Test Mode bit
crc = cyclic redundancy check covers 2B+D & M4
febe = far end block error bit
cso = cold start only
deact = deactivation

2B1Q Superframe Technique & Overhead Bit Assignments
(8 × 1.5 ms "Basic Frames" = 12 ms Superframe)

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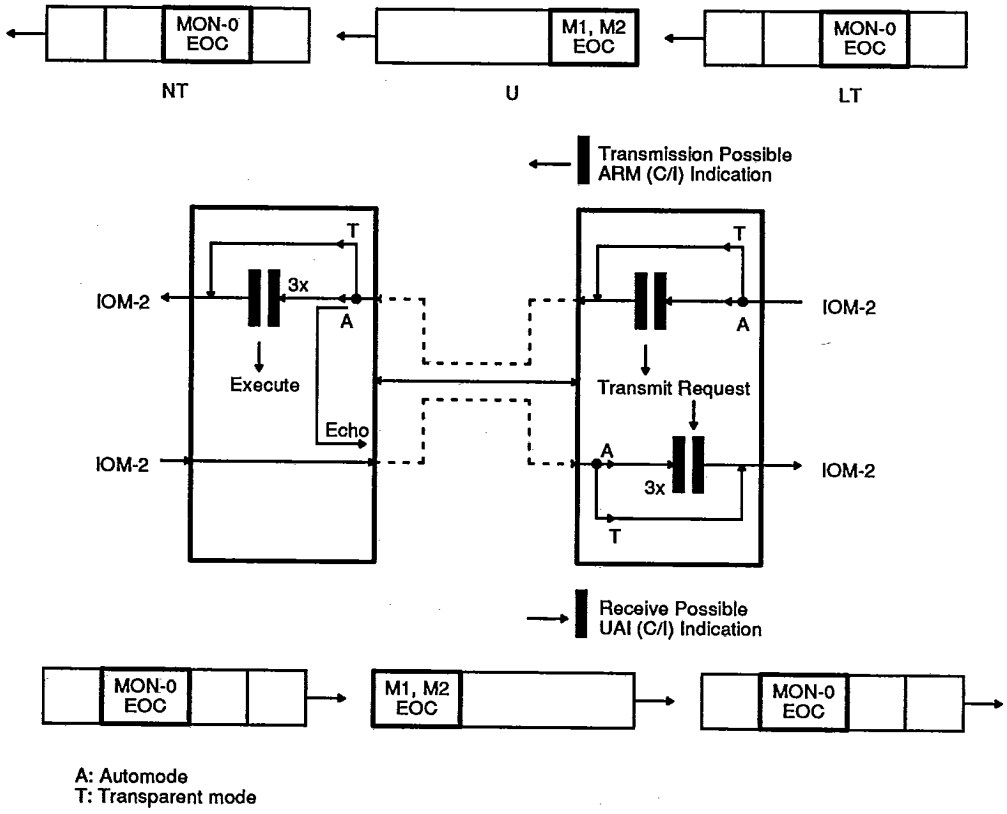
U Interface Maintenance Channel

Embedded Operation Channel (EOC)

The EOC protocol operates in a repetitive command or response mode with a triple last look and master function on the network side.

All messages are latching. That is, they will be continually executed until an RTN (return to normal) message appears.



A: Automode
T: Transparent mode

Figure 10. EOC Procedure

11892B-12

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Table 5. Frame and Functions

EOC Address Field a1	a2	a3	Data/ Message Indicator d/m	Information I1	I2	I3	I4	I5	I6	I7	I8	(o)rigin (d)estination LT	NT	Message
0	0	0												NT Address
1	1	1												Broadcast Address
			1											Message
			0											Data
			1	0	1	0	1	0	0	0	0	o	d	LBBD
			1	0	1	0	1	0	0	0	1	o	d	LB1
			1	0	1	0	1	0	0	1	0	o	d	LB2
			1	0	1	0	1	0	0	1	1	o	d	RCC
			1	0	1	0	1	0	1	0	0	o	d	NCC
			1	1	1	1	1	1	1	1	1	o	d	RTN
			1	0	0	0	0	0	0	0	0	d/o	o/d	H
			1	1	0	1	0	1	0	1	0	d	o	UTC

RTN	= Return to Normal	Releases all outstanding EOC controlled operations; reset of EOC processor to initial state.
UTC	= Unable to Comply Ack	Validates the receipt of an EOC message, but the EOC message is not in the menu of NT.
NCC	= Notify of Corrupted CRC	
RCC	= Request Corrupt CRC	
H	= Hold State	
LBBD	= Loopback B1, B2 and D	Request within NT/SBCX.
LB1/LB2	= Loopback Channel (B1 or B2)	Request within NT/IEC-Q.

Only EOC frames with data/message indicator set to 1 (message) are able to evaluate; otherwise, a UTC message will be replied.

NT Automode

For NT Automode configuration, every EOC message will be recognized and executed after receiving three identical consecutive EOC frames with correct NT address 000 or broadcast address 111. All received EOC frames are echoed back in the next transmitted EOC frame (0.75 ms frame delay) except:

- Wrong address
  In this case, the HOLD state message with NT address will be transmitted until a correctly addressed message is received.
- Message not executable
  A UTC message is transferred back after the third non-executable identical received message.

For test purposes, all EOC frames are transmitted via the IOM-2 Monitor channel, after the third correct reception.

NT Transparent Mode

For NT Transparent Mode, the received EOC frame will not be analyzed or executed but rather transmitted downstream to the IOM-2 Monitor channel. In the upstream direction, the last incoming EOC code from the IOM-2 Monitor channel is used for transmission.

LT Automode

In the LT Automode, EOC frames to be sent are taken from the IOM-2 Monitor channel and are continually transmitted until a new EOC frame is to be sent. After POWER DOWN, RESET or during start procedure, an RTN (return to normal) message is transmitted. Every new transmit request will enable the return message.The return message upstream via IOM-2 is a single transmission of an accepted EOC frame. Every EOC frame will be accepted only after first detecting 3 identical consecutive EOC frames and if the new EOC frame is different from the previously accepted one.

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LT Transparent Mode

For LT Transparent Mode the transmit procedure corresponds to the LT automode. In the receive direction, the IEC-Q is transparent to every EOC frame.

CRC Process

An error monitoring function is implemented covering the 2B+D and M4 data transmission of a U-superframe by a Cyclic Redundancy Check (CRC).

The computed polynomial is:

$$G(u) = u^{12} + u^{11} + u^3 + u^2 + u + 1$$

(+ modulo 2 addition)

The generated check digits (CRC bits CRC1, CRC2, . . ., CRC12) from the data are transmitted in the following U-superframe after the data transmission (CRC1 most significant bit). The receiver will compute the CRC of the received 2B+D and M4 data and a comparison will be done with the received CRC bits generated by the transmitter.

A CRC error will indicate a block error: FEBE (Far End Block Error) or NEBE (Near End Block Error) are set to 0 (Error) depending on the upstream or downstream direction.

The FEBE bit will be placed in the next available U-superframe transmitted to the originator.

The IEC-Q contains two error counters clocked by the far end or near end error indication.

The maximum counter value is 255; a reset is performed either during activation of the U interface or after read out. Both counter values can be read out via the Monitor channel (MON-8) of the IOM-2 interface. In the NT mode, block error indications are issued additionally by a MON-1 message every time an error has occurred.

Corrupted CRC (CCRC)

Data fault conditions can be generated for testing of the CRC procedure by manipulating the CRC reset.

A Request of Corrupted CRC (RCC) will invert the transmitted CRC bits.

The Notify of Corrupted CRC (NCC) causes the received CRC bits to be corrupted. In both test modes the error counters in the addressed chip are stopped and error indications via IOM-2 interface are retained.

In the transparent mode the EOC messages will pass through the chip without execution. There is no suppression of error counter and error messages towards the IOM interface.

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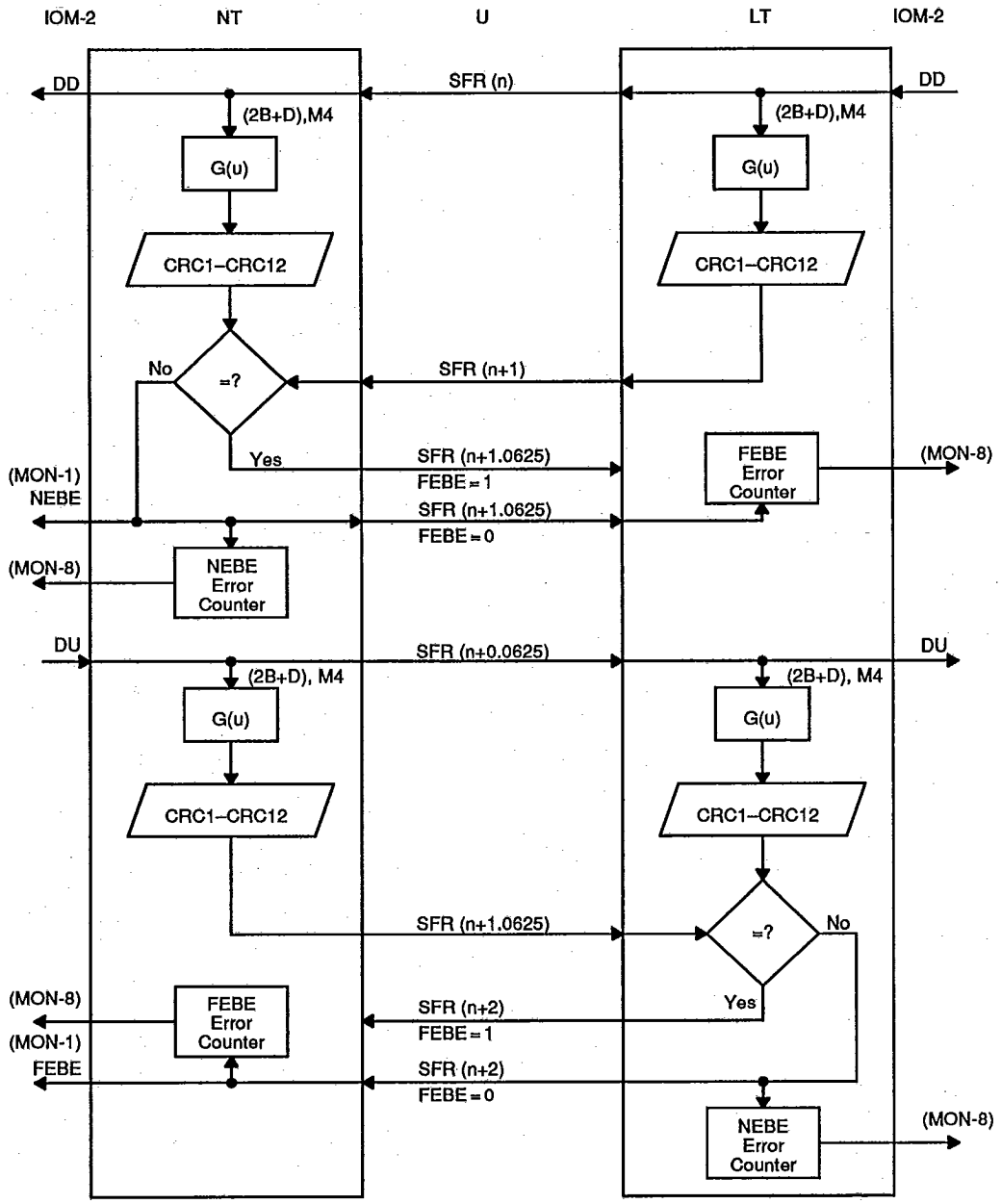

Figure 11. CRC Process 11892B-13

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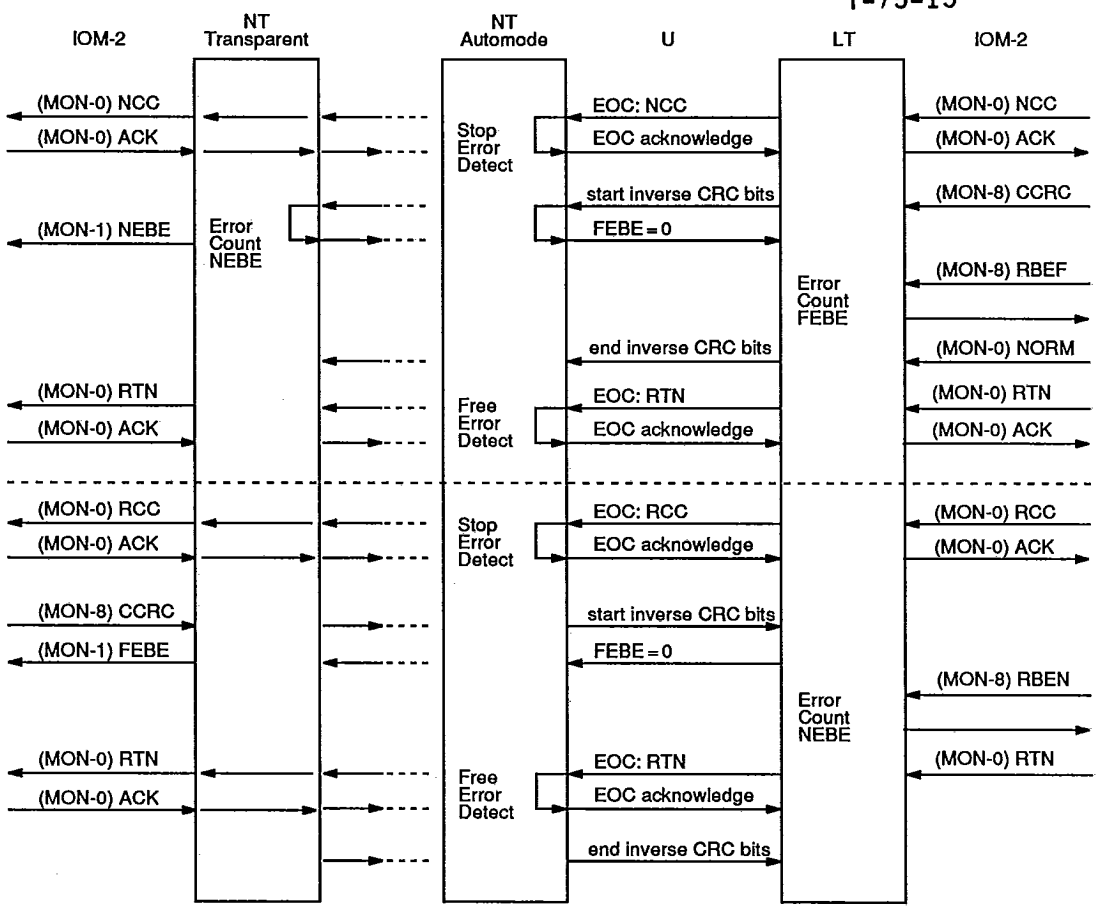

11892B-14

Figure 12. Corrupted CRC test

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T-75-15

IOM-2 Interface

The IOM-2 interface is viewed as a standard interface that interconnects different modules together in a terminal. The interface is synchronized by frame and data clock signals supplied by a master clock source. The definition of master or slave mode depends on whether the timing for the interface is received or supplied by the device.

The IOM-2 interface consists of four physical connections. Two lines are for the transmission of data, one for each direction. The other two lines are for the frame and data clocks (see Figure 13).

DU Data Upstream—Transmission of data from the subscriber side to the exchange side.

DD Data Downstream—Transmission of data from the exchange side to the subscriber side.

DCL Data Clock—Twice the data transmission frequency on DU and DD.

FSC Frame Synchronization Clock—Resets the bit counter at the start of each frame.

The downstream and upstream directions are always with respect to the exchange. From the device point of view, these connections can also be named D_{IN} and D_{OUT}, referring to the reception or transmission of data, respectively.

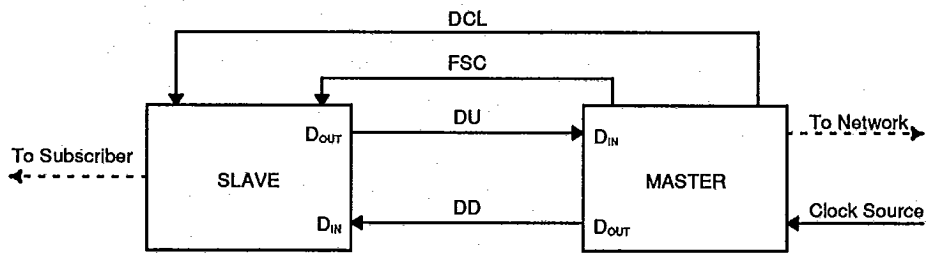

Figure 13. IOM-2 Interface Signals 11892B-15

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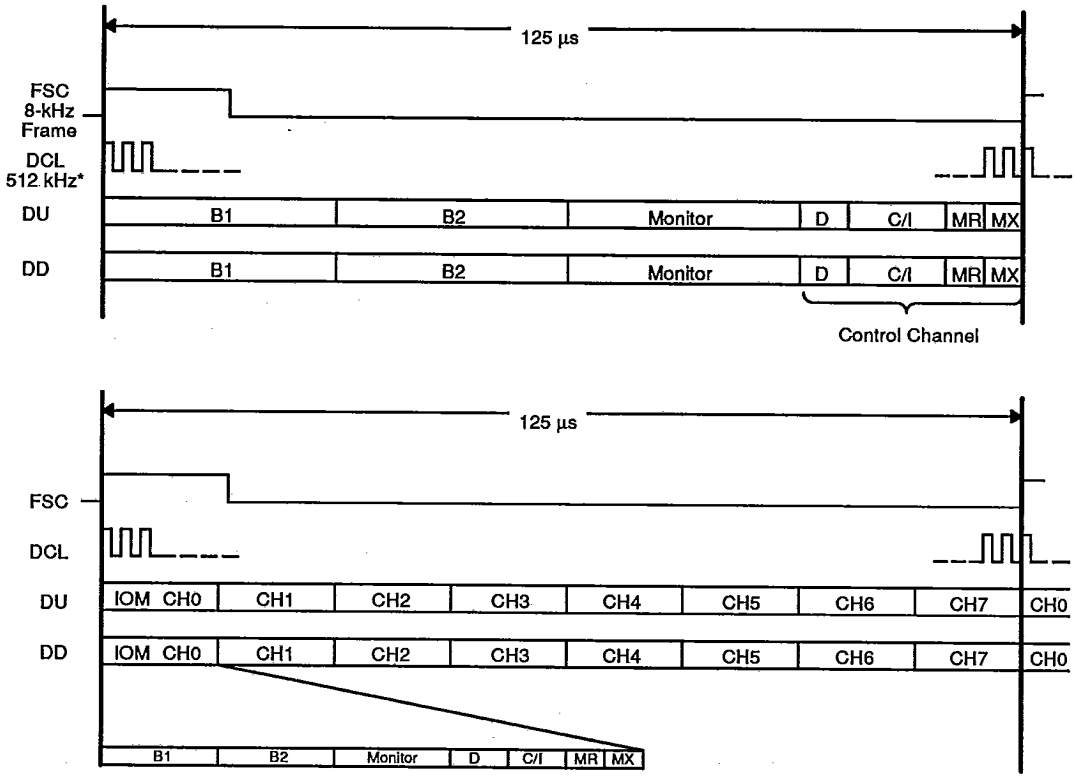

Figure 14. IOM-2 Interface Multiplexed Frame Structure (2.048 kb/s)

B1, B2: Circuit switched voice/data
D: D channel for signaling and packet switched data
C/I: Command/indication bits for control
MR, MX: Monitor handshake bits

11892B-16

*DCL is programmable for values from 512 kHz to 4.096 MHz.

IOM-2 Interface Maintenance Functions

Control/Indication Channel

The Control/Indication channel (C/I channel) is used to control the operational status of the IEC-Q and to issue corresponding indications.

In general, commands (on D_{IN}) have to be applied continuously as long as the required action is needed.

A command is validated by the IEC-Q if it has been detected in two subsequent IOM frames (double last look criterion). Indications (on D_{OUT}) are issued by the IEC-Q as long as no other indication has to be forwarded. They are not strictly state oriented.

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Table 6. C/I Channel Codes

Code	NT Mode		LT Mode	
	In	Out	In	Out
0000	TIM	DR	DR	—
0001	RES	—	RES	DEAC
0010	—	FJ	—	FJ
0011	—	—	LTD	HI
0100	EI1	EI1	RES1	RSY
0101	SSP	—	SSP	EI2
0110	DT	INT	DT	INT
0111	—	PU	—	UAI
1000	AR	AR	AR	AR
1001	—	—	—	ARM
1010	ARL	ARL	ARL	—
1011	—	—	—	EI3
1100	AI	AI	—	AI
1101	—	—	—	LSL
1110	—	AIL	—	—
1111	DI	DC	DC	DI

AI	Activation Indication
AR	Activation Request
ARL	Activation Request Local Loop
ARM	Activation Request Maintenance bits
DC	Deactivation Confirmation
DR	Deactivation Request
DEAC	Deactivation Accepted
DI	Deactivation Indication
DT	Data Through (test mode)
EI1	Error Indication 1 (error on U)
EI2	Error Indication 2 (error on S/T)
EI3	Error Indication 3 (timeout 15 s: error on U)
HI	High Impedance (set by PFOFF)
INT	Interrupt (set by power controller)
LTD	LT Disable (control of pin DISS)
LSL	Loss of Signal Level on U
UAI	U Activation Indication
RES	Circuit Reset
RES1	Receiver Reset
RSY	Loss of Synchronization
PU	Power Up
SSP	Test Mode (Send Single Pulses)
TIM	Timing Required
FJ	Frame Jump

IOM-2 MONITOR Channel

The MONITOR (MON) channel is used for the transfer of messages and data related to maintenance functions. The MX and MR bits in the fourth octet of the IOM frame are used for flow control (active Low).

Transfer Procedure

The MON channel procedure allows a full duplex transmission. The MX bit is used to start or indicate the transmission of data on the MON channel. The receipt of data is acknowledged making use of the MR bit in the reverse direction.

The procedure allows the transmission of two-byte messages or data. The first byte contains the address and possibly data while the second byte contains a message or data.

The MON channel is idle when the MX bit is inactive in two or more consecutive frames. In this case, the MR bit in the reverse direction is inactive too. In the MON channel binary 1s are transmitted. The transmission of the first byte M1 is started by the transmitter with the transition of the MX bit from inactive to active in the same frame. This is allowed only if the MR bit in the reverse direction has been in the inactive state for at least two consecutive frames.

The receiver confirms the start of the transfer procedure by setting the MR bit active if the transmitted bytes are identical in the first two received frames. It acknowledges the receipt of byte M1 by keeping the MR bit in the active state for at least one more frame.

In the frame following the transition of the MR bit from inactive to active, the transmitter starts the transfer of the second byte M2 with the transition of the MX bit from active to inactive. The MX bit stays in the inactive state for only one frame if the receipt of byte M1 has been acknowledged by the receiver.

In the next frame the receiver sets the MR bit inactive and acknowledges the receipt of byte M2 by a transition of the MR bit from inactive to active one frame later.

The transmitter sets the MX bit inactive and keeps it in the inactive state for at least one more frame. The presence of the MX bit in the inactive state for two or more consecutive frames indicates the end of the message (EOM).

In the frame following the transition of the MX bit from active to inactive, the receiver sets the MR bit inactive. As it detects the EOM, it keeps the MR bit in the inactive state until a new message is received.

If the received bytes are not identical and no EOM is detected, the receiver sends no acknowledgment to the transmitter; that is, it sets the bit inactive and keeps it in this state until it has detected the response of the transmitter (MX bit inactive in at least two frames) and until a new transfer procedure is started. In general, after starting the receive procedure, the MR bit stays in the inactive state for at least two consecutive frames, the transmitter is requested to abort transmission (MX bit inactive) and to re-transmit the entire message.

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If an EOM is detected the receiver sets the MR-bit inactive, that is, no acknowledgment is issued and the MR bit is kept in this state until a new transfer procedure is started. The bit has to be set inactive at the latest one frame after the MX bit has been inactive two times. Furthermore, the receiver checks after the receipt of EOM to see whether 2 bytes have been transferred. If this is not the case the whole message is disregarded by the receiver.

To allow the start of a new cycle of MON messages every 6 ms, and to prevent a hang-up situation under failure conditions, the transmit procedure is reset to its idle state every 6 ms. If this happens when a transfer procedure is being performed, the transmitter of the IEC-Q sets the MX bit inactive two times to assure that the receiver enters the idle state too. If a transmit procedure is reset the message is lost. To prevent this situation the transmitter does not start a transfer procedure during a period of time corresponding to 16 IOM frames before the superframe indication (IOM frames 81–96) or 6 ms after (IOM frames 33–48). In this case the receiver is requested to delay the receive procedure for not more than four IOM frames compared to the timing diagram in Figure 15.

The receive procedure is also reset to its idle state every 6 ms. If this happens when a receive procedure is being performed the message may be lost because the generation of an abort request can not be guaranteed. To prevent this situation the receiver does not start a receive procedure during a period of time corresponding to 16 IOM frames before the superframe indication or 6 ms after. In this case the transmitter is requested to delay the transmit procedure for not more than five IOM frames compared to the timing diagram in Figure 15.

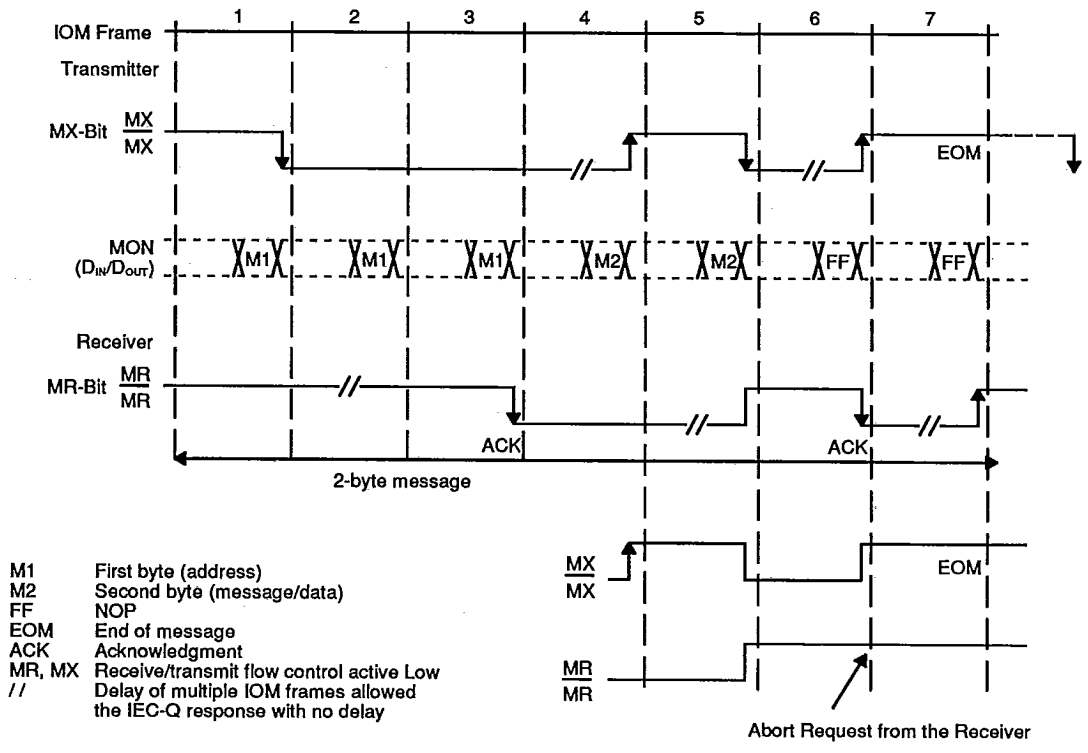

Figure 15. Transfer Procedure 11892B-17

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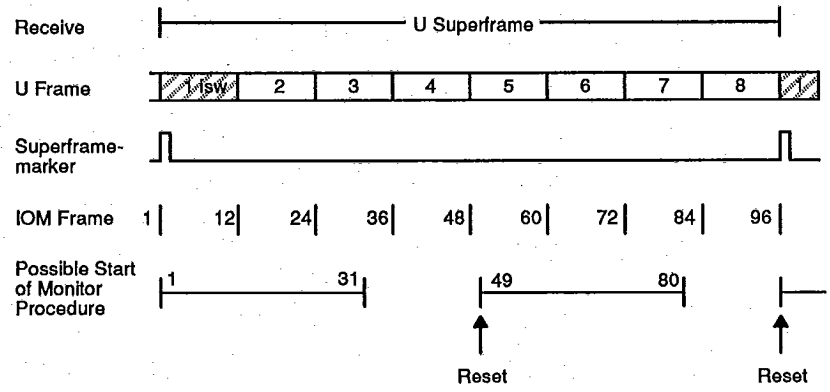

Figure 16. Monitor Access 11892B-18

Message Structure

Table 7. MON-0

Automode

0 0 0 0	a a a	1	e e e e e e e e
0	EOC addr.	d/m	EOC Code

EOC Code Hex	NT		LT	
	D	U	D	U
50	LBBD 1)		LBBD	
51	LB1 1)		LB1	
52	LB2 1)		LB2	
54	NCC 1)		NCC	
53	RCC 1)		RCC	
FF	RTN 1)		RTN	
00	H 1)		H	H
AA				UTC
zz				ACK

Notation:
zz code identical to corresponding command
U upstream (TE –> LT)
D downstream (LT –> TE)
d/m data/message indicator: 1: message
0: data

Notes: 1. These indications are issued for test purposes only. They are disregarded by the SBCX but acknowledged according to the procedure specified in the MON-1 Indications section.
2. The EOC address of the NT is 000. The NT also reacts to the broadcast address 111.

The MON-0 structure is used for EOC related messages. The EOC address, the data/message (d/m) indicator and the EOC code are as specified for the U interface.

Commands (messages on D_{IN}) are used in the LT mode only. They may be passed at any moment in time and need to be transferred only once according to the procedure specified in the MON-1 Indications section. Code repetition is performed within the chip by the EOC processor. These commands are latched. That is, they are valid as long as they are not disabled explicitly by a "return to normal" message. Only one pending command is allowed. That is, one command has to be acknowledged before a new one may be passed (valid for MON and for EOC channel).

Indications (messages on D_{OUT}) are used in the LT and NT mode. The validation (receipt of three identical consecutive messages) of received EOC messages is performed within the chip by the EOC processor. The EOC messages are issued across the MON channel every time a change has been detected in the EOC channel, but only when validated by the EOC processor (latched). In the NT mode these indications are issued for test purposes only.

Transparent Mode

The MON-0 structure is used to transfer the 24 bits defined for the EOC channel in the automode (M1, M2, M3). They are passed in the same order as on the U interface making use of two 2-byte messages per superframe. The 2-byte message marked by the superframe indication transfers the first 12 bits of a superframe. The second 2-byte message is transferred 6 ms later.

These bits are monitored continuously; that is, every 6 ms 12 bits are passed across the MON channel in both the transmit and the receive direction. The IEC-Q doesn't perform any processing of the bits and treats them in a completely transparent manner.

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Table 8. MON-1

Automode and transparent mode

0 0 0 1	x x x x	s s s s	m m m m
1		S/Q Code	M Bits

S/Q Code	NT		LT	
	D	U	D	U
0000				
0001		ST		
0010	STP			
0100	FEBE			
1000	NEBE			
1100	FNBE			
1111		NORM		

M bits				
1xx0		NTM		
1111		NORM		

Notation:
U upstream (TE –> LT)
D downstream (LT –> TE)
x don't care

Messages:
FEBE Far End Block Error
FNBE Far and Near End Block Error
NEBE Near End Block Error
NORM Return to Normal
NTM NT Test Mode
ST Self Test Request NT
STP Self Test Pass

MON-1 Indications

The MON-1 structure applies to the NT mode only and is used for indications corresponding to specific bits in the maintenance channel of the U interface and for S/Q channel related messages.

Indications related to the Q channel issued by the SBCX are transferred over the MON channel every time a change has been detected in the Q channel (latching). Block error indications (FEBE, NEBE and FNBE) are issued by the IEC-Q every time an error has occurred (non-latching); the response to a self test request (STP) is non-latching too.

All indications received by the IEC-Q during one superframe (12 ms) are passed over the MON channel in one block making use of one 2-byte message. Indications issued by the SBCX may be received with a different timing (for instance every 5 ms).

Table 9. MON-2

Automode and transparent mode

0 0 1 0	d d d d	d d d d d d d d
2	M Bits	M Bits

The MON-2 structure is used in both NT and the LT modes to transfer all the overhead bits except EOC and CRC. This corresponds to 12 bits passed in the same order as defined on the U interface and starting (first bit after the address bit) with the act bit:

U Super-Frame Position	NT –> LT		LT –> NT	
	position	control	position	control
M41	act	IEC-Q	act	IEC-Q
M51	1	MON-2	1	MON-2
M61	1	MON-2	1	MON-2
M42	ps1	pin	deact	IEC-Q
M52	1	MON-2	1	MON-2
M62	FEBE	IEC-Q	FEBE	IEC-Q
M43	ps2	pin	1	MON-2
M44	ntm	MON-1	1	MON-2
M45	cso	IEC-Q*	1	MON-2
M46	1	MON-2	1	MON-2
M47	1	MON-2	1	MON-2
M48	1	MON-2	1	MON-2

Note: *set to 0
Mxy: Mx in frame y

In the transmit direction (on D_{IN}) only the undefined bits marked with binary 1 may be controlled by making use of a MON-2 message. They are set to binary 1 after leaving a Power Down state. The transfer mode is latched; that is, the U bit transmits a given bit polarity as long as it is not changed by a new MON-2 message. No further processing is performed by the IEC-Q.The bits act, deact, FEBE and cso are always controlled by the IEC-Q itself. The ntm bit is controlled by the S chip making use of a MON-1 message. The bits ps1 and ps2 are defined by pins.

In the receive direction (on D_{OUT}) a MON-2 message defining all 12 bits is issued every time a change on at least 1 bit has been detected but not more often than once per superframe (12 ms interval). This is valid for all bits except the FEBE bit. In the LT mode, single block errors are not indicated autonomously, but may be read by making use of a local command (RBEN, RBEF). In the NT mode, single block errors are indicated by making use of a MON-1 message.

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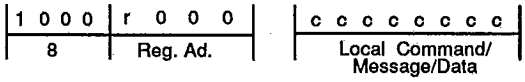
Table 10. MON-8

Automode and transparent mode



		NT		LT	
r	Code C	D	U	D	U
0	1111 0000		CCRC[1]	CCRC	
0	1111 0100		LB1[1]		
0	1111 0010		LB2[1]		
0	1111 0001		LBBD[1,3]		
0	1111 1111		NORM[1]	NORM	
0	1111 1011		RBEN	RBEN	
0	1111 1010		RBEF	RBEF	
0	1111 1000			RPFC	
0	011d ddaa		WCI[2]	WCI[2]	
0	010* **aa		RCI[2]	RCI[2]	
0	ddd* ****	ACI[2]			ACI[2]
0	00000000		RID	RID	

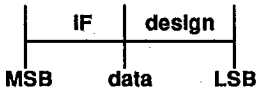
Notation:
U upstream (TE –> LT)
D downstream (LT –> TE)
1 binary 1
0 binary 0
a . . . a address controller interface to pin PCA
d . . . d data controller interface to pin PCD

Notes: 1. These codes are only used in the transparent mode.
2. See controller interface description.
3. TE mode only.

Commands:
CCRC Corrupt crc
LB1 Loopback Channel B1 request (within NT/IEC-Q)
LB2 Loopback Channel B2 request (within NT/IEC-Q)
LBBD Loopback B1, B2, and D channel request (within NT/IEC-Q)
NORM Return To Normal
RBEF Read Block Error Counter Far End
RBEN Read Block Error Counter Near End
WCI Write Controller Interface
RCI Read Controller Interface
ACI Answer Controller Interface
RID Read Identification
RPFC Read Power Feed Current Value

The MON-8 structure is used for local functions. Commands (on D_{IN}) concerning loopback and CRC may be passed at any time and need to be transferred only once. They are latched; that is, they are valid as long as they are not disabled explicitly by a NORM message, except the commands requesting the transfer of internal data which are non-latching.

In the case of the identification code, all data are set to 0:



IF = 00 (U Interface)
design = 000000 (Reserved)

Test Loops

For the test of the line cards, several test loops are provided which can be controlled from the exchange. In the complete loop all channels (2B+D) shall be transmitted back towards the transmitting station without modification. The data from the other end of the line is ignored. There are separate loops for single channels called individual B-channel loopbacks. The individual B-channel loopback can provide per channel maintenance capabilities without totally disrupting service to the customer. All loops are transparent loops; that means all bits toward the loop are passed onward as well as looped back. Nevertheless, the NT receives this signal and remains synchronized.

Switching an Analog Loop in the IEC-Q

The analog loop is closed in the IEC-Q as near to the U interface as possible. Using internal switches, the signal from the line driver is fed back directly to the input. It is a short-circuit between the pins A_{OUT} and A_{IN} as well as between B_{OUT} and B_{IN}. The input signal from the hybrid is ignored in this mode.

The analog loop mode is controlled via the IOM-2 C/I channel.

In an analog loop the transmit path is set to the LT mode and the receive path is set to the NT mode independently of the polarity of the LT pin.

Switching the Complete Loop and the Individual B-Channel Loopback

The individual B-channel loopbacks are always closed in the IEC-Q. The complete loop can be closed in the IEC-Q NT-PABX and NT-TE modes. With internal switches the corresponding user data at D_{OUT} (2B+D or B1 or B2) are directly fed back into D_{IN}. The control input (Monitor- and C/I-channel as well as MX- and MR-bit) is still read from the IOM-2 interface. Although these loops are closed by command from the exchange, the IEC-Q can still be deactivated by RES and SSP C/I- channel commands from the Layer 2 device.

In the NT the activation of an analog loop leads to the deactivation of all services initiated by the exchange. While the analog loop is activated the NT is not available for services, that is, a complete or an individual B-channel loopback can't be closed and a required CCRC shall not be carried out.

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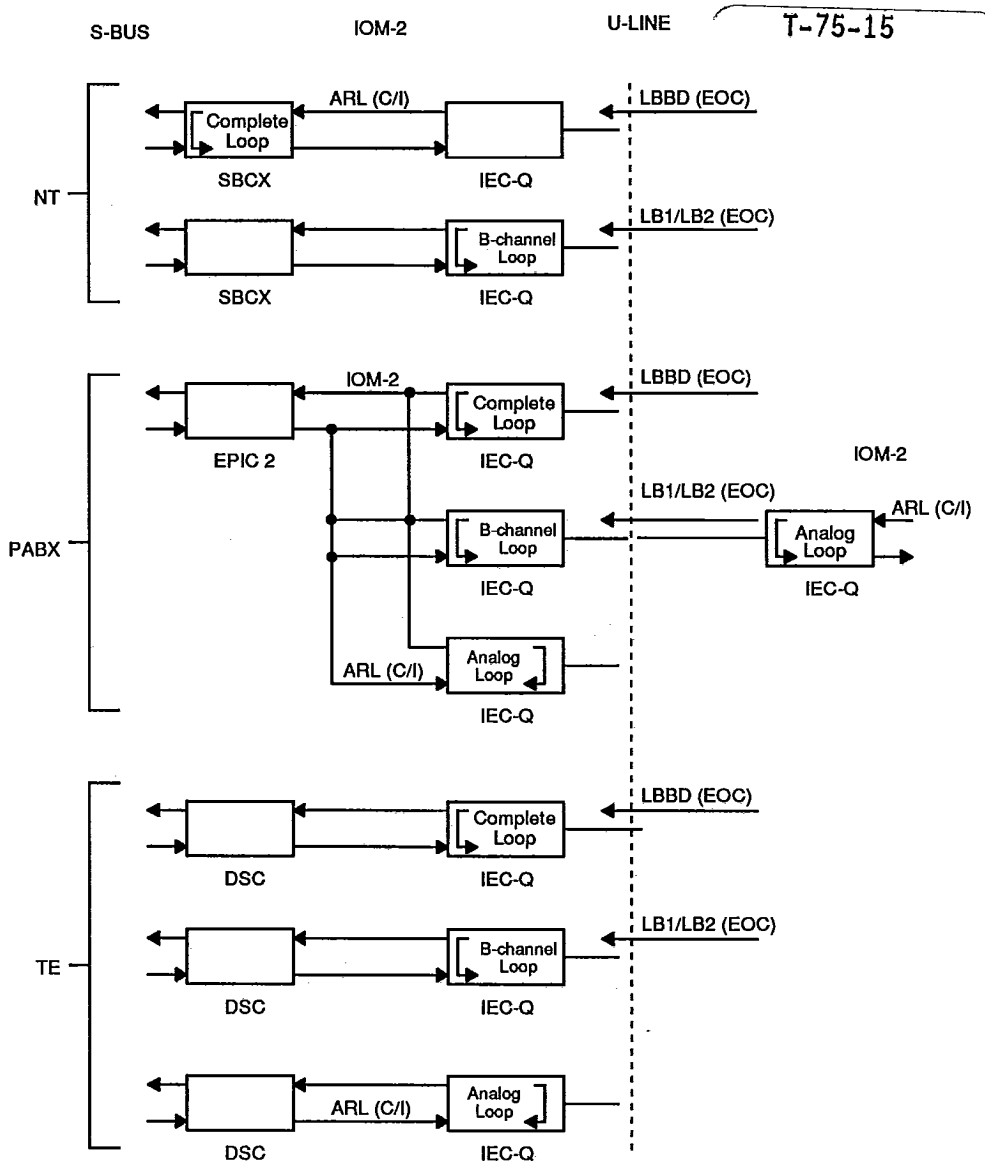

Figure 17. Test Loops Closed by the IEC-Q or Under its Remote Control

Note: For transparent mode operation the EOC loop request is performed over the IOM-2 interface NT upstream by a MON-8 message.

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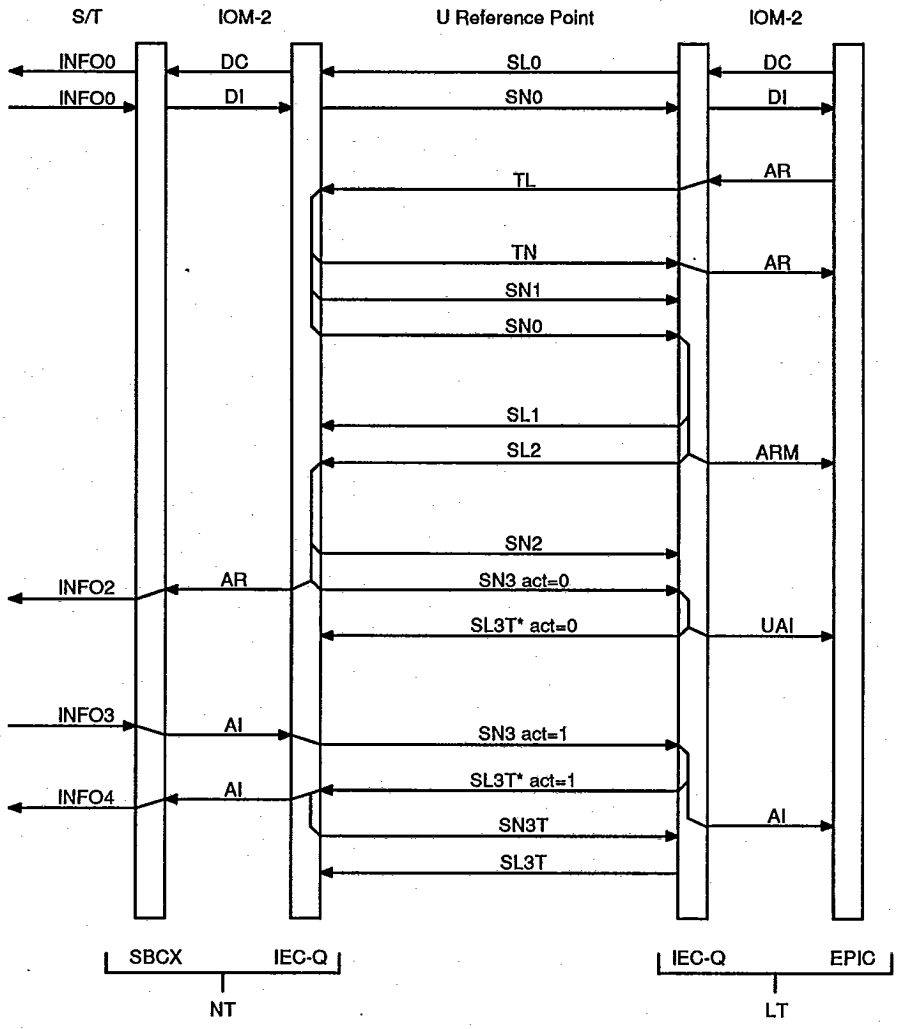
ACTIVATION AND DEACTIVATION PROCEDURES

Activation can be initiated by either the LT or the NT side. Deactivation is always initiated from the LT side.



Note: SL3 is generated by exchange at this time.

11892B-20

Figure 18. Activation From LT

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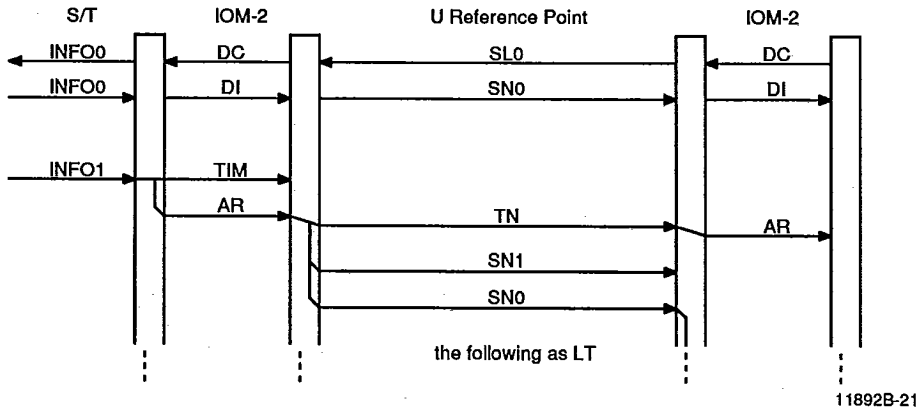

Figure 19. Activation from NT

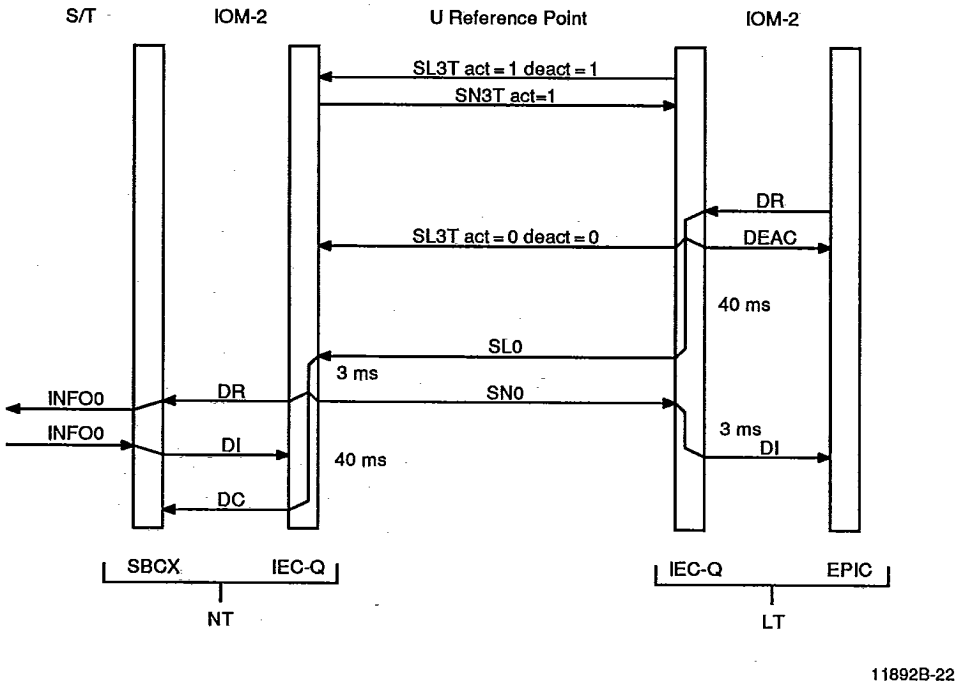

Figure 20. Deactivation Procedure

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Table 11

Signal	Synch Word (SW)	Superframe (ISW)	2B+D	M
TN	±3	±3	±3	±3
SN0	no signal	no signal	no signal	no signal
SN1	present	absent	1	1
SN2	present	absent	1	1
SN3	present	present	1	normal
SN3T	present	present	normal	normal
TL	±3	±3	±3	±3
SL0	no signal	no signal	no signal	no signal
SL1	present	absent	1	1
SL2	present	present	0	normal
SL3*)	present	present	0	normal
SL3T	present	present	normal	normal

*) SL3 is generated by exchange.

TL/TN alternate ±3 for 10 kHz tone.
SNx signal from NT to LT.
SLx signal from LT to NT.

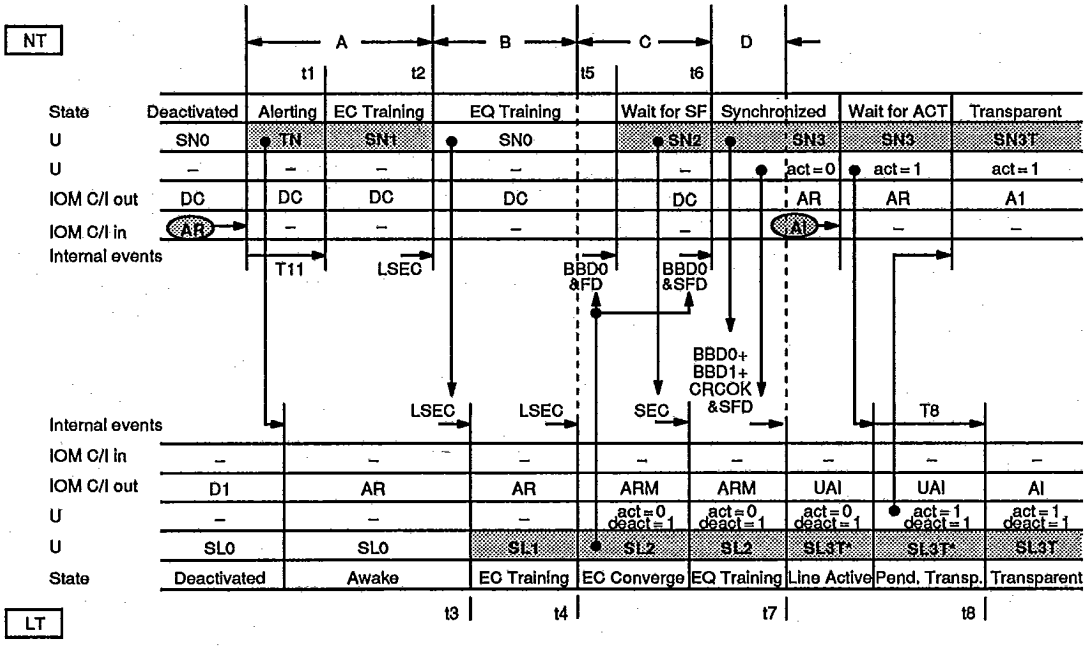

Figure 21. Activation from NT

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* SL3 is generated by exchange at this time.

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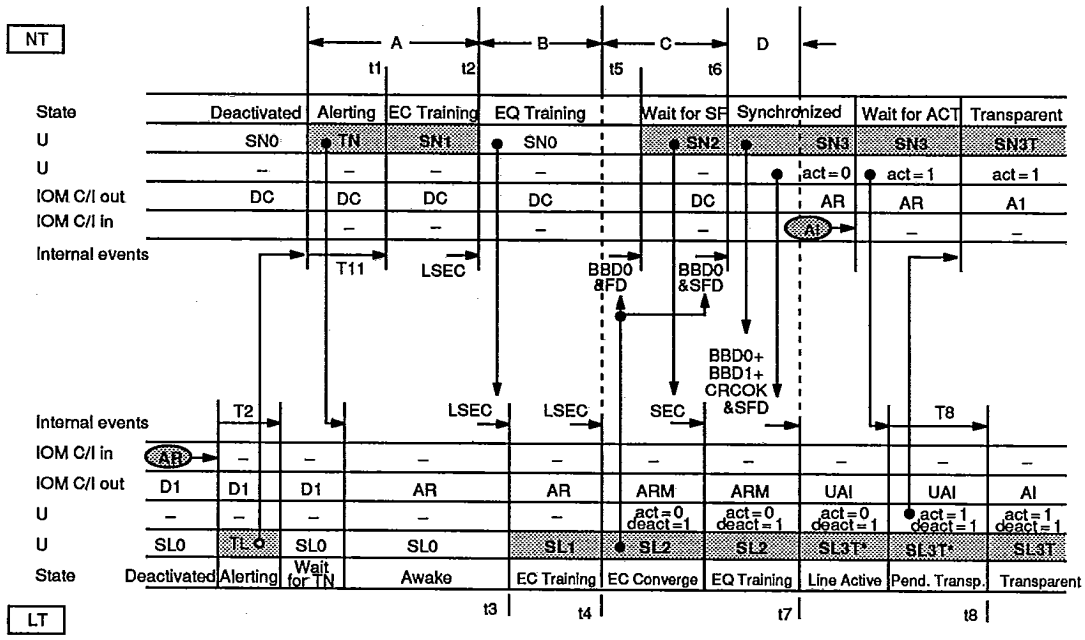

Figure 22. Activation from LT

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t2 – t3 ≤ 480 ms
A + c ≤ 5 s cold start
A + C ≤ 150 ms warm start
B + D ≤ 10 s cold start
B + D ≤ 150 ms warm start

* SL3 is generated by exchange at this time.

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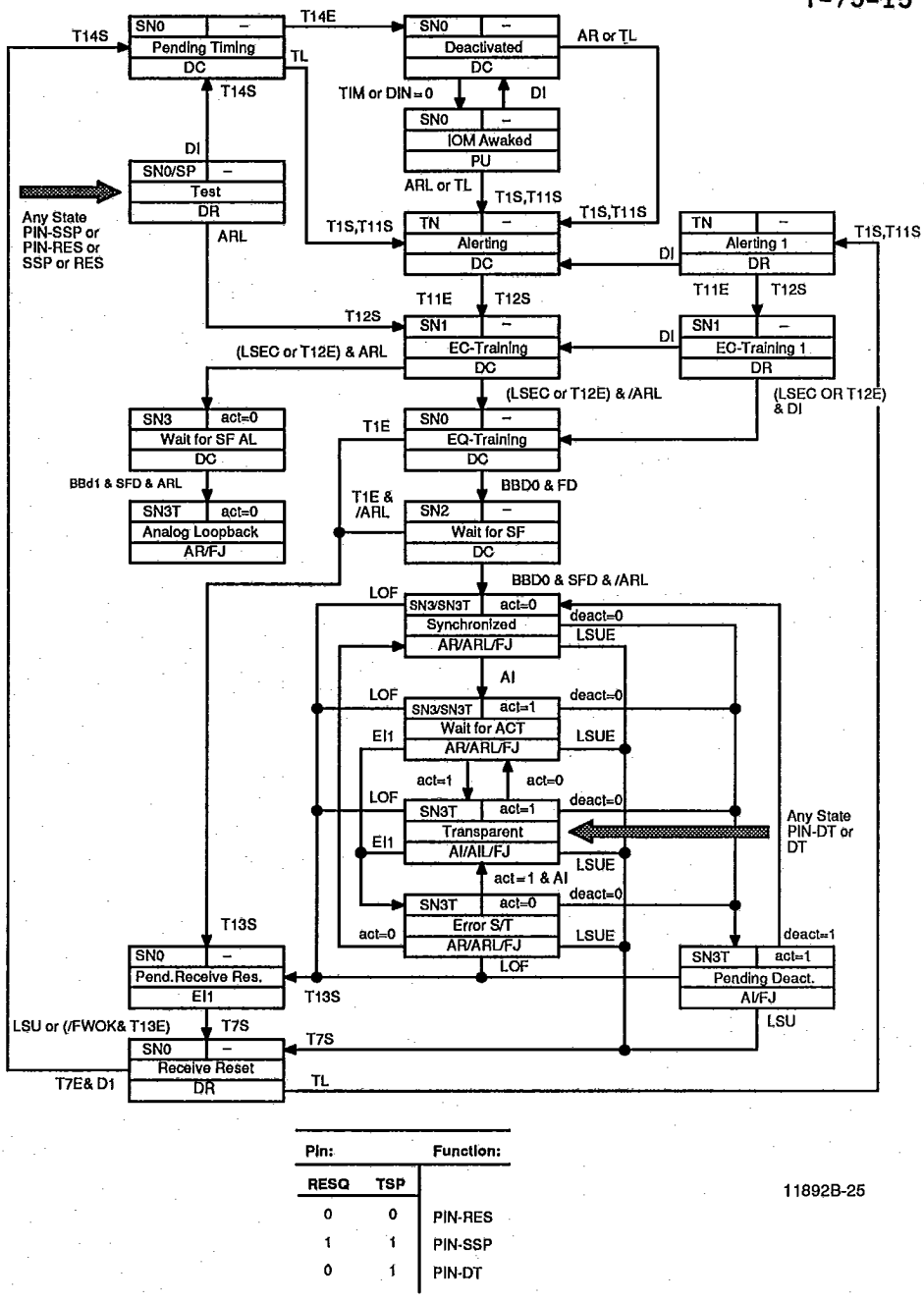

Figure 23. State Transition Diagram NT, NT-PABX Modes

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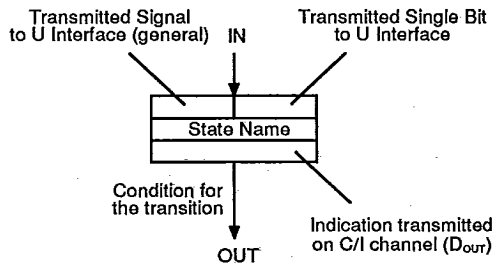
Explanation for NT State Diagram



The following commands or events are used for the transition:

C/I Channel (on DIN)

AI—Activation Indication
The SBCX issues this indication to announce that the receiver is synchronized. The IEC-Q informs the network side by setting the act bit to 1.

AR—Activation Request
INFO1 has been received by the SBCX (NT mode only, not relevant in NT-PABX mode) and the IEC-Q is requested to start the activation process by sending the wake-up signal TN.

ARL—Activation Request Local Loopback
The IEC-Q is requested to operate an analog loopback (close to the U interface) and to begin the start-up sequence by sending SN1 (without starting timer T1). This command may be issued only after the IEC-Q has been reset by making use of the C/I channel code RES or the pin reset RESQ. This assures that the EC and EQ coefficient-updating algorithms converge correctly. The ARL command has to be issued continuously as long as the loopback is required.

DI—Deactivation Indication
This indication is used during a deactivation procedure to inform the IEC-Q that timing signals are not needed any more and that the IEC-Q may enter the deactivated (power-down) state. The DI indication has to be issued by the SBCX continuously until the IEC-Q has answered with the DC code.

DIN=0—Binary 0 polarity on DIN
In the NT mode this asynchronous signal requests the IEC-Q when staying in the deactivated state to enter the power-up state and to provide timing signals on the IOM interface. Hereafter, binary 0s in the C/I channel (code TIM 0000 or any other code different from DI 1111) maintain the IOM interface activated.

DT—Data Through
This unconditional command is used for test purposes only and forces the IEC-Q into a state equivalent to the transparent state. The far-end transceiver is assumed to be in the same condition.

T-75-15

EI1—Error Indication 1
The SBCX indicates an error condition on its receive side (loss of frame alignment or loss of incoming signal). The IEC-Q informs the network side by setting the act bit to 0 thus indicating that transparency has been lost.

RES—Reset
Unconditional command which resets the whole chip; especially the EC and EQ coefficients are set to 0. For cold start the reset code should be applied for a period of time of at least 8 IOM frames (1 ms).

SSP—Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U interface.

TIM—Timing
In the NT mode the IEC-Q is requested to continue providing timing signals and not to leave the power up-state. In the NT-PABX mode the IEC-Q is requested to enter the power-up state or not to leave it.

Pins

Pin-Res—Pin-Reset
Corresponds to pin RESQ. The functionality of this pin is the same as for the C/I code RES.

Pin-SSP—Pin-Send Single Pulses
Corresponds to pin TSP. The functionality of this pin is the same as for the C/I code SSP.

Pin-DT—Pin-Data Through
This function is activated when both pins RESQ and TSP are active (RESQ=0 and TSP=1). The functionality is the same as for the C/I code DT.

Events related to the U Interface

act=0/1—act Bit Received from Network Side
act=1 requests the IEC-Q to achieve transparency of the transmission in both directions. As transparency in receive direction (U interface to IOM) is already performed when the receiver is synchronized, the receipt of act=1 establishes transparency in transmit direction (IOM to U interface) too. In the case of loopbacks however, transparency in both directions of transmission is performed when the receiver is synchronized.

act = 0 indicates that the network side has lost transparency.

deact=0/1—dea Bit Received from the Network Side
deact=0 informs the IEC-Q that a deactivation procedure has been started by the network side.

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deact=1 reflects the case when deact=0 was detected by mistake for example, due to transmission errors, and allows the IEC-Q to recover from this situation.

LOF—Loss of Framing on the U Interface

LSEC—Loss of Signal Level behind the Echo Canceller
Internal signal which indicates that the Echo Canceller has converged.

LSU—Loss of Signal level on the U Interface
This signal indicates that a loss of signal level of a duration of 3 ms has been detected on the U interface. This short response time is relevant in all cases where the NT waits for a response (no signal level) from the network side, that is, after a deactivation has been announced (receipt of deact=0), after the NT has lost framing, and after timer T1 has elapsed.

LSUE—Loss of Signal level on the U Interface (Error condition)
This signal indicates that a loss of signal level of a duration of 588 ms has been detected on the U interface. This long response time (see also LSU) is valid in all cases where the NT is not prepared to lose signal level; that is, the LT has stopped transmission because of loss of framing, an unsuccessful activation, or interruption of the transmission line.

SFD—Superframe Detected

FD—Frame Detected

TL—Tone (wake-up signal) received from the LT
The IEC-Q is requested to start the activation process.

BBD0/1—Binary 0s or 1s Detected in the B and D Channels
This internal signal indicates that for a period of time of 6–12 ms, a continuous stream of binary 0s or 1s (analog loopback) has been detected. It is used as a criterion for receiver synchronization (SL2 from the network side or SN3 in the case of an analog loopback detected correctly).

Timers

The start of timers is indicated by TxS, the expiration by TxE. The following timers are used:

	(ms)		(state)
T1	15000	activation control	
T11	9	TN transmit	alerting
T12	5500	supervisor EC converge	EC training
T13	15000	frame synchronization	pending receive reset
T7	40	hold time	receive reset
T14	0.5	hold time	pending timing

The following indications or signals are transmitted:

C/I Channel (on DOUT) T-75-15

AI—Activation Indication
The IEC-Q has established transparency of transmission in the direction IOM to U interface. In the NT mode, the SBCX is requested to send INFO4 and to achieve transparency of transmission in the direction IOM to S/T interface. In the NT-PABX mode, the AI code signals that the IEC-Q is "ready for sending."

AIL—Activation Indication Loopback
The IEC-Q has detected act=1 while loopback 2 is still established. In the NT mode, the SBCX is requested to send INFO4 (if a transparent loopback 2 is to be implemented) and to keep loopback 2 established. In the NT-PABX mode, the AIL code indicates that act=1 has been detected and that loopback 2 is still established within the IEC-Q.

AR—Activation Request
The U receiver has synchronized on the incoming signal. In the NT mode, the SBCX is requested to start the activation procedure on the S/T interface by sending INFO2. In the NT-PABX mode, the AR code on DOUT has to be answered by the AI code on DIN.

ARL—Activation Request Loopback
The IEC-Q has detected a loopback 2 command in the EOC channel and has established transparency of transmission in the direction IOM to U interface. In the NT mode, the SBCX is requested to send INFO2 (if a transparent loopback 2 is to be implemented) and to operate loopback 2. In the NT-PABX mode, the ARL code indicates that loopback 2 is in operation within the IEC-Q.

DC—Deactivation Confirmation
Idle code on the IOM interface. Normally the IEC-Q stays in the power-down mode, but an activation procedure may have been started from the network side as well.

DR—Deactivation Request
The IEC-Q has detected a deactivation request command from the network side or stays in a test mode. In the NT mode, the SBCX is requested to start the deactivation procedure on the S/T interface by sending INFO0. In the NT-PABX mode, the DR code on DOUT has to be answered by the DI code on DIN.

EI1—Error Indication 1
The IEC-Q has entered a failure condition (loss of framing on the U interface or expiration of timer T1).

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FJ—Frame Jump
This indication is relevant only in the NT-PABX mode and signals that either a data buffer overflow/underflow has been detected or a phase jump of one of the IOM timing signals DCL or FSC has occurred. The FJ code is issued for a period of 1.5 ms.

Signals Transmitted on the U Interface

The signals SNx, TN and SP transmitted on the U interface are defined in this section. The following states are used:

Alerting
The wake-up signal TN is transmitted for a period of T11 either in response to a received wake-up signal TL or to start an activation procedure on the network side.

Alerting IOM Awaked
This state is entered when a wake-up tone was received in the receive reset state and the deactivation procedure on the user side was not yet finished. The transmission of wake-up tone TN is started.

Analog Loopback
Upon detection of binary 1s for a period of 6–12 ms and of the superframe indication the analog loopback state is entered and transparency is achieved in both directions of transmission. This state can be left making use of any unconditional command. However, only the C/I channel code RES or pin RESQ should be used. This assures that the EC and EQ coefficients are set to zero and that for a subsequent normal activation procedure the receiver updating algorithms converge correctly.

Deactivated (full reset)
This state corresponds to the power-down or low-power consumption mode; that is, no timing signals are delivered on the IOM interface and no signal is sent on the U interface. The IEC-Q waits for a wake-up signal TL from the network side or a wake-up signal (D_{IN}=0) from the user side to start an activation procedure. In the NT-PABX mode (where timing signals are delivered from the PABX side) the C/I channel codes AR and TIM are valid too.

EC Training
The signal SN1 is transmitted on the U interface to allow the NT receiver to update the EC coefficients. The automatic gain control (AGC), the timing recovery and the EQ updating algorithm are disabled. The EC training state is left when the EC has converged (LSEC) or when timer T12 has elapsed.

EC Training IOM Awaked
This state is entered if the transmission of signal SN1 has to be started and the deactivation procedure on the user side is not yet finished.

EQ Training
The receiver waits for signal SL1 or SL2 to be able to update the AGC, to recover the timing phase, to detect the synch word (SWD) and to update the EQ coefficients. The EQ training state is left upon detection of binary 0s in the B and D channels for a period of 6–12 ms corresponding to the detection of SL2.

Error S/T
Loss of framing or loss of incoming signal has been detected on the S/T interface (EI1). The network side is informed by setting the act bit to 0 (loss of transparency on the user side). The following codes are issued on the C/I channel:

–normal activation or single channel loopback: AR

–loopback 2: ARL

IOM Awaked
Timing signals are delivered on the IOM interface. The IEC-Q enters the deactivated state again upon detection of the C/I channel code DI (idle code).

Pending Deactivation
The IEC-Q waits for the receive signal level to be turned off (LSU) to enter the receiver reset state and start the deactivation procedure.

Pending Receive Reset
This state is entered upon detection of loss of framing on the U interface or expiration of timer T1. This failure condition is signaled to the network side by turning off the transmit level (SN0). The IEC-Q then waits for a response (no signal level LSU) from the network side to enter the receive reset state.

Pending Timing
In the NT mode this state assures that the C/I channel code DC is issued four times before the timing signals on the IOM interface are turned off.

Receive Reset
This state is entered upon detection of a deactivation request from the network side, after a failure condition on the U interface (loss of signal level LSUE) or through the pending reset state upon expiration of timer T1 or loss of framing.

No signal is transmitted on the U interface, especially no wake-up signal TN, and the SBCX is requested to start the deactivation procedure on the user side (DR). Timer T7 assures that no activation procedure is started from the user side for a minimum period of time of T7.

The state is left only after completion of the deactivation procedure on the user side (receipt of the C/I channel code DI), unless a wake-up tone is received from the network side.

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Synchronized
When the IEC-Q has reached this state, it informs the network side by sending the superframe indication (inverted synchword) and the user side by issuing the C/I channel codes AR or ARL. The loopback commands decoded by the EOC processor control the output of indications and transmit signals:

–normal activation: SN3 and AR

–single channel loopback: SN3T and AR

–loopback 2: SN3T and ARL

The IEC-Q waits for the receipt of the C/I channel code AI to enter the wait for act state.

Test
This test mode is entered when the unconditional commands RES, SSP, Pin-RES or Pin-SSP are used. It is left when both pins RESQ and TSP are inactive and the C/I channel codes DI or ARL are received.

The following signals are transmitted on the U interface:

–no signal level (SN0) when the C/I channel code RES is applied or pin RESQ is activated.

–single pulses (SP) when the C/I channel code SSP is applied or pin TSP is activated.

Transparent
This state is entered upon the detection of act=1 received from the network side and corresponds to the fully active state. In the case of a normal activation in both directions of transmission.

The user side is informed by the following codes:

–normal activation or single channel loopback: AI

–loopback 2: AII

Wait for Act
Upon the receipt of AI, the act bit is set to 1 and the NT waits for a response (act=1) from the network side. The output of indications and transmit signals is as defined for the synchronized state.

Wait for Superframe
Upon detection of SL2, the signal SN2 is sent on the U interface and the receiver waits for detection of the superframe indication. Timer T1 is then stopped and the synchronized state is entered.

Wait for Superframe Analog Loopback
This state is entered in the case of an analog loopback and allows the receiver to update the AGC, to recover the timing phase and to update the EQ coefficients. Signal SN3 is sent instead of signal SN2 in the wait for SF state.

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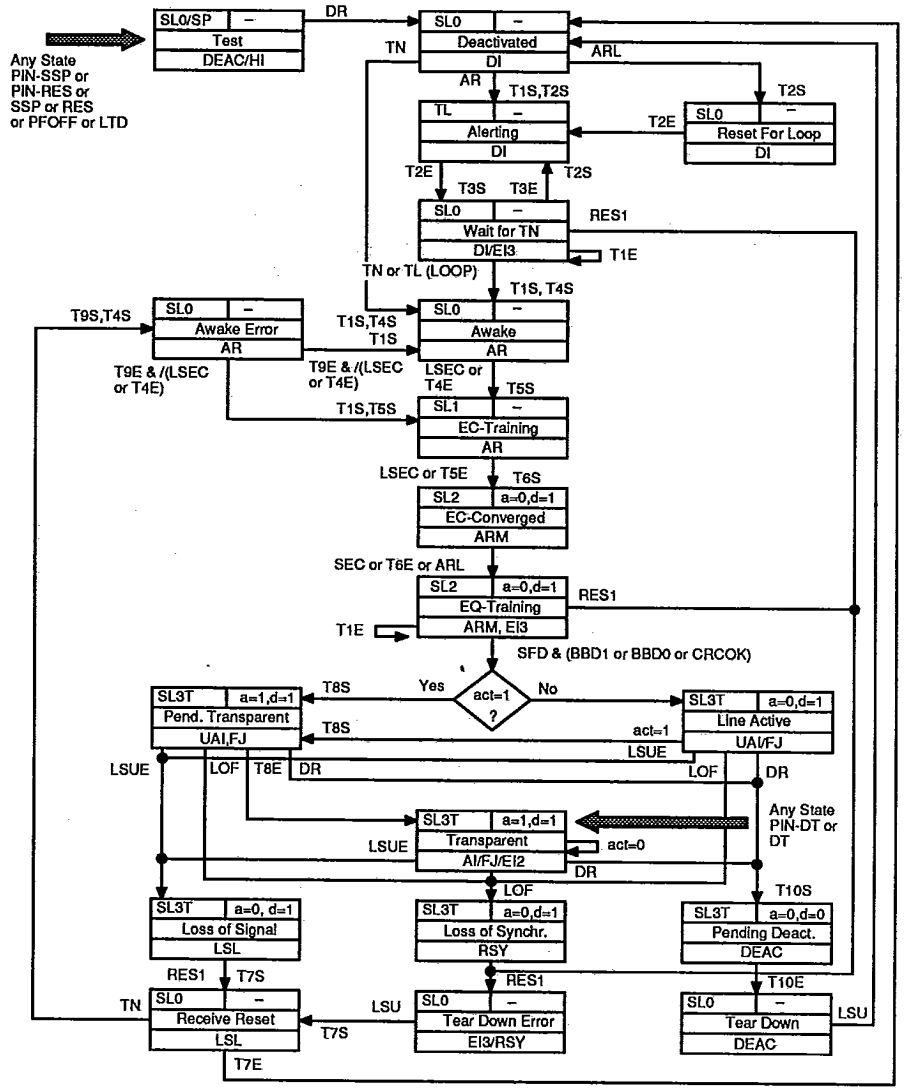

Pin:		Function:
RESQ	TSP	
0	0	PIN-RES
1	1	PIN-SSP
0	1	PIN-DT
PS1		PFOFF
1		

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Figure 24. State Transition Diagram LT Mode

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Explanation for LT State Diagram

The following commands or events are used for the transition:

C/I Channel (on DIN)

AR—Activation Request
The IEC-Q is requested to enter the power-up state and to start an activation procedure by sending the wake-up signal TL.

ARL—Activation Request Local Loopback
The IEC-Q is requested to operate an analog loopback (close to the U interface) and to start the start-up sequence by sending the wake-up tone TL. This command may be issued only after the IEC-Q has been set to the deactivated state (C/I channel code DI issued on DOUT) and has to be issued continuously as long as loopback is requested.

DR—Deactivation Request
This command requests the IEC-Q to start a deactivation procedure by setting the deact bit to 0 and to cease transmission afterwards. The DR code is not an unconditional command and the IEC-Q reacts on it only in the states line active, pending transparent and transparent, that is, when the C/I channel codes UAI, AI, FJ or EI2 are issued on DOUT.

DT—Data Through
This unconditional command is used for test purposes only and forces the IEC-Q into the transparent state. The far-end transceiver is assumed to be in the same condition.

LTD—LT Disable
This is an unconditional command which requests the IEC-Q to switch off the remote-power-feed circuit for the subscriber line by activating the pin DISS.

RES—Reset
Unconditional command which resets the whole chip; for cold start the reset code should be applied for a period of at least eight IOM frames (1 ms).

RES1—Reset 1
The Reset 1 command resets all receiver functions, especially the EC and EQ coefficients and the AGC are set to 0. The RES1 code should be used when the IEC-Q has entered a failure condition (expiry of timer T1, loss of framing or loss of signal level) indicated by the C/I channel code EI1 on DOUT. This command starts a deactivation procedure on the U interface, besides resetting the receiver.

SSP—Send Single Pulses
Unconditional command which requests the transmission of single pulses on the U interface.

Pins

Pin-RES—Pin-Reset
Corresponds to pin RESQ. The functionality of this pin is the same as for the C/I code RES.

Pin-SSP—Pin-Send Single Pulses
Corresponds to pin TSP. The functionality of this pin is the same as for the C/I code SSP.

Pin-DT—Pin-Data Through
RESQ and TSP are active (RESQ=0 and TSP=1). The functionality is the same as for the C/I code DT.

PFOFF—Power Feed Off
Corresponds to pin PS1. This pin indicates that the remote-power-feed circuit for the subscriber line has been turned off. The IEC-Q is requested to forward this indication making use of the C/I channel code HI.

Events Related to the U Interface

act=0/1—act bit received from the user side
act=1 signals that the NT has detected INFO3 on the S/T interface and indicates that the whole basic access is synchronized in both directions of transmission. The network side is requested to provide transparency of transmission in both directions and to respond with setting the act bit to1. In the case of loopbacks (loopback 2 or single channel loopback in the NT), however, transparency is required even when the NT is not sending act=1.

Transparency is achieved in the following manner:

The IEC-Q performs transparency in both directions of transmission after the receiver has achieved synchronization (state EQ training is left) independently of the status of the received act bit.

The status "ready for sending" is reached when the state transparent is entered, that is, when the C/I channel indication AI is issued. This is valid in the case of a normal activation procedure for call control. In the case of loopbacks (loopback 2 or single channel loopback in the NT and analog loopback in the LT), however, the status "ready for sending" is reached when the state line active is entered; that is, when the C/I channel indication UAI is issued. Until the status "ready for sending" is reached, binary 0s have to be passed in the B and D channels on DIN.

act=0 indicates the loss of transparency on the user side (loss of framing or loss of signal level on the S/T interface). The IEC-Q informs the network side by issuing the C/I channel indication EI2, but performs no state change or other actions.

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CRCOK—Cyclic Redundancy Check OK
This input is used as a criterion that the receiver has acquired frame synchronization and converged both its EC and EQ coefficients.

LOF—Loss of Framing on the U Interface

LSEC—Loss of Signal Level behind the Echo Canceller
In the awake state, this input is used as indication that the NT has ceased the transmission of signal SN1. In the EC training state, this input is used as an internal signal indicating that the EC in the LT has converged.

LSU—Loss of Signal Level on the U Interface
This signal indicates that a loss of signal level of a duration of 3 ms has been detected on the U interface. This short response time is relevant in all cases where the LT waits for a response (no signal level) from the user side, that is, after a deactivation procedure has been started or after loss of framing in the LT.

LSUE—Loss of Signal Level on the U Interface (error condition)
This signal indicates that a loss of signal level of a duration of 492 ms has been detected on the U interface. This long response time (see also LSU) is valid in all cases where the LT is not prepared to lose signal level; that is, the NT has stopped transmission because of losing framing or because of an unsuccessful activation or the transmission line is interrupted.

SEC—Signal Level behind the Echo Canceller
This signal indicates that a signal level corresponding to SN2 from the NT has been detected on the U interface.

SFD—Superframe Detected

TN—Tone (wake-up signal) received from the NT
When staying in the deactivated state, the IEC-Q is requested to start an activation procedure and to inform the network side making use of the C/I channel code AR. When staying in the wait for awake acknowledge state, the signal TN sent by the NT acknowledges the receipt of a wake-up signal TL from the LT. When an analog loopback is operated, the wake-up signal TL sent by the LT transmitter is detected by the LT receiver.

BBD0/1—Binary 0s or 1s Detected in the B and D Channels
This internal signal indicates that for a period of time of 6–12 ms a continuous stream of binary 0s or 1s has been detected. It is used as a criterion that the receiver has acquired frame synchronization and converged both its EC and EQ coefficients. BBD1 corresponds to the signals SN2 or SN3 in the case of a normal activation and BBD0 corresponds to the internally received signal SL2 in the case of an analog loopback or possibly a loopback 2 in the NT.

Timers

	(ms)		(state)
T1	15000	supervisor for start-up	
T2	3	TL transmission	alerting
		receiver reset	reset for loop
T3	40	re-transmission of TL	wait for TN
T4	6000	supervisor SN0 detect	awake
T5	300	supervisor EC converge	EC training
T6	6000	supervisor SN2 detect	EC converge
T8	24	delay time for AI indication	pend transparent
T7	40	hold time	receive reset
T9	40	hold time	awake error
T20	40	DEAC transmission	pend deactivation

The following indications or signals are transmitted:

C/I Channel (on DOUT)

AI—Activation Indication
This indication signals that act=1 has been received and that timer T8 has elapsed. This indication is not issued in the case of an analog loopback; it may be issued in the case of loopback 2 or a single channel loopback in the NT.

AR—Activation Request
The AR code signals that a wake-up signal has been received and that a start-up procedure is being performed; receiver synchronization is not yet achieved.

DEAC—Deactivation
This indication is issued in response to a DR code or in the test state.

DI—Deactivation Indication
Idle code on the IOM interface. Normally the IEC-Q stays in the deactivated state, unless an activation procedure was started by the network side.

EI2—Error Indication 2
The NT receiver on the S/T interface has detected a loss of signal level or has lost framing (receipt of act=0).

EI3—Error Indication 3
This indication is issued when the IEC-Q has entered the failure condition; unsuccessful activation (expiration of timer T1).

LSL—Loss of Signal Level
The IEC-Q has entered a failure condition after loss of signal level (LSUE).

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RDY—Resynchronization indication after a loss of framing (LOF)
For EI3, LSL, and RDY indication the network side should react by applying the C/I channel code RES1, to allow the IEC-Q to enter the receive reset state and to reset the receiver functions.

FJ—Frame Jump
This indication signals that either a data buffer overflow/underflow has been detected or a phase jump of one of the IOM timing signals DCL or FSC has occurred. The FJ code is issued for a period of 1.5 ms.

HI—High Impedance
PFOFF is activated which means that the remote-power-feed circuit for the subscriber line is turned off.

UAI—U Activation Indication
The UAI code signals that the line system is synchronized in both directions of transmission (see also the input act=1).

ARM—Activation Request Maintenance
Transmission of maintenance bits is possible.

Signals transmitted on the U Interface

The signals SLx, TL and SP transmitted on the U interface are defined in this section. The polarity of the overhead bits act and deact is indicated as follows:

a=0/1 corresponds to act bit set to binary 0/1.

d=0/1 corresponds to deact bit set to binary 0/1.

The following states are used:

Alerting
The wake-up signal TL is transmitted for a period of time of T2 in response to an activation request from the network side (AR or ARL). In the case of an analog loopback the signal TL is forwarded internally to the wake-up signal detector and stored.

Awake
This state is entered upon the receipt of a wake-up or an acknowledge signal TN from the NT. In the case of an activation started by the network side, timer T1 is restarted when the awake state is entered.

Awake Error
This state is equivalent to the awake state, but is entered only when a wake-up signal is received while in the receive reset state. As the receive reset state was entered upon the application of the C/I channel code RES1, the awake error state assures that a minimum amount of time elapses between the application of the RES1 code and the entrance into a state (EQ training) in which the IEC-Q again reacts on the RES1 code.

The network side is requested to stop issuing the command RES1 within T9 after the receipt of the C/I channel code AR on DOUT and to replace it by another command such as the idle code DC.

Deactivated (full reset)
This state corresponds to the power-down or low power consumption mode (the receiver and parts of the interface are forced into a power-down mode; functions related to the IOM interface and the wake-up signal detector are still active); no signal is sent on the U interface. The IEC-Q waits for a wake-up signal TN from the user side or an activation request (AR or ARL) from the network side to start an activation procedure.

EC Converged
Upon converge of the EC coefficients, the IEC-Q starts the transmission of signal SL2 and waits for the receipt of signal SN2 from the NT (SEC). If no signal is detected within T6 however, the start-up procedure is continued. In the case of an analog loopback, this state is left immediately because the EC compensates for the looped back transmit signal and no signal level is encountered behind the EC.

EC Training
The signal SL1 is transmitted on the U interface to allow the LT receiver to update its EC coefficients. The EC training state is left when the EC has converged (LSEC) or when timer T5 has elapsed. Timer T5 allows the start-up procedure to proceed even if LSEC (e.g., because of a high noise level on the U interface) could not be detected.

EQ Training
The EQ training is left after the receiver synchronization has been achieved and the superframe indication detected (SFD). Upon expiration of timer T1 the C/I channel indication EI3 is issued.

Line Active
In this state the IEC-Q performs transparency of the transmission in both directions. The line system is synchronized and the maintenance channel is operational. The IEC-Q stays in the line active state

–during a normal activation procedure for call control or when a single channel loopback is performed in the NT and no INFO3 signal is received on the S/T interface; that is, all TE's are unplugged

or

–when an analog loopback is established

or

–possibly when a loopback 2 is established in the NT and the SBCX monitors INFO3 on the S/T interface and no INFO3 is received.

In the case of normal activation for call control, binary 0s have to be applied to the B and D channels on the IOM interface. After the C/I channel indication UAI has been issued, the Layer 2 receiver should be fully operational

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to prevent the first Layer 2 message issued by the user side, upon the receipt of the AI code in the TE, to be lost.

Loss of Signal
This state is entered upon the detection of a failure condition, that is, loss of receive signal (LSUE). The act bit is set to 0 and the C/I channel indication LSL is issued. The IEC-Q waits for the C/I channel command RES1 to enter the receive reset state.

Loss of Synchronization
This state is entered upon the detection of a failure condition, that is, loss of framing by the LT receiver (LOF). The act bit is set to 0 and the C/I channel indication RSY is issued. The IEC-Q waits for the C/I channel command RES1 to enter the tear down error state and subsequently the receive reset state.

Pending Deactivation
This is a transient state entered after the receipt of a DR code. The deact bit is set to 0. Timer T10 assures that the deact bit is set to 0 in at least three subsequent superframes before the transmit level is turned off.

Pending Transparent
This is a transient state entered upon the detection of act=1 and left by T8. The act bit is set to 1. The purpose of this state is to issue the C/I channel indication AI (corresponding to "ready for sending") T8 only after the act bit has been set to 1 by the LT transceiver. This assures that under normal operating conditions the AI indication is issued first on the TE side and only afterwards on the network side and that normally the Layer 2 receiver in the TE is already operational when the first Layer 2 message is issued by the network side.

Receive Reset
The receive reset state assures that for a period of T7 no signal, especially no wake-up signal TL, is sent on the U interface; that is, no activation procedure is started from the network side. However, a wake-up signal TN from the user side is acknowledged.

Tear Down
In this state transmission is ceased in order to deactivate the basic access and the IEC-Q waits for a response (no signal level, LSU) from the user side.

Tear Down Error
This state is entered after loss of framing was detected. Transmission is ceased in order to deactivate the basic access and the IEC-Q waits for a response (no signal level, LSU) from the user side. EI3 indication is transmitted after a transition forced by RES1 from the wait for TN or EQ training states. In the case of transition from the loss of synchronization state RSY is sent.

Test
This test mode is entered when the unconditional commands RES, SSP, LTD, Pin-RES, Pin-SSP or PFOFF are used. It is left when the pins RESQ, TSP and PS_1 are inactive and the C/I channel code DR is received.

The output signals are as follows:

–when the C/I channel code RES is applied or when the pin RESQ is activated: SL0 and DEAC

–when the C/I channel code SSP is applied or when the pin TSP is activated: single pulses (SP) and DEAC

–when the C/I channel code LTD is applied: SL0 and DEAC; furthermore, the pin DISS is activated

–when the pin PS1 is activated: SL0 and HI

In this state the IEC-Q does not react to the receipt of a wake-up signal TN.

Transparent
This state corresponds to the fully active state in the case of a normal activation for call control. It may be entered in the case of a loopback 2 or a single channel loopback in the NT. The network side is informed that the status "ready for sending" is reached (indication AI). If the user side loses transparency (receipt of act=0), the network side is informed by making use of the C/I channel indication EI2, but no state change is performed.

Wait for Awake Acknowledge
The IEC-Q waits for a response (tone TN from the NT or tone TL in the case of an analog loopback) to the transmission of wake-up signal TL. If no response is received within T3, the state is left for retransmission of a wake-up tone TL. This procedure is repeated until the detection of tone TN or until the expiration of timer T1. In this case the C/I channel indication EI3 is issued, but no state change is performed.

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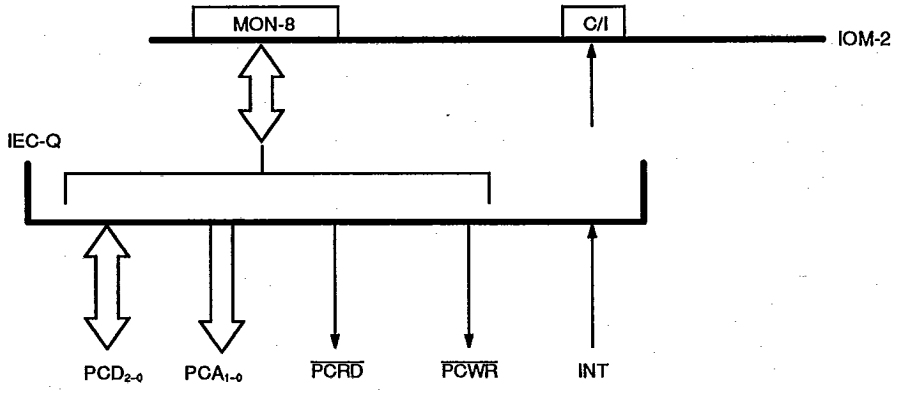
CONTROLLER INTERFACE

A controller interface is implemented to handle control functions via the IOM-2 interface to connect circuits without direct access to a microprocessor. A typical application is the direct connection of the IEPC power controller.

INT

For every change at the input pin (INT) the IEC-Q will transmit a C/I channel code 0110 (INT) in four subsequent IOM frames.

The input condition of the interrupt pin is sampled every four IOM-2 frames.



11892B-27

Figure 25. Controller Interface

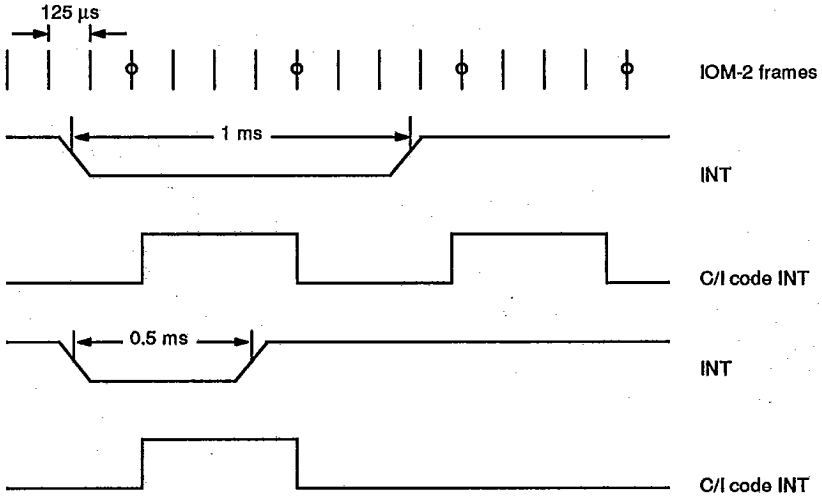


Figure 26. INT

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PCA_{1-0}, PCD_{2-0}, $\overline{PCWR}$, $\overline{PCRD}$

Communication is performed by using the local Monitor message (MON-8) of the IOM-2 interface. The following 2-byte messages are adapted to the IEPC power controller status register read and write operations, but can be used in general too.

MON-8 WCI

1	0	0	0	0	0	0	0

Write Controller Interface

0	1	1	D0	D1	D2	A0	A1

MON-8 RCI

1	0	0	0	0	0	0	0

Read Controller Interface

0	1	0	—	—	—	A0	A1

MON-8 ACI

1	0	0	0	0	0	0	0

Answer Controller Interface

D0	D1	D2	—	—	—	—	—

After the receipt of the Monitor message, the IEC-Q will set the address-/data-bits and generate the read and write pulse. The address-bits are latching, the output is stable until an overwrite by a new dedicated MON-8 message appears.

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DC CHARACTERISTICS

Unless otherwise specified, the static and dynamic characteristic limits apply over a supply voltage range of 4.75 to 5.25 V.

Static Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage		3.5		V_{DD} +0.3	V
V_{IL}	Low Level Input Voltage				1.0	V
I_{IL}	Low Level Input Leakage Current	V_{IN} = DGND	−10			µA
I_{IH}	High Level Input Leakage Current all inputs except A_{IN}, B_{IN}, X_{IN}, X_{OUT}, V_{REF}	$V_{IN} = DV_{DD}$			10	µA
V_{OH1}	High Level Output Voltage all outputs except D_{OUT}	I_{OH1} = 0.4 mA	4.0			V
V_{OH2}	High Level Output Voltage D_{OUT}	I_{OH2} = 6 mA	4.0			V
V_{OL1}	Low Level Output Voltage all outputs except D_{OUT}	I_{OL1} = 0.4 mA			0.33	V
V_{OL2}	Low Level Output Voltage D_{OUT}	I_{OL2} = 6 mA			0.5	V
C_{IN}	Input Capacitance D_{IN}, PS_1, PS_2, DCL, FSC (input), D_{OUT} (open)				10	pF

Power Consumption

All measurements with random 2B+D data in active states, +5 V, 0 to +75°C.

Am2091

Symbol	Parameter	Min	Typ	Max	Unit	Comments
	135 ohm line load		290		mW	Power-up Mode
			50		mW	Power-down LT/NT-PABX Mode
			35		mW	Power-down NT Mode

Am20911

Symbol	Parameter	Min	Typ	Max	Unit	Comments
			150		mW	Power-up Mode
			50		mW	Power-down LT/NT-PABX Mode
			35		mW	Power-down NT Mode

Am20912

Symbol	Parameter	Min	Typ	Max	Unit	Comments
	135 ohm line load		140	160	mW	Power-up Mode
			10	25	mW	Power-down Mode

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Dynamic Characteristics

IOM-2 Interface Timing

Data is transmitted in both directions (DU and DD) at half the data clock rate. The transmitter synchronizes the information to the rising edge.

The data clock (DCL) is a square wave signal with a duty cycle ratio of typically 1:1. The frequency is variable and can be set for values ranging from 512 kHz to 4.096 MHz.

The frame clock (FSC) is an 8-kHz signal for synchronizing data transmission on DU and DD. The rising edge of this signal gives the time reference for the first bit transmitted in the first IOM-2 channel. In the master mode (NT) the output of FSC will mark the position of the superframe by either a single High phase of a DCL period, or a two time High phase of a DCL period is transmitted.

For power saving reasons, the IOM-2 interface can be switched into a "power-down" state. In this case, the idle state of the data lines are High, while those of the clock lines are Low.

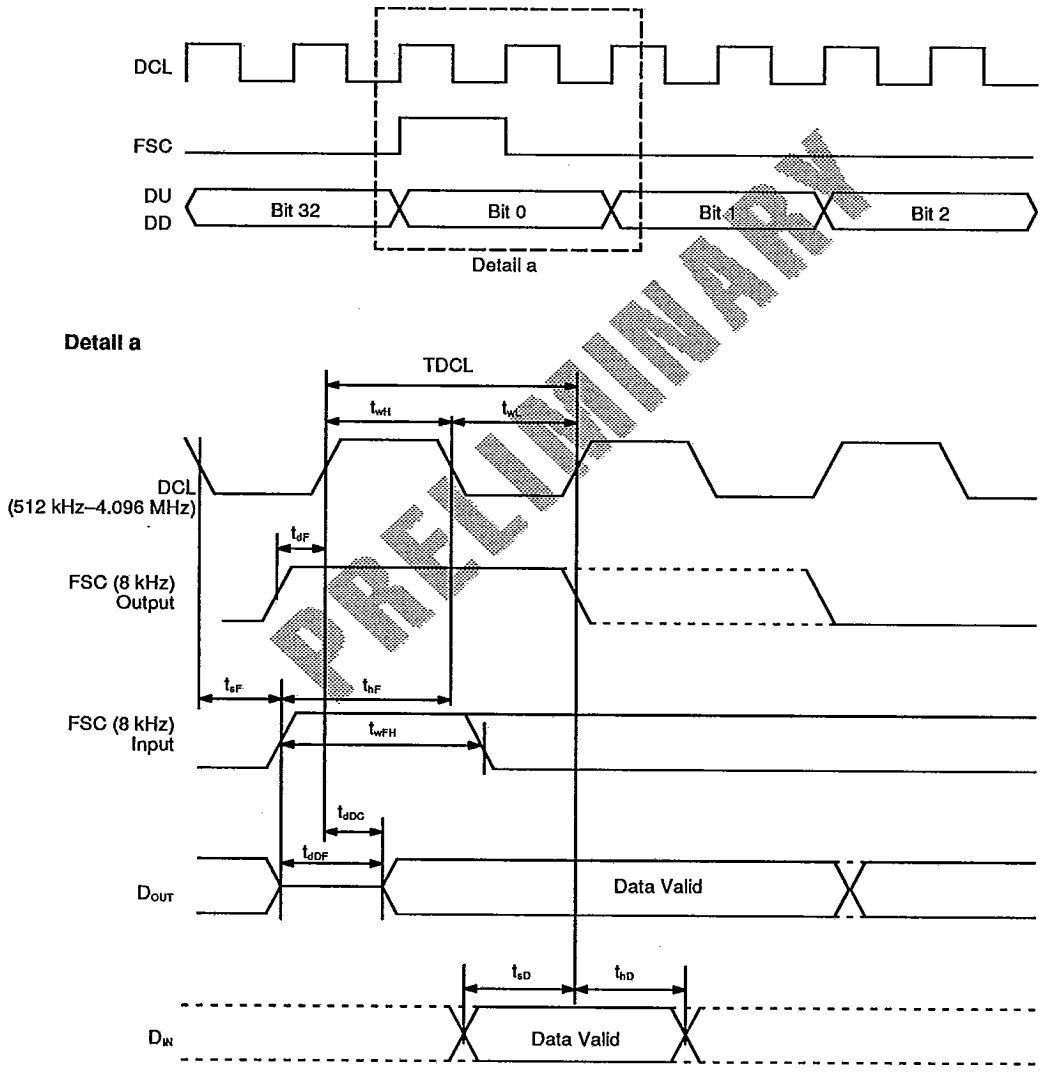

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Figure 27. IOM-2 Interface Timing

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Table 12. Dynamic Input Characteristics

Parameter	Signal	Abbr	Min	Max	Units	Notes
Data Clock	DCL	t_r, t_f		60	ns	
Clock Period	DCL	TDCL	200		ns	
Pulse Width	DCL	t_{wH}, t_{wL}	53		ns	
Frame Sync	FSC	t_r, t_f		60	ns	
Frame Setup	FSC	t_{sF}	30		ns	
Frame Hold	FSC	t_{hF}	30		ns	
Frame Width High	FSC	t_{wFH}	100		ns	
Frame Width Low	FSC	t_{wFL}	2×TDCL		ns	
Data Delay/Frame	D_{OUT}	t_{dDF}		150	ns	1
Data Setup	D_{IN}	t_{sD}	$t_{wH}+20$		ns	
Data Hold	D_{IN}	t_{hD}	50		ns	

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Table 13. Dynamic Output Characteristics

Parameter	Signal	Abbr	Test Condition	Min	Typ	Max	Units	Notes
Data Clock	DCL	t_r, t_f	CL = 25 pF			30	ns	
Clock Period	DCL	TDCL	CL = 25 pF	1875	1953	2035	ns	2
Pulse Width	DCL	t_{wH}, t_{wL}		880	977	1075	ns	2
Clock Period	DCL	TDCL	CL = 25 pF	565	651	735	ns	3
Pulse Width	DCL	t_{wH}, t_{wL}		230	325	420	ns	3
Frame Width High Superframe	FSC	t_{wFH}	CL = 25 pF		TDCL			
Frame Width High Normal Frame	FSC	t_{wFH}	CL = 25 pF		2×TDCL			
Frame Sync.	FSC	t_r, t_f	CL = 25 pF			30	ns	
Frame Delay	FSC	t_{dF}	CL = 25 pF	160	130	100	ns	
Data Out	D_{OUT}	t_f	C = 150 pF R = 1 kohm to V_{DD} DOD pin High or RESQ pin Low			200	ns	
Data Out	D_{OUT}	t_r, t_f	C = 150 pF DOD pin Low RESQ pin High			150	ns	
Data Delay/Clock	D_{OUT}	t_{dDC}	CL = 150 pF			100	ns	
Data Setup	D_{IN}	t_{sD}		$t_{wH}+20$			ns	
Data Hold	D_{IN}	t_{hD}		50			ns	

PRELIMINARY

Notes: 1. Condition CL = 150 pF
2. 256 kb/s
3. 768 kb/s

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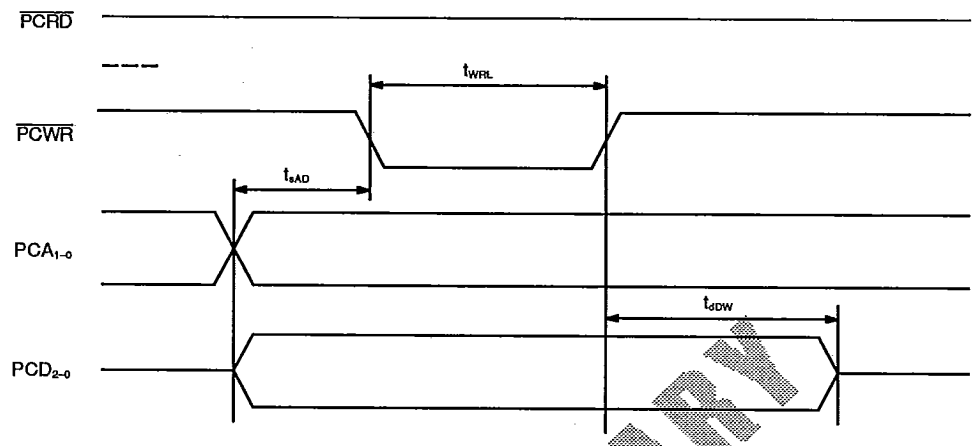
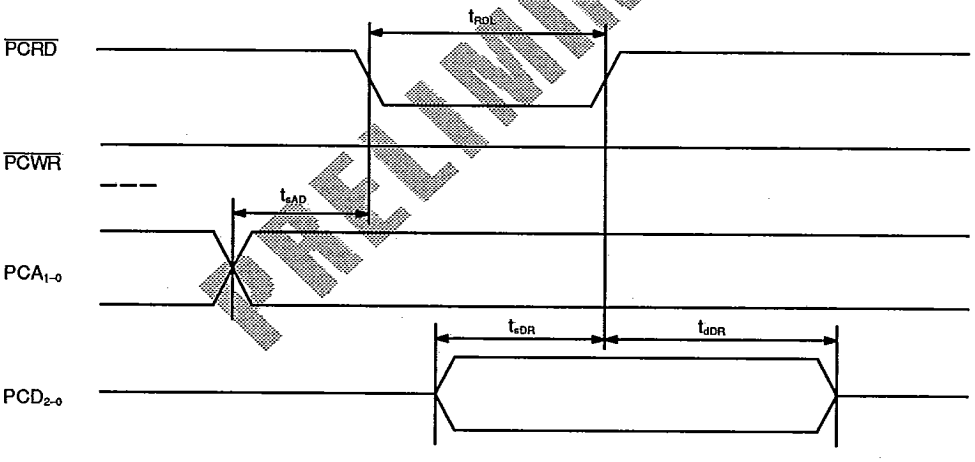
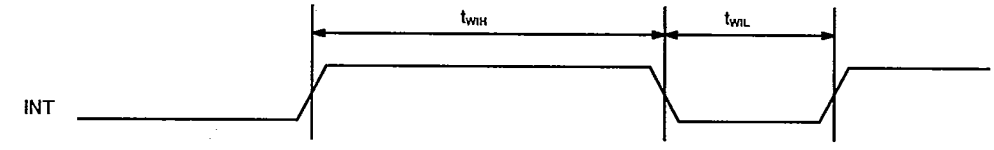
WRITE Access



READ Access



Interrupt



11892B-30

Figure 28. Controller Interface Timing

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Table 14. Dynamic Characteristics

Parameter	Signal	Abbr	Min	Typ	Max	Units
Write Clock	PCWR	t_r, t_f			30	ns
Write Width	PCWR	t_{WRL}		4×TDCL		
Address Setup	PCA_{+}	t_{sAD}		2×TDCL		
Data Delay Write	PCD_{2-0}	t_{dDW}		2×TDCL		
Data Delay Read	PCD_{2-0}	t_{dDR}	130			ns
Setup Data Read	PCD_{2-0}	t_{sDR}	130			ns
Read Clock	PCRD	t_r, t_f			30	
Read Width	PCRD	t_{RDL}		4×TDCL		
Interrupt Length	INT	t_{WIH}	0.5			ms
		t_{WIL}	0.5			ms

PRELIMINARY

All test condition: CL = 25 pF

Am20912 ANALOG LINE PORT FUNCTIONS

The analog part of the IEC-Q consists of three main building blocks:

–the analog-to-digital converter in the receive path

–the digital-to-analog converter and

–the output buffer in the transmit path

Furthermore, it contains some special functions. These are:

–the analog test loop

–the range function (damping of the input signal)

–the level detect function (starting activation of the IEC-Q)

Analog-to-Digital Converter (ADC)

The ADC was specially developed for this application. It is a sigma-delta modulator of second order using a clock rate of 15.36 MHz. This means a ratio clock frequency/baseband width of 192 or 7 octaves. The output signal is converted to a standard digital word in a special digital filter. At the output of this digital filter a resolution and linearity of 65 dB or approximately 11 bits is achieved. The input signal to this ADC can be damped by 6 dB, activating the range function. The ADC can be internally tied to the output of the transmitter activating the loop function. Range and loop can be activated simultaneously, but then the damping is approximately 12 dB.

Input Signal Range

The peak input signal, measured between A_{IN} and B_{IN}, must be below 4 V peak-to-peak. The maximum SNR is achieved with 1.3 Vpp (range inactive) or 2.6 Vpp (range active) input signal voltage.

Input Impedance

The input impedance, measured between A_{IN} and B_{IN}, is at least 50K.

Special Functions

Range Function

For short lines, the input signal to the ADC is automatically attenuated by 6 dB ±1 dB in order to lower the High receive signal.

Loop Function

An external loop command in the C/I channel activates an internal analog test loop from the output pins to the input pins of the IEC-Q. The signal is attenuated by 12 dB within this loop.

Level Detect

The level detect circuit evaluates the differential signal between A_{IN} and B_{IN}. The differential threshold level is between 12 and 41 mV. The DC level (common mode level) may be between 0 and 3 V. Level detect is not affected by the loop and range setting.

Digital-to-Analog Converter (DAC)

The shape of the output pulse is formed in a special DAC. The DAC was specially optimized for excellent matching between positive and negative pulses and high linearity. It uses a fully differential switched-capacitor approach. The staircase-like output signal of the DAC drives the output buffers. The shape of the DAC output signal is shown below, with the peak amplitude normalized to one. This signal is fed to the output through a switched-capacitor lowpass and an RC lowpass of first order with a corner frequency of 1 MHz ±50%.

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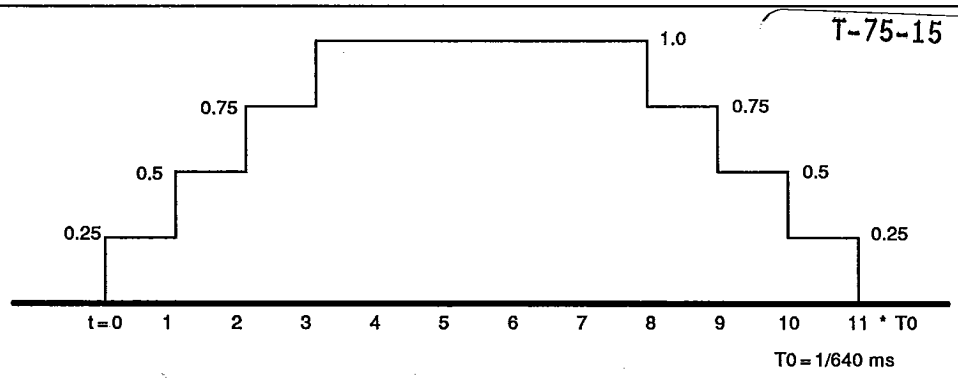

Figure 29. DAC Output for a Single Pulse 11892B-31

The duration of each output pulse is 11 steps, with t = 1/640 ms per step. On the other hand, the pulse rate is 80 kHz or one pulse per 8 steps. Thus, subsequent pulses are overlapping for a duration of 3 steps.

Symbol Rate

The symbol rate is 80 kbaud ±1 ppm and applies to synchronous symbol transmission with a clock generated by LT circuits.

Output Stage

The output stage consists of two identical buffers, operated in a differential mode. This concept allows an output voltage swing of 6.4 V peak-to-peak at the output pins of the IEC-Q. The buffers are optimized for:

–high output swing

–high linearity

–low quiescent current to minimize power consumption.

The output jitter produced by the transmitter (with jitter-free input signals) is below 0.02 UIpp measured with a high pass filter of 30 Hz cutoff frequency. Without the filter, the output jitter is below 0.1 UIpp.

Pulse Shape

The pulse mask for a single positive pulse measured between AOUT and BOUT with a load of 102 ohms is given in the following figure.

Signal Amplitude

The peak-to-peak voltage of a single positive pulse measured between AOUT and BOUT and terminated with 102 ohms is 3.3 V ±8%.

Offset Voltage

The offset voltage, measured under the same conditions as above, is less than 2% of the peak amplitude.

Signal Stability

The signal amplitude measured over a period of one minute varies less than 1%.

Output Impedance

The output impedance measured between AOUT and BOUT is below 4 ohms in power-up and below 12 ohms in power-down mode. The required impedance of 135 ohms ±5% seen from the line side of the transformer is established by putting two resistors of 25 ohms ±1% each in the hybrid.

Load

The load is given by the hybrid, the transformer and the subscriber line. The transformer ratio should be 1:1.32 (circuit/line side) and the total inductivity seen from the line side between 10 and 15 mH.

Noise and Distortion Level

The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 80 kHz, is at least 60 dB below the signal for an evenly distributed but otherwise random sequence of +3, +1 and -1, -3.

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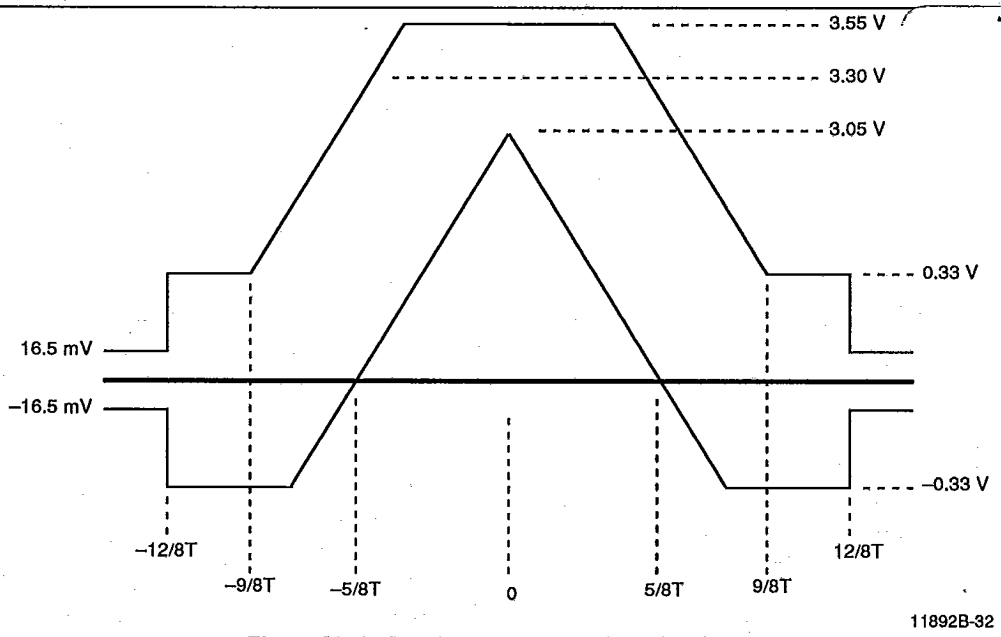

Figure 30. Pulse Mask for a Single Positive Pulse

Table 15. Specified Data of Analog Functions

Parameter	Min	Typ	Max	Units
Receive Path:				
Signal/(Noise + Dest.)	57	62		dB
DC-level at AD-Output	0.45	0.5	0.55	V
Threshold of Level Detect	12		41	mV
Transmit Path:				
Signal/(Noise + Dest.)	60	65		dB
Output DC-level	2.05	2.375	2.6	V
Offset between A_{OUT}/B_{OUT}			35.5	mV
Signal Amplitude	2.95	3.2	3.45	V
Output Impedance between A_{OUT}/B_{OUT}:				
Power-up		2	4	ohm
Power-down		6	12	ohm
Power Consumption (135 ohm line load, random 2B+D data):				
Power-up		140	160	mW
Power-down		10	25	mW

(T_A = 70°C, V_{DD} = 4.75 V)

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Clock Generation

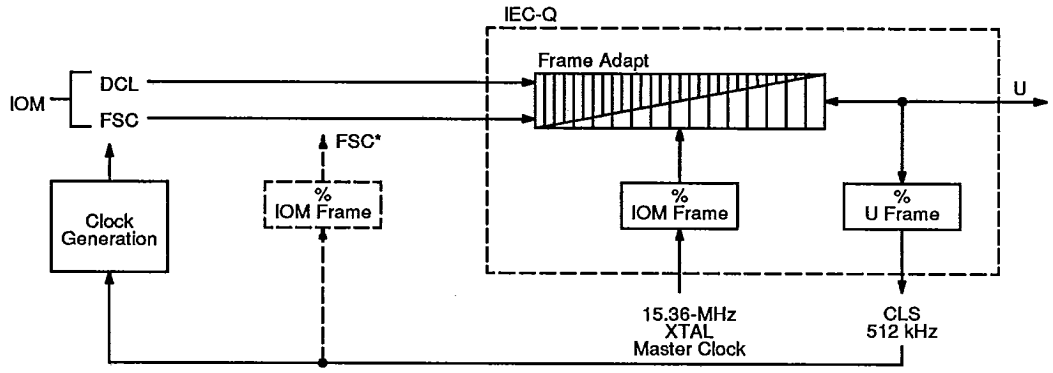
NT Modes

The master clock is derived from a built in crystal oscillator. The crystal is connected to the pins X_{IN} and X_{OUT}. The maximum capacitive load at X_{IN} is 60 pF each.

Master clock:
Nominal frequency: 15.36 MHz
Overall tolerance: ±100 ppm

A crystal (serial resonance) is connected which meets the following specification:

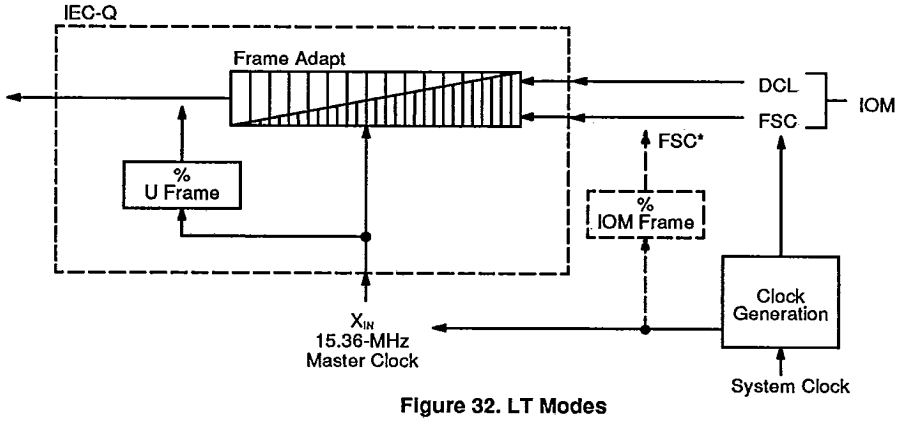
Nominal frequency: 15.36 MHz
Overall tolerance: ±60 ppm
Load capacitance: 20 pF
Resonance resistance: 20 ohm
Shunt capacitance: 7 pF



Max difference of phase deviation of FSC and FSC* : ±18 µs

11892B-33

Figure 31. NT-PABX Mode



11892B-34

Figure 32. LT Modes

In the LT modes, the timing signals are derived from the system clock via an external phase locked loop. The master clock is fed to pin X_{IN}.

Master clock:
Nominal frequency: 15.36 MHz
Duty ratio: 0.4–0.6
Rise and fall times: <10 ns
Max low freq. phase wander within 1 period: ±0.85 ps
Jitter (peak-to-peak):
Max difference of phase deviation of FSC and FSC*: ±18 µs
Start of activation, phase difference: 0

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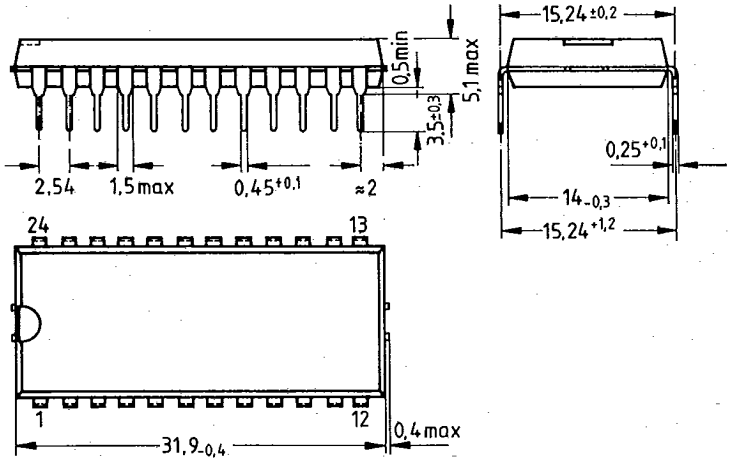
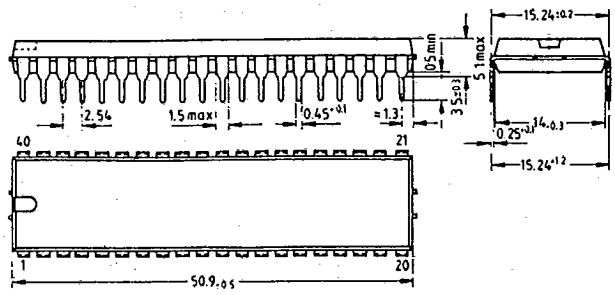
PHYSICAL DIMENSIONS

T-75-15

PD024



PD040



Note: Physical dimensions are given in mm.
Distance pin to pin: 2.54 mm
Package Width: 15.24 mm

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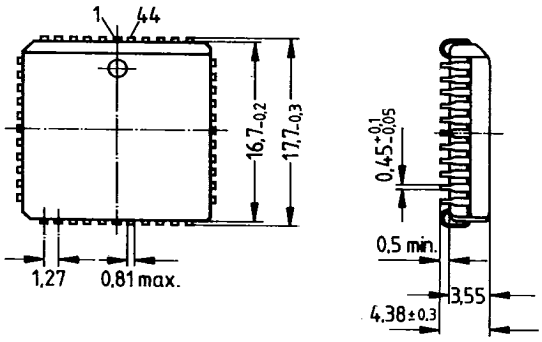
PL044



Note: Physical dimensions are given in mm.
Distance pin to pin: 2.54 mm
Package Width: 15.24 mm

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