National Semiconductor

COP452L/COP352L Frequency Generator and Counter

General Description

The COP452L and COP352L are peripheral members of the COPS™ family fabricated using N-channel silicon gate MOS technology. Containing two independent 16-bit counter/register pairs, they are well suited to a wide variety of tasks involving the measurement and/or generation of times and/or frequencies. Included in the features are multiple tone generation, precise duty cycle generation, event counting, waveform measurement, frequency bursts, delays, and "white noise" generation. An on-chip zero crossing detector can trigger a pulse with a programmed delay and duration. The COP352L is the extended temperature version of the COP452L. The COP352L is the functional equivalent of the COP452L.

The COP452L series peripheral devices can perform numerous functions that a microcontroller alone cannot perform. They can execute one or more complex tasks, attaining higher accuracies over a broader frequency range than a microcontroller alone. These devices remove repetitive yet demanding counting, timing, and frequency related functions from the microcontroller, thereby freeing it to perform other tasks or allowing the use of a simpler microcontroller in the system.

Features

- Unburdens microcontroller by performing "mundane" tasks
- Wider range and greater accuracy than microcontroller alone
- Generates frequencies, frequency bursts, and complex waveforms
- Measures waveform duty cycle
- Two independent pulse/event counters
- True zero crossing detector triggers output pulse
- White noise generator
- Compatible with all COP400 microcontrollers
- MICROWIRE™ compatible serial I/O
- 14-pin package
- Single supply operation (4.5V–6.3V, COP452L; 4.5V–5.5V, COP352L)
- Low cost
- TTL compatible

Block Diagram

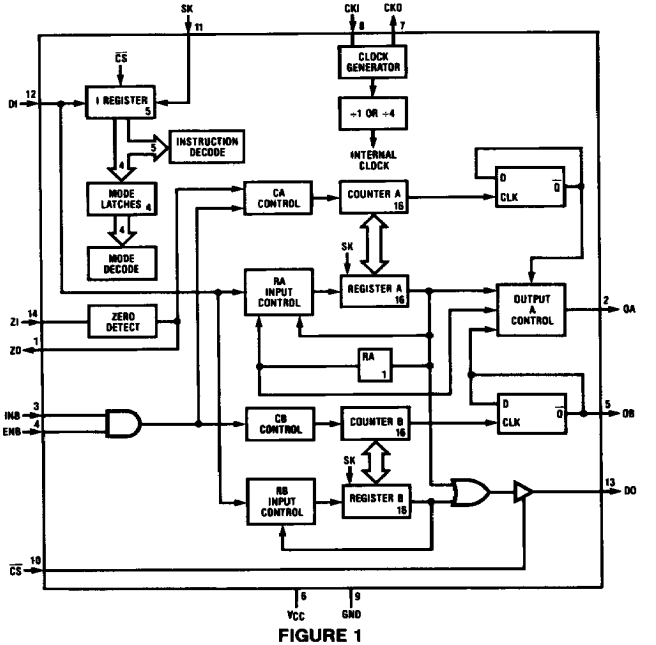

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FIGURE 1

COP452L
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (except ZI) relative to GND	−0.5V to +7.0V
Voltage at Pin ZI relative to GND	−0.8 to +10V
Sink Current, Output OA	15 mA
Sink Current, All Other Outputs	5 mA
Total Sink Current	35 mA
Source Current, Outputs OA, OB	5 mA
Source Current, All Other Outputs	1 mA
Total Source Current	10 mA
Ambient Operating Temperature	0°C to 70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.5W at 25°C 0.2W at 70°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $0°C \le T_A + 70°C$, $4.5V \le V_{CC} \le 6.3V$ (COP452L), unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	All Outputs Open		14	mA
Input Voltage Levels				
CKI Input Levels	V_{CC} = Max.	3.0		V
Logic High (V_{IH})	V_{CC} = 5.0V ±5%	2.0		V
Logic Low (V_{IL})			0.4	V
DI, INB, ENB, SK, $\overline{CS}$				
Logic High	V_{CC} = Max.	3.0		V
Logic High (V_{IH})	V_{CC} = 5.0V ±5%	2.0		V
Logic Low (V_{IL})			0.8	V
ZI Input Voltage		−0.8	+10	V
Impedance to GND at ZI		−1.6	7.8	kΩ
ZI Offset Voltage	(Note 1)		150	mV
Output Voltage Levels				
TTL Operation	V_{CC} = 5.0V ±5%			
Logic High (V_{OH})	I_{OH} = 100 μA	2.4		V
Logic Low (V_{OL})	I_{OL} = −1.6 mA		0.4	V
Maximum Allowable Output Current Levels				
Sink Current				
OA	(Note 2)		15	mA
All Other Outputs	(Note 2)		5.0	mA
Total Sink Current	(Note 3)		35	mA
Source Current				
OA, OB	(Note 2)		−5.0	mA
All Other Outputs	(Note 2)		−1.0	mA
Total Source Current	(Note 3)		−10	mA

Note 1: ZI offset voltage is the absolute value of the difference between the voltage at ZI and ground (pin 9) that will cause the zero detect circuit output to change state. This is the maximum value which takes into account the worst case effects of process, temperature, voltage, and gain variation.

Note 2: The maximum current for the specified pin must be limited to this value or less.

Note 3: The total current in the device must be limited to this value or less.

COP452L
AC Electrical Characteristics $0°C \le T_A \le 70°C$, $4.5V \le V_{CC} \le 6.3V$ unless otherwise specified

Parameter		Conditions	Min	Max	Units
CKI Input Frequency (f_{IN})		÷4 Mode	100	2100	kHz
		÷1 Mode	64	525	kHz
Duty Cycle		÷4	30	55	%
÷1		÷1	45	55	%
Rise Time (t_r)		f_{IN} = 2.1 MHz		50	ns
Fall Time (t_f)		f_{IN} = 2.1 MHz		40	ns
SK Input Frequency			25	250	kHz
SK Duty Cycle			30	70	%
Internal Clock Frequency (f_I)			25	525	kHz
Internal Count Rate			0	$f_I/2$	Hz
Output Frequency			$f_I/131072$	$f_I/2$	Hz
Inputs					
DI	t_{SETUP}		800		ns
	t_{HOLD}		1.0		μs
Outputs					
CKO	t_{pd1}	C_L = 50 pF		0.2	μs
	t_{pd0}			0.2	μs
ZO	t_{pd1}	ZI = Sine Wave *(Figure 4)*		0.7	μs
	t_{pd0}			0.6	μs
DO	t_{pd1}	C_L = 50 pF		1.0	μs
	t_{pd0}			0.6	μs
OA	t_{pd1}	C_L = 50 pF		0.7	μs
		V_{OUT} = 1.5V			
	t_{PD0}			0.8	μs
OB	t_{pd1}			1.0	μs
	t_{pd0}			0.4	μs

COP352L
Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (except ZI) relative to GND	−0.5V to +7.0V
Voltage at Pin ZI relative to GND	−0.8V to +10V
Sink Current, Output OA	15 mA
Sink Current, All Other Outputs	5 mA
Total Sink Current	35 mA
Source Current, Outputs OA, OB	5 mA
Source Current, All Other Outputs	1 mA
Total Source Current	10 mA
Ambient Operating Temperature	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Power Dissipation	0.5W at 25°C 0.125W at 85°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics $-40°C \le T_A \le 85°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})		4.5	5.5	V
Operating Supply Current	All Outputs Open		16	mA
Input Voltage Levels				
CKI Input Levels	V_{CC} = Max.	3.0		V
Logic High (V_{IH})	V_{CC} = 5.0V ±5%	2.2		V
Logic Low (V_{IL})			0.3	V
DI, INB, ENB, SK, $\overline{CS}$				
Logic High	V_{CC} = Max.	3.0		V
Logic High (V_{IH})	V_{CC} = 5.0V ±5%	2.2		V
Logic Low (V_{IL})			0.6	V
ZI Input Voltage		−0.8	+10	V
Impedance to GND at ZI		1.6	7.8	kΩ
ZI Offset Voltage	(Note 1)		150	mV
Output Voltage Levels				
TTL Operation	V_{CC} = 5.0V ±5%			
Logic High (V_{OH})	I_{OH} = 100 μA	2.4		V
Logic Low (V_{OL})	I_{OL} = −1.6 mA		0.4	V
Maximum Allowable Output Current Levels				
Sink Current				
OA	(Note 2)		15	mA
All Other Outputs	(Note 2)		5.0	mA
Total Sink Current	(Note 3)		35	mA
Source Current				
OA, OB	(Note 2)		−5.0	mA
All Other Outputs	(Note 2)		−1.0	mA
Total Source Current	(Note 3)		−10	mA

Note 1: ZI offset voltage is the absolute value of the difference between the voltage at ZI and ground (pin 9) that will cause the zero detect circuit output to change state. This is the maximum value which takes into account the worst case effects of process, temperature, voltage, and gain variation.

Note 2: The maximum current for the specified pin must be limited to this value or less.

Note 3: The total current in the device must be limited to this value or less.

COP352L
AC Electrical Characteristics $-40°C \le T_A \le +85°C$, $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified

Parameter		Conditions	Min	Max	Units
CKI Input Frequency (f_{IN})		÷4 Mode	256	2100	kHz
		÷1 Mode	64	525	kHz
Duty Cycle		÷4	35	55	%
		÷1	50	55	%
Rise Time (t_r)		f_{IN} = 2.1 MHz		50	ns
Fall Time (t_f)		f_{IN} = 2.1 MHz		40	ns
SK Input Frequency			25	250	kHz
SK Duty Cycle			30	70	%
Internal Clock Frequency (f_I)			64	525	kHz
Internal Count Rate			0	$f_I/2$	Hz
Output Frequency			$f_I/131072$	$f_I/2$	Hz
Inputs					
DI	t_{SETUP}		800		ns
	t_{HOLD}		1.0		μs
Outputs					
CKO	t_{pd1}	C_L = 50 pF		0.25	μs
	t_{pd0}			0.25	μs
ZO	t_{pd1}	ZI = sine wave *(Figure 4)*		0.8	μs
	t_{pd0}			0.7	μs
DO	t_{pd1}	C_L = 50 pF		1.1	μs
	t_{pd0}			0.7	μs
OA	t_{pd1}	C_L = 50 pF		0.7	μs
		V_{OUT} = 1.5V			
	t_{pd0}			0.8	μs
OB	t_{pd1}			1.0	μs
	t_{pd0}			0.4	μs

Timing Diagrams

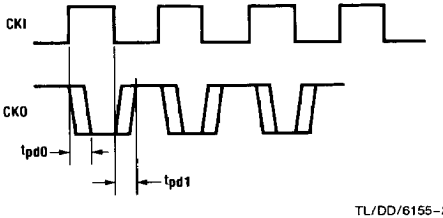

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FIGURE 2a. CKO Output Timing

FOR DUTY CYCLE, TRIGGERED PULSE AND TRIGGERED PULSE AND COUNT

FOR OTHER MODES

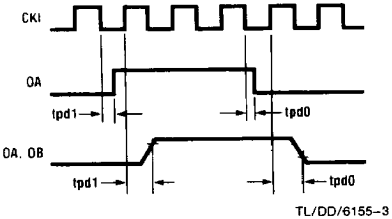

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FIGURE 2b. OA and OB Output Timing

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Timing Diagrams (Continued)

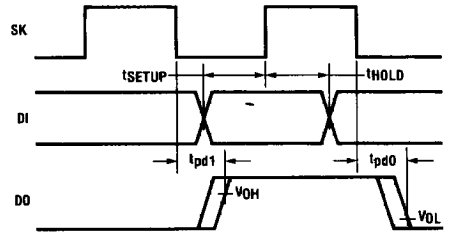

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FIGURE 3a. Synchronous Data Timing

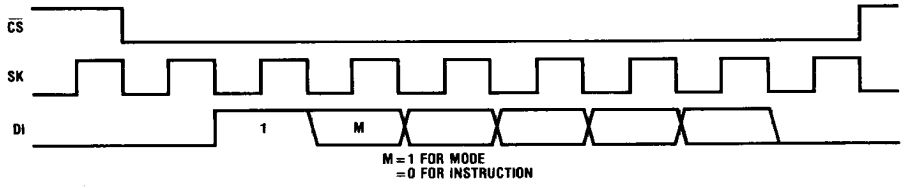

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FIGURE 3b. Instruction Timing (Except Read/Write)

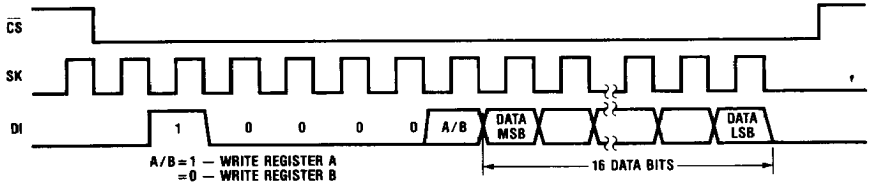

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FIGURE 3c. Write Instruction Timing

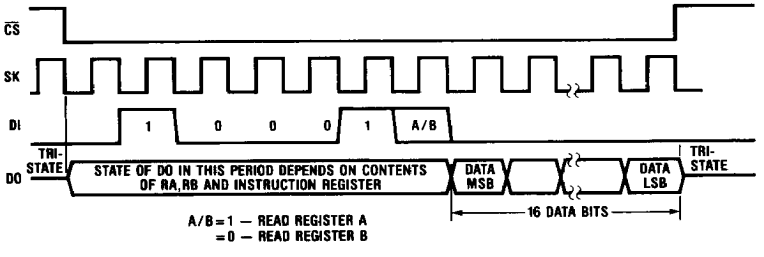

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FIGURE 3d. Read Instruction Timing

Timing Diagrams (Continued)

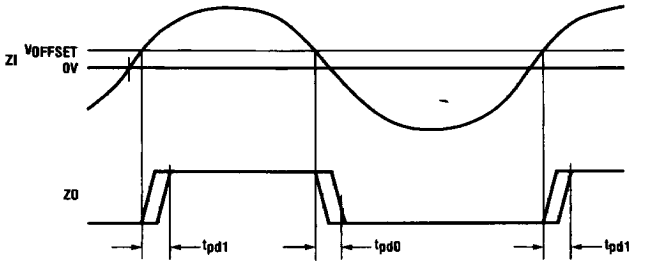

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FIGURE 4a. ZO Timing, $V_{OFFSET} > 0V$

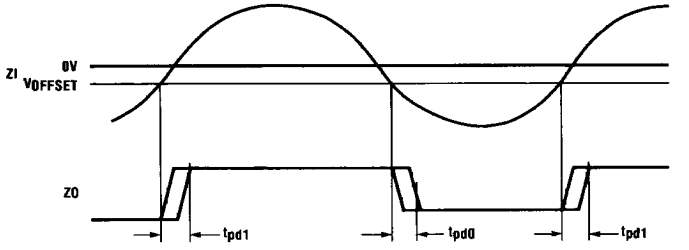

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FIGURE 4b. ZO Timing, $V_{OFFSET} < 0V$

Pin Descriptions

Pin	Description	Pin	Description
ZO	Zero Cross Output Signal	CKI	Crystal Oscillator Input
OA	Counter A, Logic Controlled Output	GND	Ground
INB	Counter B, External Input	$\overline{CS}$	Chip Select
ENB	Enable for INB	SK	Serial Data I/O Clock Input
OB	Counter B Output	DI	Serial Data Input
V_{CC}	Power Supply	DO	Serial Data Output
CKO	Crystal Oscillator Output	ZI	AC Waveform Input, Counter A External Input

Connection Diagram

Dual-In-Line Package

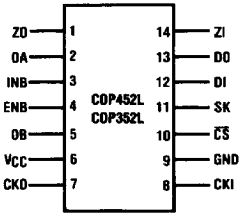

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FIGURE 5. Pin Connection Diagram

Order Number COP452D, COP352D, COP452N or COP352N
See NS Package Number D14D or N14A

Typical Performance Characteristics

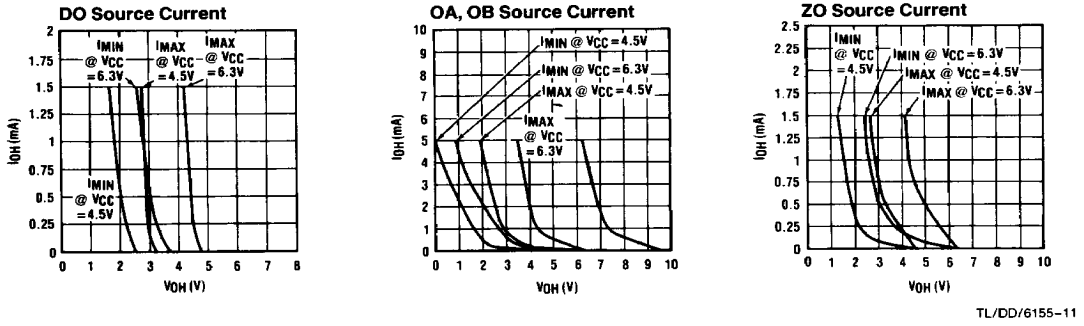

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FIGURE 6. COP452L

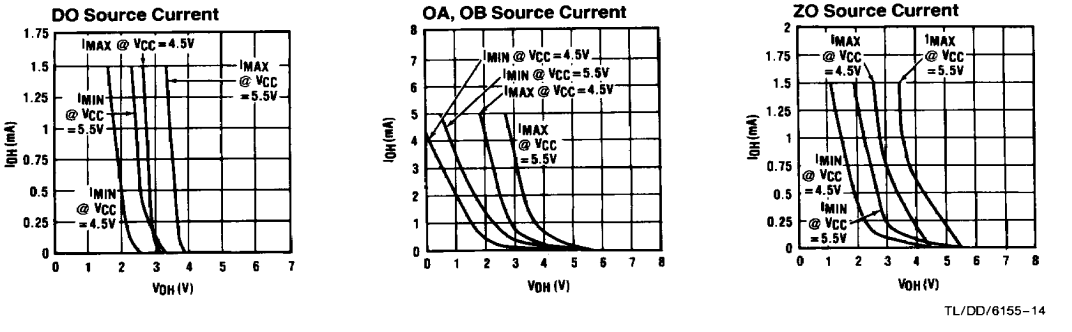

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FIGURE 7. COP352L

Functional Description

The COP452L and COP352L are functionally identical devices. They differ only in V_{CC} range and/or operating temperature range, and certain electrical parameters associated with those temperature and voltage ranges. The following information will refer only to the COP452L. All the information, however, applies equally to the COP452L and COP352L.

INSTRUCTION SET AND OPERATING MODES

The COP452L has ten instructions and eleven operating modes as indicated in *Figure 8*. The information for the instruction or mode is sent to the COP452L via the serial interface. The MSB is always a "1" and is properly viewed as a start bit. The second MSB identifies the communication as an instruction or a mode. The lower four bits contain the command for the device.

Instruction	Opcode MSB LSB	Comments
LDRB	100000	Load register B from DI
LDRA	100001	Load register A from DI
RDRB	100010	Read register B to DO
RDRA	100011	Read register A to DO
TRCB	100100	Transfer register B to counter B
TRCA	100101	Transfer register A to counter A
TCRB	100110	Transfer counter B to register B
TCRA	100111	Transfer counter A to register A
CK1	101000	CKI divide by one
CK4	101001	CKI divide by four
LDM	11xxxx	Load mode latches

FIGURE 8a. COP452L Instruction Set

Operating Mode	Opcode MSB LSB
Reset	111111
Dual Frequency	110000
Frequency and Count	110100
Dual Count	110101
Number of Pulses	110010
Duty Cycle	110011
Waveform Measurement	110110
Triggered Pulse	110001
Triggered Pulse and Count	110111
White Noise and Frequency	111000
Gated White Noise	111001

FIGURE 8b. COP452L Operating Modes

A block diagram of the COP452L is given in *Figure 1*. Positive logic is used. The COP452L can execute ten instructions as indicated in *Figure 8a*, and has eleven operating modes. The operating mode is under user software control.

The device basically consists of two sixteen bit shift registers and two sixteen bit binary down counters organized as two register-counter pairs. In most operating modes, the two register-counter pairs are completely independent of one another. For frequency generation, both the register and counter of a given pair are utilized. The counter counts down to zero where a toggle flip-flop is toggled. Then the data in the register is loaded, automatically, to the counter and the process continues. A similar procedure is used in the duty cycle mode and number of pulses modes. For counting, the counters count the pulses at their respective inputs. There is no automatic counter-register transfer in the count modes. The counters wraparound from 0 to FFFF in the count modes. Data I/O is via the serial port and the registers. The counters are not involved in the input/output process at all.

The device requires a low chip select signal. When the device is selected ($\overline{CS}$ low) the driver on the DO pin is enabled and the device will accept data at DI on each SK pulse. When the device is deselected ($\overline{CS}$ high) the DO driver is TRI-STATE® and the I register is reset to 0. Note that chip select does not affect any other portion of the device. The mode latches are not affected. The COP452L will continue to operate in the mode specified by the user until the mode is changed by the user.

The COP452L contains a clock generator. The user may connect a crystal network to CKI and CKO or he may drive CKI from an external oscillator. Certain RC and LC networks may also be used. See the applications for further information.

The user also has control over whether the clock generator divides the CKI signal by 4 or 1. This allows the user to quickly get a 4 to 1 change in frequency output or input count rates. Alternatively, it allows the user to use a higher speed crystal or clock generator. The internal clock frequency (the frequency after the divider) must remain between the specified limits to guarantee proper operation. The state of the divider is not affected by $\overline{CS}$.

There is an internal power-on reset circuit which places the device in the Reset mode (mode latches all set to 1) and sets the clock divider to divide by four. If the CKI frequency is less than four times the minimum internal frequency the first access of the COP452L *must* be the command to set the divider to divide by 1. This command will be accepted and will be processed. Proper operation of the COP452L is not guaranteed if the internal frequency is less than the specified minimum. The power-on reset circuit does not affect the counter and registers of the COP452L.

When the COP452L is subjected to rapid power supply cycling, the internal power on reset will not function. Power must be removed for at least 20 seconds to allow restoration of internal reset circuitry. If the application requires power on-off cycles more frequently than once each 20 seconds the software reset with proper CKI divide by must be used to establish the initial state of the COP452L.

INSTRUCTION DESCRIPTION

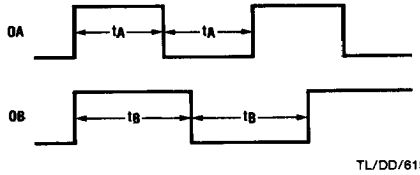
1. **Load Register (LDRA/LDRB)**—The selected register (A/B) is loaded with 16 bits of data shifted in on DI and clocked in by SK.
2. **Read Register (RDRA/RDRB)**—The data in the selected register (A/B) is shifted out serially onto DO. At the same time the data is recirculated back to the register.
3. **Load Counter (TRCA/TRCB)**—The contents of the selected register are transferred to its associated counter. (Counter A is loaded from register A; counter B is loaded from register B.) The contents of the register are unaffected.
4. **Copy Counter (TCRA/TCRB)**—The contents of the selected counter are transferred to its associated register. (Counter A loads register A; counter B loads register B.) The contents of the counter are unaffected.

Functional Description (Continued)

5. **CKI Divide by One**—The oscillator divider at the CKI input is set to divide by one. The internal frequency is therefore equal to the CKI frequency. This instruction should not be used if the CKI frequency is greater than the maximum internal frequency.
6. **CKI Divide by Four**—The oscillator divider at the CKI input is set to divide by four. The internal frequency is therefore equal to one-fourth of the CKI frequency. This instruction should not be used if the CKI frequency is less than four times the minimum internal frequency.
7. **Load Mode Latches**—The four mode latches are loaded with the lower four bits of the instruction.

MODE DESCRIPTION

1. **Reset Mode**—This mode sets OA and OB to "0". The mode latches are all set to "1". No counting occurs; the COP452L is in an idle condition. The registers and counters are not altered in any way.
2. **Dual Frequency**—Two frequencies are generated—one at output OA and one at output OB. The period of the square wave at OA is determined by the contents of register A. The period of the square wave at OB is determined by the contents of register B. In frequency generation modes, the counters count down until they reach zero. At that point the output toggles and the counters are automatically loaded from the respective registers. The counters are only loaded when they count down to zero. Therefore it may be necessary to initially load the counters. The frequency outputs at OA and OB are completely independent of one another. The respective counter inputs (INB, ZI) have no effect on the counters in this mode.



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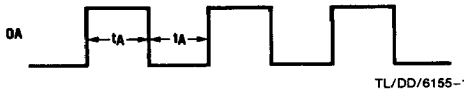
$t_A = (A + 1)t$
$t_B = (B + 1)t$
$0 \le A \le 65535; 0 \le B \le 65535$

Where: A = Contents of register A
B = Contents of register B
t = Period of internal clock
= Period of CKI oscillator (÷ mode)
= 4 × period of CKI oscillator (÷4 mode)

Period of output square wave = 2(N + 1)t
Where t is devined above
N = Contents of register
$0 \le N \le 65535$ ($0 \le N \le FFFF_{16}$)

3. **Frequency and Count**—A single frequency is output at OA. Counter B counts external pulses on INB (when ENB = 1). There is no automatic clear of the counter. Since counter B counts down from whatever state it is in it is usually desirable to preload the counter. Preloading the counter with all zeroes will give the two's complement of the count. Preloading the counter with all ones will give the one's complement of the count.



TL/DD/6155-18

$t_A = (A + 1)t$

Where: A = Contents of register A
t = Period of internal clock
(as previously defined)
$0 \le A \le 65535$ ($0 \le A \le FFFF_{16}$)

OB toggles each time counter B counts through zero.

Maximum count rate at INB = $f_I/2$

Where: f_I = Internal Clock frequency
= CKI input frequency (÷1 mode)
= CKI input frequency ÷4 (÷4 mode)

Minimum pulse width required for reliable counting = t
where t = period of internal clock.

4. **Dual Count**—In this mode counter A and counter B are enabled as external event or pulse counters. Counter A counts pulses at ZI and counter B counts pulses at INB (when ENB = 1). There is no automatic clear of either counter. Each counter counts down from whatever state it starts in. Thus, to ease reading the information, the counters should be preloaded. Preloading the counters with all zeroes will give the two's complement of the count. Preloading the counters with all ones will give the one's complement of the count. The circuitry which decrements the counters is enabled by the high to low transition at the count input. There is no interaction between the two register counter pairs.

OA toggles every time counter A counts through "0".

OB toggles every time counter B counts through "0".

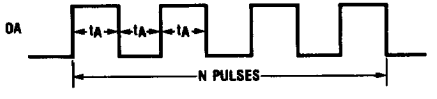
The counters, when counting, count down and wrap around from 0 to FFFF and continue counting down.

Maximum count rate = $f_I/2$
where: f_I = internal clock frequency

Minimum pulse width = t
where: t = period of internal clock
(as previously defined).

There is no requirement that the count signal be symmetrical. The pulse width low must be at least equal to t. The pulse width high must also be at least equal to t.

5. **Number of Pulses Mode**—This mode outputs at OA a specified number of pulses of a specified width. The number of pulses is specified by the contents of register B. The pulse width is specified by the contents of register A.



TL/DD/6155-19

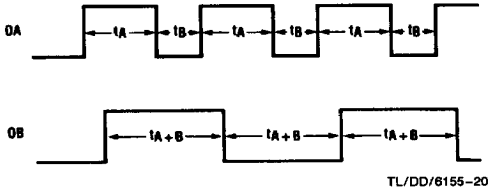
$t_A = (A + 1)t$
$N = B + 1$

Where: A = Contents of register A
B = Contents of register B
t = period of internal clock
(as previously defined)
$1 \le A \le 65535, A \ne 0$ ($1 \le A \le FFFF_{16}$)
$0 \le B \le 65535$ ($0 \le B \le FFFF_{16}$)

Functional Description (Continued)

OB toggles each time a pulse train is generated at OA. The pulse is generated each time the COP452L is selected and an instruction is set to the device. Counter B is automatically loaded from register B after the N pulses are generated. Counter A is automatically loaded from register A at each transition of OA. Therefore simply reloading the number of pulses mode will repeat the previous sequence.

6. Duty Cycle Mode—This mode generates a rectangular waveform at OA. The pulse width high is specified by the contents of register A. The pulse width low is specified by the contents of register B. A combination square wave signal is generated at OB.



TL/DD/6155–20

$t_A = At$

$t_B = Bt$

$t_{A+B} = (A + B)t$

Where: A = Contents of register A

B = Contents of register B

t = period of internal clock (as previously defined)

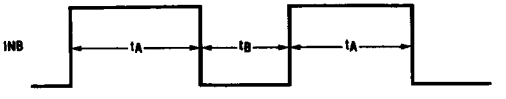
$1 \le A \le 65535$, $A \neq 0$ $(1 \le A \le FFFF_{16})$

$1 \le B \le 65535$, $B \neq 0$ $(1 \le B \le FFFF_{16})$

7. Waveform Measurement Mode—This mode measures the high and low times of an external waveform at INB (with ENB = 1). Counter A counts the pulse width high and counter B counts the pulse width low. On the high to low transition counter A is transferred to register A and then cleared. On the low to high transition counter B is transferred to register B and then cleared. The counters, therefore, count down from zero. Therefore the value read from the registers is a two's complement value. The transfer from the counter to register is inhibited during a read instruction.

The outputs OA and OB toggle each time the respective counter counts through zero.

The minimum pulse width, either high or low, that can be measured, is the period of the internal frequency. The maximum pulse width that can be measured is the maximum count (65535) multiplied by the period of the internal frequency.



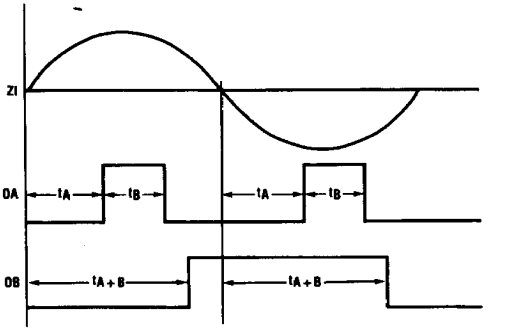
TL/DD/6155–21

$65535t \ge t_A \ge t$

$65535t \ge t_B \ge t$

Where: t = period of internal clock

8. Triggered Pulse Mode—This mode outputs a pulse triggered by the zero crossing of a signal at ZI. The delay from the zero crossing is specified by the contents of register A. The pulse width is specified by the contents of register B. Input INB is ignored. See applications section for further information.



TL/DD/6155–22

$t_A = (A + 1.5)t$

$t_B = Bt$

$t_{A+B} = (A + B + 1.5)t$

Where: A = Contents of register A

B = Contents of register B

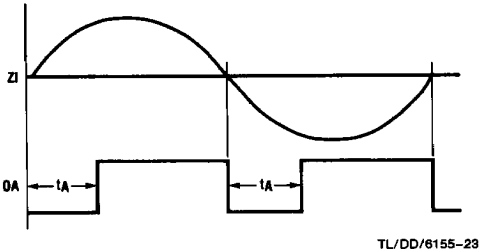
t = period of internal clock (as previously defined)

$0 \le A \le 65535$ $(0 \le A \le FFFF_{16})$

$1 \le B \le 65535$, $B \neq 0$ $(1 \le B \le FFFF_{16})$

9. Triggered Pulse and Count Mode—This mode outputs a pulse at OA triggered by the zero crossing of a signal at ZI. The contents of register A specify the delay from the zero crossing. The pulse remains high until the next zero crossing of the signal at ZI.

Independently of the zero detection, counter B counts external events at INB (when ENB = 1). The conditions on the counter as described previously apply here.



TL/DD/6155–23

$t_A = (A + 1.5)t$

Where: A = Contents of register A

t = period of internal clock (as previously defined)

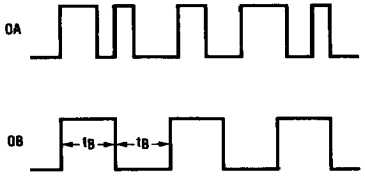
$0 \le A \le 65535$ $(0 \le A \le FFFF_{16})$

OB toggles each time counter B counts through 0

6

Functional Description (Continued)

10. White Noise and Frequency Mode—Register A is converted to a 17-stage shift register generator for the generation of pseudo-random noise at output OA. OB outputs a square wave whose period is specified by the contents of register B. The shift register generator is shifted at the internal frequency (= CKI frequency or ¼ CKI frequency depending on the oscillator divider). See the applications section for more information on the white noise generator.



TL/DD/6155-24

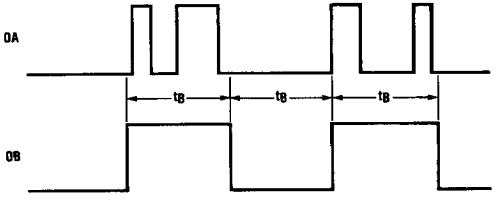
$t_B = (B + 1)t$

Where: B = Contents of register B

t = period of internal clock (as previously defined)

$0 \le B \le 65535 \quad (0 \le B \le FFFF_{16})$

11. Gated White Noise Mode—This mode generates pseudo-random noise ANDed with a square wave. OA outputs this combined signal. OB outputs a square wave frequency. Register A is converted into a 17-stage shift register generator which is shifted at the internal frequency rate. Counter A is not used. Counter B and register B are used in the frequency generation. See the applications section for further information on the white noise generation.



TL/DD/6155-25

$t_B = (B + 1)t$

Where: B = Contents of register B

t = period of internal clock (as previously defined)

$0 \le B \le 65535 \quad (0 \le B \le FFFF_{16})$

GENERAL NOTES

The master timing reference in the COP452L is the internal frequency. This is the CKI frequency after it has passed through the divider. This frequency must remain within its specified limits. The maximum count rate at either input is this frequency divided by 2. The minimum pulse width that can be measured is the period of this frequency.

$\overline{CS}$, other than removing DO from the TRI-STATE condition and allowing data to come into the I register via DI, does not affect the operation of the device. $\overline{CS}$ must go high between accesses in order to clear the I register. Since the I register is cleared when $\overline{CS}$ goes high, the user must insure that $\overline{CS}$ does not go high before the COP452L has accepted the information in the I register. See the software interface section for further explanation on this point. CS does not affect the mode latches.

In those modes where there is an automatic transfer from the register to the counter (frequency generation, duty cycle, number of pulses, triggered pulse), care must be exercised when reading or writing the register. To insure proper, "glitch-free" operation, one of the two procedures below must be followed:

1. Place the COP452L in the RESET mode.
2. Read or write the appropriate register.
3. Place the COP452L back in the original mode.

Alternatively:

1. Read or write the appropriate register.
2. Send the instruction to copy the appropriate register to its counter.

WARNING: Failure to observe one or the other of these procedures can cause some faulty output conditions.

The COP452L powers up in the RESET mode and with oscillator divide by 4. If the CKI input frequency is less than 4 times the minimum internal clock frequency the user *must* set the oscillator divider to divide by 1 *before* attempting any operation with the COP452L. The instruction setting the oscillator divider will be accepted regardless of the value of the internal clock frequency.

Caution: *Failure to observe this requirement will result in the improper operation of the COP452L.*

Applications Information

ZERO CROSS

The ZI input normally requires a resistor and diode external to the device as indicated in *Figure 9a*. The resistor is part of a voltage divider used to ensure that the voltage at pin ZI does not exceed 10V peak and to protect the diode which is required to clamp the negative voltage swing at the input to less than −0.8V. *Figure 9b* is the recommended input circuit if logic level pulses are input to ZI for counting.

As indicated above, the input voltage at ZI must not exceed 10V peak. For inputs less than 10V peak, the resistor in *Figure 9a* is required only to protect the diode. Otherwise, the resistor should be selected to guarantee that the voltage at pin ZI does not exceed 10V peak. *Figure 10* shows this resistor (R_S) and the impedance (R_{IN}) which forms the first part of the input circuit at ZI. The absolute value of R_{IN} can vary widely with process variation. The user should compute the divider with R_S and the worst case maximum of R_{IN} so that the voltage at pin ZI is 10V or less. The following relationship should be used when the input voltage is greater than 10V peak:

$$\frac{R_{IN(MAX.)}}{R_S + R_{IN(MAX.)}} \times V_{IN} \le 10V \text{ peak}$$

Substituting the maximum value for R_{IN} and solving for R_S gives:

$$R_S \le \frac{V_{IN}}{10} \times 7.8k - 7.8k$$

where: V_{IN} = peak input voltage.

Note that this equation is not valid for V_{IN} less than 10V. In this case, the value of R_S is chosen primarily for protection of the diode and not to divide the voltage down to acceptable values.

Applications Information (Continued)

ZERO CROSS OFFSET

As the electrical characteristics indicate, the ZI input has a worst case offset of 150 mV in the zero crossing detection. Therefore, the output of the zero cross detection circuit will change state within ±150 mV of zero volts. There are no directional characteristics to this, i.e., approaching zero from the positive or negative direction has no effect on where the output of the zero cross detection circuit will change state (see *Figure 4*). The offset further indicates that the voltage at pin ZI must exceed 150 mV peak in order to guarantee that the zero crossings will be detected and the appropriate signals generated.

TRIGGERED PULSE MODES

The delays from the zero crossing in the triggered pulse modes are measured from the point where the output of the zero crossing detection circuit changes state—the trip point of this circuit. As stated before, the delay time from this trip point is:

$$T = (A + 1.5)t$$

where: T = delay time from trip point

A = contents of register A

t = period of internal clock

The delay from the true zero crossing of the input waveform has other parameters that must be considered. The equation is of the form:

$$T = (A + 1.5)t \pm |X_1| + X_2 + X_3$$

where: T, A, t are as defined previously

X_1 = time for input waveform to reach the trip point of the zero cross detection circuit

X_2 = propagation delay through the zero cross detection circuit

X_3 = input synchronization delay

Parameter X_1 is dependent on the peak voltage at pin ZI and on the frequency of the input signal. The peak voltage at ZI is in turn dependent on the R_S–R_{IN} voltage divider and the input voltage. The X_1 time is added or subtracted because the trip point of the zero cross detection circuit may be either above or below zero. In the worst case, the trip point is the maximum offset of 150 mV. For a sine wave signal, X_1 is determined as follows:

$$V_{OFFSET} = V_p \sin[2\pi f(X_1)]$$

$$X_1 = \frac{1}{2\pi f} \arcsin \frac{V_{OFFSET}}{V_P}$$

and

$$V_P = V_{IN} \frac{R_{IN}}{R_S + R_{ON}}$$

substituting we have

$$X_1 = \frac{1}{2\pi f} \arcsin \left(V_{OFFSET} \frac{R_S + R_{IN}}{V_{IN} R_{IN}} \right)$$

where: V_{OFFSET} = zero crossing offset or trip point

V_P = peak input voltage at pin ZI

f = frequency of input signal

R_{IN} = internal impedance to ground at pin ZI

R_S = external series resistance at ZI

Both V_{OFFSET} and R_{IN} vary from device to device. It is clear from the equation above that the maximum value of $|X_1|$ is obtained when V_{OFFSET} is at its maximum of 150 mV and R_{IN} is at its minimum of 2.6 kΩ. The minimum value of $|X_1|$ is obtained if V_{OFFSET} is 0. Using this information, the following range of $|X_1|$ is obtained:

$$0 \le |X_1| \le \frac{1}{2\pi f} \arcsin 0.15 \frac{R_S + 2.6k}{V_{IN} \times 2.6k}$$

Parameter X_2 is the propagation delay through the zero crossing detection circuit and its range is given by:

$$0.3\ \mu s \le X_2 \le 0.6\ \mu s$$

Parameter X_3 is the internal synchronization delay and is dependent upon when the zero crossing occurs relative to the internal timing which reads the output of the zero crossing detection circuit. The range for X_3 is:

$$0 \le X_3 \le \frac{t}{2}$$

where: t = period of internal clock

With the preceding information, minimum and maximum values of the delay from true zero can be derived by simply substituting into the original equation.

$$T_{MIN} = (A+1.5)t - \frac{1}{2\pi f} \arcsin \left(0.15 \frac{R_S + 2.6k}{V_{IN} \times 2.6k} \right) + 0.3\ \mu s$$

$$T_{MAX} = (A+1.50)t + \frac{1}{2\pi f} \arcsin \left(0.15 \frac{R_S + 2.6k}{V_{IN} \times 2.6k} \right) + 0.6\ \mu s + \frac{t}{2}$$

The preceding information should enable the user to determine more closely the actual delay from zero of output OA of the COP452L. This analysis applies to both of the triggered pulse modes. The three parameters, X_1, X_2, X_3, also apply in the same way in the triggered pulse and count mode when OA returns to 0 since it is the zero cross detection circuit that causes the output to return to zero in that mode.

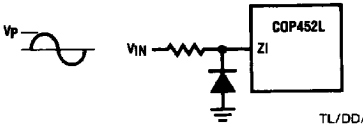


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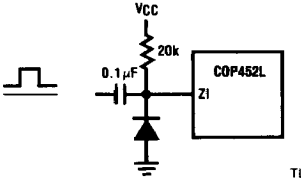
FIGURE 9a



TL/DD/6155-27

FIGURE 9b

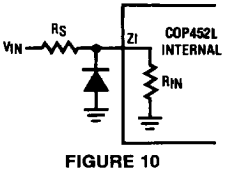


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FIGURE 10

Applications Information (Continued)

TRIGGERED PULSE MODES: INTERVENING ZERO CROSSINGS

In the triggered pulse modes, it is possible to specify a delay from the zero crossing which will extend beyond the next zero crossing. In the triggered pulse and count mode, the intervening zero crossing is ignored and therefore lost. The device will still continue to operate properly. The situation is somewhat different in the "pure" triggered pulse mode where both a delay and a pulse width are specified. Any zero crossing which occurs during the programmed delay time is ignored and therefore lost. However, if the delay time is counted out and the zero crossing occurs during the pulse width high time, the zero crossing will be recognized and the delay time will start counting again while the pulse width high time is being counted. This can result in a variety of possible conditions at the output—ranging from the apparent loss of that zero crossing to an effective very short delay from the zero crossing. What will occur depends on the values of the two counters and on their relationship to the times between zero crossings. Some interesting output waveforms can be produced, but their utility is questionable. Therefore, the user should exercise extreme caution in this mode and make sure that the times are such that all zero crossings occur at the "right" times. Otherwise, the user must be prepared to accept the bizarre effects that this situation can produce.

COUNT MODES

As stated before, the counters are 16-bit down counters. Preloading them when they are enabled as external event counters with ones or zeroes will give the one's or two's complement of the count. To read the counters it is necessary to first copy the counter to its respective register and then read the register.

The user can utilize the fact that the outputs toggle when the counter counts through zero. The counter can be preloaded with a value that represents the number of events the user wishes to count. When the output corresponding to that counter toggles, the specified number of events have occurred. Thus, the user can know that the required number of events have occurred without having to actually read the counter.

The counters require a pulse width greater than or equal to the period of the internal frequency in order to be reliably decremented. It is possible for a narrower pulse to decrement the counter, but it is not guaranteed. A narrower pulse will decrement the counter if it appears at the count input at the right time relative to the internal timing of the device. Since the user does not have access to this internal timing, it is impossible for him to synchronize the count input to this timing and effectively reduce the required width of the count pulse. Therefore, applying pulses at the count input of less than one period of the internal frequency in width may cause erratic counting in the sense that some of the pulses may be recognized and some may not be recognized. Reliable counting is assured only if the width of the count pulse is greater than or equal to one period of the internal frequency.

The counters decrement on a low-going pulse at the input. As stated above, the pulse must remain low at least one internal frequency period to give reliable counting. Similarly, the count signal must go high and remain high at least one internal frequency period before it goes low again. However, the count signal does *not* have to be symmetrical.

COP452L OSCILLATOR

The COP452L will operate over a wide range of oscillator input frequencies. The input frequency may be supplied from an external source or CKI and CKO can be used with a crystal or resonator to generate the oscillator frequency. *Figure 11* indicates some crystal networks for some typical crystal values.

RC and LC networks can also be connected between CKI and CKO to produce the oscillation frequency. *Figure 12* indicates some examples of such networks. *Figure 12a* is the recommended RC network for use in this manner. With C_1 = 0.005 μF, R = 1.5 kΩ, and C_2 between 20 pF and 400 pF oscillation frequencies between about 1 MHz and 2 MHz should be obtainable. The oscillation frequency decreases with increasing values of C_2. The user should feel free to experiment with the R and C values, and with the network configuration, to produce the oscillation frequency desired.

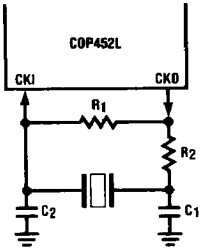
Figures 12b and *12c* indicate LC networks that can be used to produce the COP452L oscillation frequency. In *Figure 12b*, with L = 100 μH and C = 100 pF, a frequency of about 2 MHz should be produced. In *Figure 12c*, with L = 56 μH, C_2 = 27 pF, and C_1 between 33 pF and 0.01 μF, frequencies between about 1.5 MHz and 2 MHz can be produced.

There is, in effect, an inverter between CKI and CKO. This inverter was designed for use with a crystal and its associated network. It was not designed for use with the RC and LC networks previously described. However, these networks will work and are usable. The user should be prepared to experiment with the networks to determine component values, stability, oscillation frequency, etc. These networks should be viewed as the starting point for a user who wishes to use networks of this type to generate the COP452L oscillation frequency.

The RC networks provide an inexpensive way to generate the oscillation frequency. It is foolish, however, to expect any significant degree of frequency stability or accuracy over temperature and voltage with a simple RC network—especially if inexpensive, uncompensated components are used. LC and RLC networks can produce very stable and accurate frequencies. Regardless of the network used, the user must consider the variation of the external components in his design if accuracy and stability are important considerations in his application.

The crystal networks of *Figure 11* provide frequency stability and accuracy and are easy to use. If the application requires oscillation frequency accuracy and stability the crystal networks are recommended as the best solution.

Applications Information (Continued)



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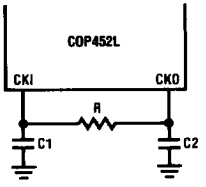
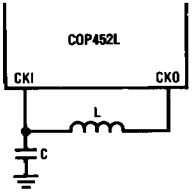
Crystal Value	Component Values			
	R_1	R_2	C_1	C_2
455 kHz	1M	16k	80 pF	80 pF
32 kHz	1M	220k	6 pF–36 pF	30 pF

FIGURE 11. COP452 Crystal Oscillator



TL/DD/6155-31



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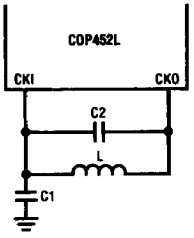

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a. b. c.

FIGURE 12. RC and LC Networks to Produce COP452 Oscillator Frequency

WHITE NOISE GENERATION MODES

In the two white noise modes register A is converted into a 17-stage shift register, or polynomial, generator. With feedback taps at stages 17 and 14, as indicated in *Figure 13*, a maximal length sequence is generated. With these feedback taps the characteristic polynomial of the sequence is:

$$X^{17} + X^3 + 1.$$

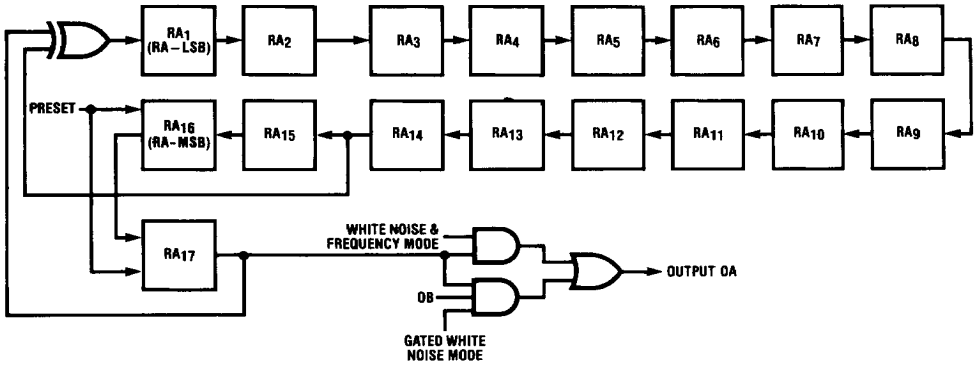
The output of this generator is a pseudo-random sequence. Since the register is shifted at the internal frequency rate, the sequence repeats after a period equal to $(2^{17} - 1)t$, where t is the period of the internal frequency.

The first 16 stages of the shift register are the 16 bits of register A that the user may read or write. Entering either white noise mode presets the 16th stage to a 1 and connects the 17th stage to the shift register. If the user wishes, he can write register A and then enter the white noise and frequency mode. The output at OA will then be "1", and the lower 15 bits of the data user had written to register A. Following that, the polynomial sequence dictates the output. This injection of a 1 into the 16th stage prevents the lockup condition that occurs if all the stages are 0.

WARNING: To insure proper operation, the white noise must be entered from the Reset mode. The COP452 must be in the Reset mode before the desired white noise mode and there may be no intervening modes between Reset and the desired white noise mode. (The state of 17th stage is don't care (unknown).)

6

Applications Information (Continued)



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Note: Setting the Register A to all 1's will result in a predictable pattern each time this mode is activated.

FIGURE 13. COP452L White Noise Generator

INTERFACE TO COPS MICROCONTROLLERS

Figure 14 indicates the typical interface between the COP452L and a COPS microcontroller. As is obvious from the figure, the interface is the standard MICROWIRE. G_2 is indicated as the chip select line because it is available on all COPS microcontrollers. Obviously, any convenient output of the microcontroller may be used as the chip select for the COP452L.

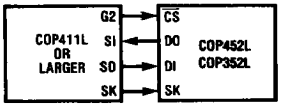

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FIGURE 14

The $\overline{CS}$ pin of the COP452L must be toggled between successive communications with the device. The internal I register (instruction register) is held reset (all zero) when $\overline{CS}$ is high. Since this is the only way in which the I register is cleared, failure to take $\overline{CS}$ high between accesses will result in improper operation.

The COP452L contains an internal power-on reset circuit which sets the mode latches to one, i.e., places the COP452L in the RESET mode, and sets the oscillator divider to divide by 4. The counters and registers are not affected by this reset circuit and are therefore undefined at power up.

INTERFACE SOFTWARE FOR THE COP452L

Sample software for interfacing COPS microcontrollers to the COP452L is given below. The code is completely general and will work in any COPS microcontroller. The following assumptions are made:

1. Pin G_2 is used as the chip select for the COP452L (because G_2 is available on all COPS microcontrollers).
2. G_2 is assumed high on entry to the routines.
3. The SK clock is off (0) on entry to the routines.
4. Register 0 of the microcontroller is arbitrarily chosen as the I/O register.
5. The leading digit sent out is of the form 001X where 1 is a start bit; X is 1 or 0, depending on the operation.
6. The next lower digit contains the remaining 4 bits of the command.
7. If data is being sent, it is in the next 16 bits of information sent.
8. Location GSTATE chosen as RAM address 0,15.
9. SK frequency is less than or equal to the internal frequency.

Since the COP452L is an I/O device, the code takes precautions to insure that SO is 0 prior to enabling the SK clock. (This is a wise precaution to take in any system with I/O peripherals on the serial port.)

Two versions of the WRITE routine are provided. The destructive WRITE routine destroys the information in the microcontroller as the data is being sent out to the COP452L. The nondestructive WRITE routine preserves the data in the microcontroller as that data is being sent out to the COP452L. The destructive routine is a little more code efficient than the nondestructive routine.

Applications Information (Continued)

```
WRCMND:   CLRA                ; SET UP POINTER FOR COMMAND ONLY WRITE
          AISC    1
          JP      WRITE
WRDATA:   CLRA                ; SET UP POINTER FOR COMMAND AND DATA WRITE
          AISC    5
WRITE:    LBI     GSTATE      ; GSTATE = LOCATION 0,15
          RMB     2
          OMG                 ; SEND COP452L CHIP SELECT LOW
          CAB                 ; POINT TO PROPER LOCATION FOR OUTPUT
          LEI     8           ; ENABLE SHIFT REGISTER MODE
          RC                  ; JUST TO INSURE SO = 0 BEFORE CLOCK ON
          CLRA
          XAS                 ; THESE 3 WORDS FOR SAFETY ONLY
          SC                  ; SO SK WILL TURN ON AT NEXT XAS
SEND:     LD
          XAS
          XDS
          JP      SEND
FINISH:   RC                  ; ALL DONE, SK OFF, DESELECT COP452L, AND SET
          XAS                 ; SO TO ZERO
DONE:     LBI     GSTATE
          SMB     2
          OMG
          LEI     0
          RET
;
CODE TO WRITE COP452L — DATA DESTROYED IN MICROCONTROLLER
```

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Applications Information (Continued)

The code below is the code to read COP452L. It is written so that the command to the COP452L is sent out nondestructively, i.e., the data in the microcontroller is preserved. A routine which sends out the data destructively could be easily generated but is not shown here. The user is referred to the techniques in the WRITE routines to determine how to modify this READ routine to send the command out destructively.

```
READ:     CLRA              ; READ INSTRUCTION IN 0, 1 AND 0, 0 AND IS
          AISC   1          ; OF THE FORM 00100010 OR 00100011 IF READ
          LBI    GSTATE     ; RA OR RB
          RMB    2
          OMG               ; SELECT THE COP452L
          CAB
          SC
          CLRA              ; SO THAT ZEROES GO OUT FIRST
          LEI    8
SEND2:    XAS
          LD
          XDS
          JP     SEND2      ; NONDESTRUCTIVE SENDING OF READ INSTRUCTION
          XAS
          CLRA              ; SET UP TO READ
          AISC   2
          CAB
          NOP               ; NOW WAIT FOR THE DATA
          NOP
          NOP
RDLOOP:   CLRA
          XAS
          XDS
          JP     RDLOOP
          RC                ; TURN OFF THE CLOCK
          XAS               ; READ LAST 4 BITS
          JP     DONE       ; COMMON EXIT WITH WRITE ROUTINE
                            ; EXITS WITH DATA IN LOWER 3 DIGITS OF RO
                            ; AND IN THE ACCUMULATOR

SAMPLE CODE TO READ THE COP452L

WRCMND:   CLRA              ; SET UP POINTER FOR COMMAND ONLY WRITE
          AISC   1
          JP     WRITE
WRDATA:   CLRA              ; SET UP POINTER FOR COMMAND AND DATA WRITE
          AISC   5
WRITE:    LBI    GSTATE
          RMB    2
          OMG                ; SELECT THE COP452L — G2 LOW
          CAB                ; LOAD THE POINTER
          RC
          CLRA
          LEI    8           ; ENABLE SHIFT REGISTER MODE
          XAS                ; SEND OUT ZEROES
          SC
          CLRA
SEND:     XAS                ; FIRST TIME THROUGH, TURNS ON CLOCK
          LD                 ; THEN SENDS DATA
          XDS
          JP     SEND
          XAS                ; SEND LAST 4 BITS
          CLRA
          NOP
FINISH:   RC
          XAS                ; ALL DONE, SK OFF
DONE:     LBI    GSTATE
          SMB    2           ; DESELECT THE COP452
          OMG
          LEI    0           ; SEND SO LOW
          RET

CODE TO WRITE COP452L — DATA PRESERVED IN MICROCONTROLLER
```

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Applications Information (Continued)

The software interface routines provided above are general purpose routines written to work in the general case for all COPS microcontrollers. They are written as subroutines to be called by the main program. There is no question that other routines can be written to perform the required function. It is also clear that these routines can be reduced in specific applications. These routines should be viewed as providing a framework from which the user can develop routines which are optimal to a specific application.

Assumption 9 mentioned prior to the code itself presents an important requirement for the interface software. There must be a time delay greater than 3 periods of the internal frequency between the time the SK clock is turned off and the time the COP452L is deselected. This is required because the COP452L reads the instruction register with timing based on its internal frequency. When the microcontroller deselects the COP452L, CS goes high and the instruction register is automatically cleared. Therefore, depending on the relative speeds of SK and the internal frequency, it is possible that the instruction register may be cleared before the COP452L has accepted the information. The sample code provided automatically satisfies the requirement mentioned above whenever the SK frequency is less than or equal to the counter clock frequency. When SK is faster than the internal frequency, some delay may be required between the time SK is turned off and the time the COP452L is deselected. The time delay is not required when reading or writing the COP452L registers or when changing the oscillator divider.

Caution: *Failure to observe this time delay will result in improper operation of the COP452L.*

APPLICATION # 1—GENERATION OF MULTIPLE TONES

The COP452L makes the generation of two independent frequencies a simple task. This application indicates how to generate frequencies with the COP452L and also indicates other aspects of control of the device.

The requirement is to generate the following two DTMF frequencies:

$$f1 = 941\ Hz$$

$$f2 = 1336\ Hz$$

We will select the CKI frequency of the COP452L as 525 kHz. Therefore, in divide by 1 mode, the internal frequency is 525 kHz. Since the registers in the COP452L are loaded with a number related to the period of the frequency, we need the periods of f1 and f2.

$$\frac{1}{f1} = t1 = 1062.7\ \mu s;\quad \frac{t1}{2} = 531.35\ \mu s$$

$$\frac{1}{f2} = t2 = 748.5\ \mu s;\quad \frac{t2}{2} = 374.25\ \mu s$$

As stated earlier, the period of an output frequency in the COP452L in the frequency generation mode is given by:

$$T = 2(N + 1)t$$

where: t = period of internal clock

N = register value

Solving for N, the equation becomes:

$$N = \frac{T}{2t} - 1$$

With the internal frequency at 1 MHz, the value of t is 1 μs. Therefore, the N values with which the registers must be loaded to generate the frequencies specified above are 278 (116 hex) and 195 (0C3 hex). Note that the fractional parts of the numbers are lost since the COP452L cannot be loaded with fractional numbers. Note that the fractionial parts may be reduced or eliminated by judicious choice of the CKI frequency. With the numbers here, the COP452L will generate a frequency with a period of 1062 μs (941.62 Hz) and a frequency with a period of 748 μs (1336.9 Hz). Note that these values are accurate to within 0.7% of the desired output frequencies.

Figure 15 indicates a connection diagram for this application. The software to accomplish this task is indicated below. The software indicates several aspects of the usage of the COP452L. The code first resets the COP452L, then loads the registers with the proper values, transfers the registers to the counters, puts the COP452L in the CKI divide by 1 state, and then loads the dual frequency mode. The output frequency generation begins when the dual frequency mode is loaded. The code as written is independent of the COP microcontroller used. The code uses the WRITE routines as described in the software interface section and assumes that these routines are located in the subroutine page.

```
            . PAGE      0
GSTATE      =           0, 15
POWUP:      CLRA
            XAS                     ; TURN OFF SK CLOCK (C = 0 AT POWER UP)
            LBI         GSTATE
            STII        15
            LBI         GSTATE
            OMG                     ; MAKE SURE COP452 IS DESELECTED
            LBI         0, 0
            JSRP        CLEAR       ; CLEAR REGISTER 0
            LBI         0, 0        ; NOW SET UP TO SEND RESET MODE TO COP452
            STII        15
            STII        3           ; RESET COMMAND AND START BIT
            JSRP        WRCMND
```

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Applications Information (Continued)

```
; THE COP452L IS NOW RESET, NOW SET UP TO WRITE REGISTER A TO
; GENERATE OUTPUT FREQUENCY OF 941 HZ AT OA

                LBI     0, 0
                STII    6               ; 116  HEX  =  278, GIVE PERIOD OF 1062 µs
                STII    1
                STII    1
                STII    0
                STII    1
                STII    2               ; START BIT PLUS CODE TO WRITE RA
                JSRP    WRDATA
; REGISTER A IS NOW LOADED. NEXT TRANSFER REGISTER A TO COUNTER A
                LBI     0, 0
                STII    5
                STII    2               ; INSTRUCTION TO TRANSFER PLUS START BIT
                JSRP    WRCMND
; ALL DONE WITH REGISTER AND COUNTER A, NEXT WORK ON REGISTER B
                LBI     0, 0
                STII    3               ; WRITE REGISTER B WITH 0C3 HEX (195)
                STII    C               ; TO GIVE FREQUENCY OF 1336 HZ
                STII    0
                STII    0
                STII    0               ; INSTRUCTION TO WRITE RB
                STII    2
                JSRP    WRDATA
; REGISTER B IS NOW LOADED. NEXT TRANSFER RB TO CB
                LBI     0, 0
                STII    4               ; INSTRUCTION TO TRANSER RB TO CB
                STII    2
                JSRP    WRCMND
; NOW LOAD CKI DIVIDE BY 1
                LIB     0, 0
                STII    8
                STII    2
                JSRP    WRCMND
; NOW PUT THE COP452 IN DUAL FREQUENCY MODE
                LBI     0, 0
                STII    0
                STII    3
                JSRP    WRCMND
; NOW THE CODE MAY PROCEED TO DO WHATEVER ELSE IS REQUIRED IN
; THE APPLICATION.
; THE SUBROUTINES USED IN THIS APPLICATION ARE CLEAR AND THE
; WRITE ROUTINES. THE ADD ROUTINE IS USED IN THE EXAMPLE BELOW
                . PAGE  2
CLEAR:          CLRA
                XIS
                JP      CLEAR
                RET
ADD:            SC
                LBI     2, 9            ; ROUTINE ADDS 1 TO COUNTER
ADD1:           CLRA
                ASC
                NOP
                XIS
                JP      ADD1
                RET
;
WRCMND:                                 ; SEE SOFTWARE INTERFACE FOR THIS ROUTINE
;
WRDATA:                                 ; SEE SOFTWARE INTERFACE FOR THIS ROUTINE
```

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Applications Information (Continued)

The preceding has done a lot with the COP452L. It is clear that the code can be reduced and specialized. The purpose here was to illustrate the various communications with the device.

An interesting effect can now be produced by making use of the 4 to 1 CKI divider. With the CKI frequency at 525 kHz, the internal frequency is well within the specified limits in either the divide by 1 or divide by 4 condition. Therefore, this characteristic of the device can be used to quickly multiply or divide the output frequency by 4. An interesting siren effect can thus be created. Sample code to do this is given below. This code assumes that the registers have been loaded and that the COP452 is in dual frequency mode. Again, the code is written to be independent of the COPS microcontroller used.

As is obvious from this code, it is a simple matter to create this effect. As was mentioned earlier, the code here is general purpose. This necessarily means that it can be reduced in specific applications. The user should view this code as representative of the techniques involved and then optimize or rewrite the routines to suit his particular application.

```
SIREN:    LBI     2, 9      ; USE REGISTER 2 AS COUNTER FOR DELAY TIME
          JSRP    CLEAR
          LBI     0, 0
          STII    8         ; CKI DIVIDE BY 1
          STII    2
          JSRP    WRCMND
PLUS1:    JSRP    ADD       ; INCREMENT COUNTER FOR DELAY
          SKC
          JP      PLUS1     ; EXIST DELAY LOOP WHEN COUNTER OVERFLOWS
          LBI     0, 0
          STII    9         ; CKI DIVIDE BY 4
          STII    2
          JSRP    WRCMND
          LBI     2,9
          JSRP    CLEAR
PLUS1A:   JSRP    ADD
          SKC               ; AGAIN, TIME OUT VIA THE COUNTER
          JP      PLUS1A
          JP      SIREN     ; DONE, START OVER AGAIN
```

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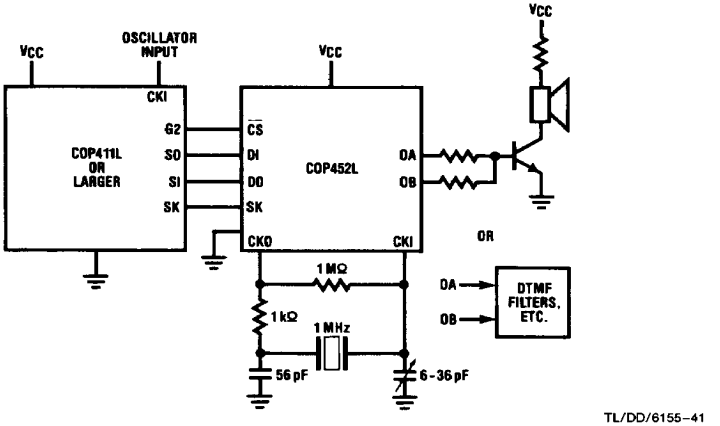

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FIGURE 15. Dual Frequency Application

Applications Information (Continued)

APPLICATION #2

This application makes use of the number of pulses mode of the COP452L to control a stepping motor. The technique is equally applicable in any situation where a number of pulses must be generated based upon the state of the system. *Figure 16* indicates the system interconnect. Since the oscillator frequency is 2.1 MHz max. and the CKO pin of the COP452L is being used to drive the CKI of the microcontroller, a COP420 is specified as the microcontroller. If a separate oscillator were provided, any COPS microcontroller could be used. The software is completely general and will work in any COPS microcontroller.

The application has the following specifications:

1. The pulse width required for the stepping motor is 5 ms ±5%.
2. The system has 4 return lines which indicate 4 possible variations in the number of output pulses required. These four conditions are:
   a. 10 pulses required
   b. 100 pulses required
   c. Repeat the last number of pulses sent
   d. Send one more than the last number of pulses
3. The system has a signal available indicating that the return lines contain valid information.
4. One pulse is required at power up.

A flowchart to implement this system is indicated in *Figure 17*. *Figure 16* is the interconnect used in this application. As the figure indicates, we will use a 2.1 MHz crystal as the time base for the COP452L. With the oscillator divide by 4 selection, this gives an internal frequency period of 1.90476 μs. With this information we can determine the number that needs to be loaded to register A to give a pulse width of 5 ms. From application #1 we have the following equation which is valid here:

$$T = (N + 1)t$$

where: T = pulse width
N = contents of register A
t = period of internal clock

Solving for N we have;

$$N = (T/t) - 1$$
$$= (5\ \text{ms}/1.90476\ \mu\text{s}) - 1$$
$$= 2625 - 1$$
$$= 2624$$

Register A must be loaded with 2624 (0A40 hex) to give a 5 ms pulse. The error created by the truncation of the number is 0.5 μs. There is an error of 0.01%—well within the tolerance limits required.

The code to operate this system is given below. The interconnect of *Figure 16* is assumed. The code uses the READ and WRITE subroutines as given in the software interface section of this data sheet. The code further assumes that those routines are located in the subroutine page.

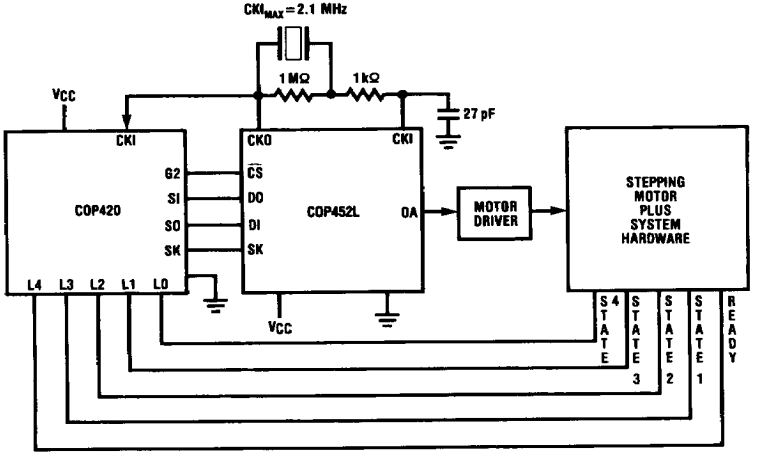

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FIGURE 16. COP452 In Stepping Motor Control

Applications Information (Continued)

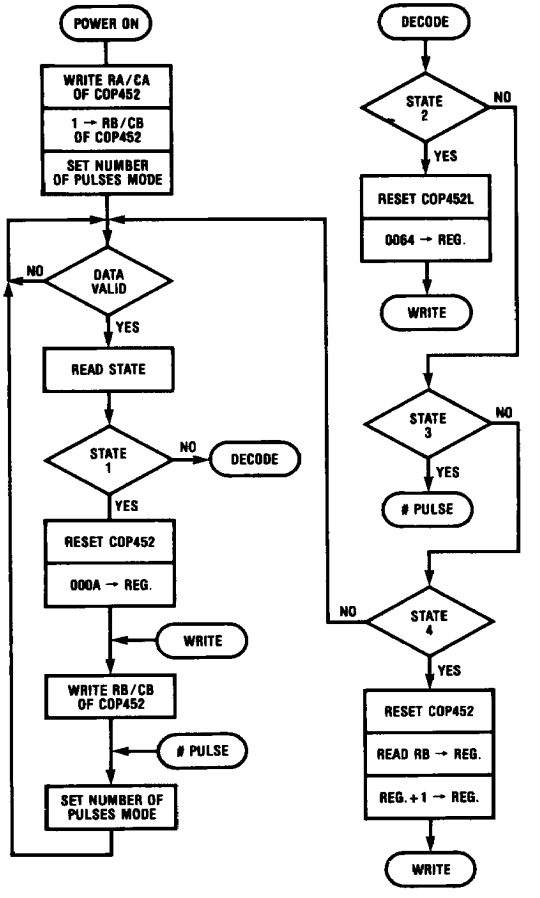

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FIGURE 17. Flow Diagram for Application # 2

```
                .PAGE   0
GSTATE          =       0, 15
POWRON:         CLRA
                XAS                     ; TURN OFF SK CLOCK
                LBI     GSTATE
                STII    15
                LBI     GSTATE
                OMG                     ; DESELECT THE COP452L — G2 HIGH
                LD
                CAMQ                    ; DRIVE THE L LINES HIGH FOR READING
                LEI     4               ; ENABLE THE L OUTPUTS
                LBI     0, 0
                STII    0
                STII    4
                STII    A
                STII    0
                STII    1
                STII    2               ; WRITE RA OF COP452L WITH 0A40 HEX TO GET
                JSRP    WRDATA          ; 5MS PULSE
```

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Applications Information (Continued)

```
                LBI     0, 0
                STII    5           ; TRANSFER RA TO COUNTER A
                STII    2
                JSRP    WRCMND
                LBI     0, 0        ; NOW WRITE RB WITH THE NUMBER OF PULSES
                STII    1
RBWRT:          STII    0           ; ONE PULSE REQUIRED AT POWER UP
RBWRT2:         STII    0
                STII    0
RBWRT3:         STII    0
                STII    2
                JSRP    WRDATA
                LBI     0, 0        ; NOW TRANSFER RB TO COUNTER B
                STII    4
                STII    2
                JSRP    WRCMND
PULSE:          LBI     0, 0
                STII    2           ; SET NUMBER OF PULSES MODE
                STII    3
                JSRP    WRCMND
; AT THIS POINT THE COP452L IS IN NUMBER OF PULSES MODE, ONE
; PULSE IS OUTPUT AT OA. NOW MUST READ THE RETURN LINES, MAKE
; THE APPROPRIATE DETERMINATION OF THE STATE OF THE SYSTEM
; AND UPDATE THE COP452L ACCORDINGLY, ALSO AT THIE POINT, THE
; COP452L IS SET UP TO AGAIN GENERATE A SINGLE PULSE 5 ms WIDE
; IF THE DEVICE IS ACCESSED AGAIN.
;
STATE:          LBI     GSTATE
                LD                  ; CONTENTS OF GSTATE = 15 HERE
                CAMQ                ; MAKE SURE L LINES ARE HIGH AND
                LEI     4           ; ENABLED
                LBI     0, 0
                INL                 ; READ THE L LINES TO A AND M(0, 0)
                SKMBZ   0           ; TEST DATA — RETURN LINES — VALID
                JMP     STATE       ; DATA NOT VALID, WAIT FOR IT TO BE VALID
                AISC    8           ; DATA IS VALID, DECODE A
                JMP     TEST2
STATE1:         STII    15          ; POINTING AT 0, 0
                STII    3           ; RESET THE COP452L FOR STATE 1
                JSRP    WRCMND
                LBI     0, 0        ; NOW SET UP TO SEND 10 PULSES
                STII    10
                JMP     RBWRIT      ; SHARE COMMON CODE
TEST2:          AISC    4
                JMP     TEST3
STATE2:         STII    15          ; IN STATE2, MUST SEND 100 PULSES
                STII    3           ; FIRST RESET THE COP452L
                JSRP    WRCMND
                LBI     0, 0        ; WRITE 100 (0064 HEX) TO RB OF COP452L
                STII    4
                STII    6
                JMP     RBWRT2
TEST3:          AISC    2
                JMP     TEST4
STATE3:         JMP     PULSE       ; STATE 3 MERELY SENDS THE SAME NUMBER OF PULSES AGAIN.
                                    ; THEREFORE, MERELY SEND THE NUMBER OF PULSES MODE COMMAND
                                    ; AGAIN
```

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Applications Information (Continued)

```
TEST4:      AISC    1
            JMP     STATE       ; ALL L LINES WERE 0, JUMP BACK TO MAIN
STATE4:     STII    15          ; RESET THE COP452L
            STII    3
            JSRP    WRCMND
            LBI     0, 0        ; NOW READ THE COP452L
            STII    2
            STII    2           ; COMMAND TO READ RB
            JSRP    READ
            LBI     0, 0        ; MOVE DATA TO LAST 4 DIGITS OF R0
            XIS
            XIS
            XIS
            XIS
            LBI     0, 0        ; NOW INCREMENT THE VALUE BY 1
            SC
PLUS1:      CLRA
            ASC
            NOP
            XIS
            CBA
            AISC    12
            JP      PLUS1
            JMP     RBWRT3      ; HAVE INCREMENTED THE VALUE, SEND IT OUT
;
            . PAGE  2
READ:                           ; SEE SOFTWARE INTERFACE SECTION FOR THESE
WRDATA:                         ; ROUTINES

WRCMND:
```

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These are general routines and can be reduced in specific applications. The application itself was kept general so that it can be easily adapted to particular applications. The user should view this code as the basis from which to work to optimize the code for a specific application.

APPLICATION #3

An application such as a tachometer requires the counting of external pulses that occur within a given time period. The COP452L can be used both to perform the counting and to establish the "viewing window," or time period, during which to count the pulses. By using the frequency and count mode of the COP452L, a frequency can be generated which will establish this viewing time. The other counter can then be used to count the pulses. *Figure 18* provides a diagram of the interconnect in this application.

As *Figure 18* indicates, the oscillator frequency for the COP452L has been selected as 250 kHz. With the oscillator divider set at divide by 1, the internal frequency is also 250 kHz. At this frequency, the minimum pulse width that can be reliably expected to decrement the counter is 4 μs—the period of the internal frequency.

A viewing time of 250 ms is arbitrarily selected. This means that the period of the output frequency is 500 ms—a frequency of 2 Hz. Using the equation developed earlier for determining the counter values we have:

$$N = \frac{T}{2t} - 1$$

$$= (500\ \text{ms}/8\ \mu\text{s}) - 1$$

$$= 62500 - 1$$

$$N = 62499 = \text{F423 hex}$$

Therefore, register A must be loaded with the hex value F423 to generate a frequency of 2 Hz at OA. Counter B will count pulses when OA is high by virtue of the ENB input. When OA is low, the microcontroller will read and reset the counter and peform any necessary operations.

With the values above for the internal frequency and the viewing window, the tachometer range is 240 RPM to 62,500 RPM. By making use of the divide by 1/divide by 4 features of the oscillator divider, the range can be extended down to 60 RPM. The range when the oscillator is divided by 4 is 60 RPM to 15,625 RPM. However, a penalty is paid for this range extension. The viewing window goes from 250 ms to 1 second. The minimum reliable pulse width also increases from 4 μs to 16 μs. The added time spent counting may or may not be acceptable. It can be reduced somewhat by changing the value of RA to give a faster frequency at the reduced counter clock frequency. However, as the OA frequency increases, the low end of the range increases.

A flow chart for this application is provided in *Figure 19*. Sample code is given below. Note that the sample code includes only the COP452L interface and control. Other system requirements, e.g., display interface, arithmetic, etc., are not included here. Other data sheets and application notes provide sufficient information to fill in those details.

The hardware interface indicated in *Figure 18* and the code below, are completely general and valid of any COPS microcontroller. In specific applications both the hardware and software may be optimized to a greater extent than that shown here.

Applications Information (Continued)

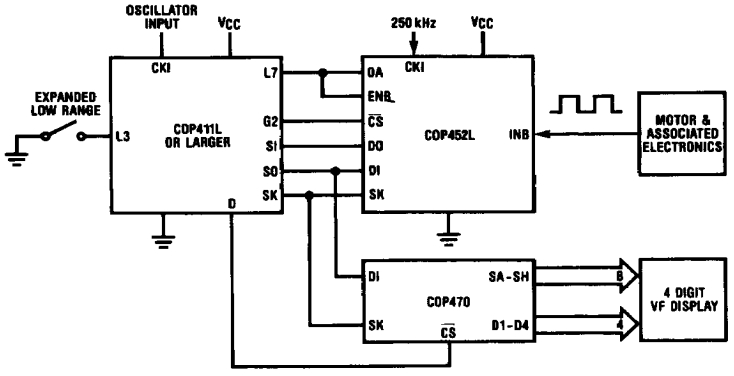

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FIGURE 18. COP452 in Wide Range Tachometer Application

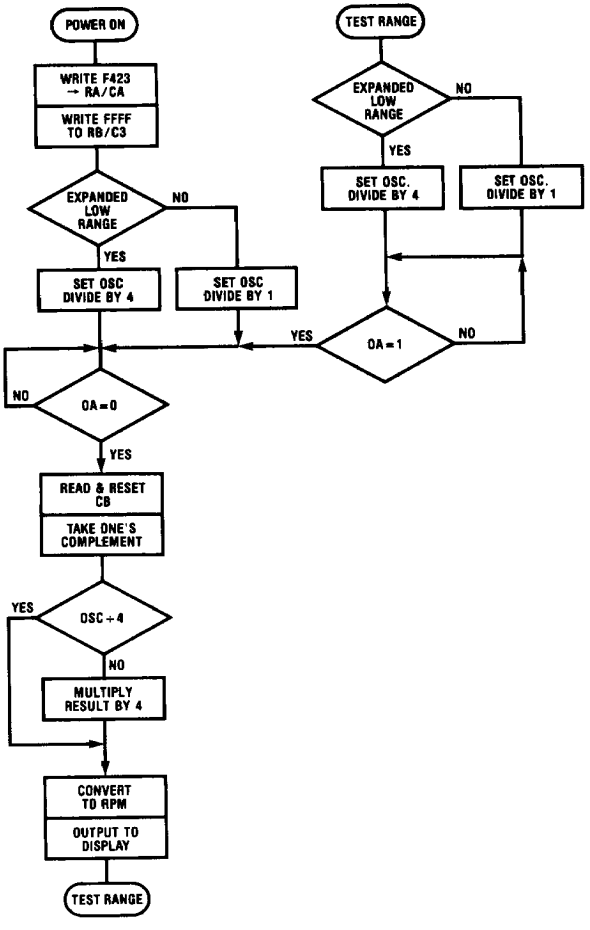

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FIGURE 19. Flowchart for Tachometer Application

Applications Information (Continued)

```
                .PAGE   0
GSTATE          =       0,15
POWRON:         CLRA
                XAS                     ; TURN OFF THE SK CLOCK—C=0 AT POWER UP
                LBI     GSTATE
                OBD                     ; DRIVE D LINES HIGH TO DESELECT DISPLAY
                STII    15
                LBI     GSTATE
                OMG                     ; DESELECT THE COP452L
                LD
                CAMQ                    ; SET THE Q REGISTER TO ALL 1'S FOR INPUT
                LBI     0,0
                STII    3               ; NOW SET UP TO WRITE RA OF COP452L
                STII    2
                STII    4
                STII    15              ; WRITE RA WITH F423 HEX
                STII    1                                                  TL/DD/6155-49
                STII    2               ; REMEMBER COP452L IS RESET AT POWER UP
                JSRP    WRDATA
                LBI     0,0
                STII    5               ; TRANSFER RA TO CA
                STII    2
                JSRP    WRCMND
                JSR     RSTRB           ; RESET RB AND COUNTER B WITH FFFF
                JSR     RANGE           ; TEST RANGE AND SET OSCILLATOR DIVIDER
                LEI     4               ; ENABLE Q TO L—DRIVE L LINES HIGH
                LBI     0,0             ; LOOK FOR OA=0
TSTOA0:         INL
                SKMBZ   3
                JP      TSTOA0
                LBI     0,0             ; OA IS 0, READ COUNTER
                STII    6               ; FIRST TRANSFER CB TO RB
                STII    2
                JSRP    WRCMND
                LBI     0,0             ; THEN READ RB
                STII    2
                STII    2
                JSRP    READ
                LBI     0,0             ; NOW TAKE THE 1'S COMPLEMENT
ONECMP:         COMP
                XIS
                COMP
                XIS
                COMP
                XIS
                COMP
                X
                LBI     0,0             ; NOW SAVE VALUE IN R1
XFER1:          LD      1
                XIS     1
                JP      XFER1
                JSR     RSTRB           ; RESET RB AND CB WITH FFFF FOR NEXT TIME
;
; AT THIS POINT INSERT THE APPROPRIATE CODE FOR ANY NECESSARY
; ARITHMETIC, BINARY/BCD CONVERSION, DISPLAY OUTPUT, AND ANY OTHER
; SYSTEM REQUIREMENTS. AFTER THESE ARE COMPLETE, JUMP TO LABEL
; TSTRNG WHICH HAS BEEN ARBITRARILY PLACED IN PAGE 4.
.PAGE           2
WRDATA:

WRCMND:                         ; SEE SOFTWARE INTERFACE SECTION FOR THESE
                                ; THREE ROUTINES
READ:
                .PAGE   4
TSTRNG:         JSR     RANGE   ; CHECK THE RANGE
                LEI     4       ; BE SURE Q IS ENABLED TO L
                LBI     0,0     ; LOOK FOR OA=1
TSTOA1:         INL
                SKMBZ   3
                JMP     TSTOA0
                JP      TSTOA1
;
; THE SUBROUTINES RANGE AND RSTRB ARE INSERTED HERE
;
RANGE:          LEI     4               ; MAKE SURE L ENABLED
                LBI     3,15            ; WILL SAVE RANGE STATUS IN 3,15
                INL
                X
                CLRA                    ; NOW PREPARE TO SET OSCILLATOR DIVIDER
                                                                   TL/DD/6155-50
```

Applications Information (Continued)

```
                AISC    8           ; AN 8 MEANS DIVIDE BY 1
                SKMBZ   3
                JP      HILOW
LOW:            AISC    1           ; IF DIVIDE BY 4, WANT A 9 IN A
HILOW:          LBI     0, 0
                XIS
                STII    2
                JMP     WRCMND
;
; THE FOLLOWING SUBROUTINE USES A SUBROUTINE LEVEL. IT RESETS BOTH
; REGISTER B AND COUNTER B OF THE COP452L TO FFFF
;
RSTRB:          LBI     0, 0
                STII    15
                STII    15
                STII    15
                STII    15
                STII    0
                STII    2
                JSRP    WRDATA      ; WRITE FFFF TO RB
                LBI     0, 0
                STII    4           ; TRANSFER RB TO CB
                STII    2
                JMP     WRCMND
```

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APPLICATION #4

The triggered pulse mode of the COP452L provides the capability of generating the appropriate signals for triac control. *Figure 20* is a general diagram of such an application.

Assume the requirement is to switch on the triac 45 degrees into the waveform. With a 60 Hz sine wave signal, the 45 degree delay is 2.0833 ms from the zero crossing. Assume also that the triac requires a gate pulse width of 150 μs. As the diagram indicates, a 2.097 MHz crystal provides the oscillator input to the COP452L. With the above information the two values that must be loaded in the COP452L can be determined. With CKI at 2.097 MHz and the oscillator divider at divide by 4, the period of the internal frequency is 1.9075 μs. From the description of the triggered pulse mode, the pulse width is given by:

$$T = Bt$$

where: T = desired pulse width

B = contents of register B

t = period of internal clock

Solving for B is trivial and gives:

$$B = T/t$$
$$= 150\ \mu s/1.9075\ \mu s$$
$$= 78.64$$

Since the register and counter can be loaded with whole numbers only, register B and counter B must be initialized with 79 (002F hex) to give a pulse width of 150 μs.

The delay from the zero cross trip point is given by:

$$T = (A + 1.5)t$$

where: T = delay from zero cross trip point

A = contents of register A

t = period of internal clock

Solving for A we have:

$$A = (T/t) - 1.5$$
$$= (2.0833\ ms/1.9075\ \mu s) - 1.5$$
$$A = 1090.66 \text{ rounded up to } 1091$$

Therefore register A and counter A must be initialized with 1091 (0443 hex) to delay 2.0833 ms (45 degrees at 60 Hz) from zero cross.

Once the data has been given to the COP452L and the device placed in the triggered pulse mode, no further attention is required. The COP452L will generate the pulses with the appropriate delay as long as the power is applied and the input sine wave is available. It is a trivial matter to change any of the information. Merely write the appropriate register/counter pair. Thus very easy control is available over the firing angle of triacs.

Sample code to accomplish this function is given below. The code is general purpose and is written to work in any COPS microcontroller.

Applications Information (Continued)

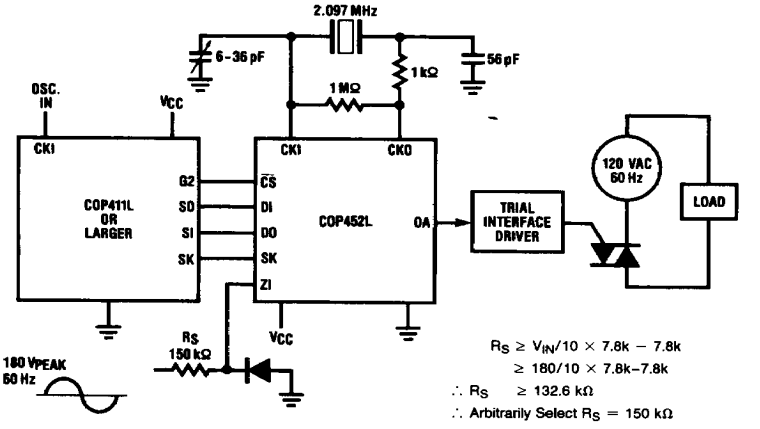

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FIGURE 20. COP452L as Triac Controller

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            . PAGE    0
GSTATE      =         0, 15
POWRON:     CLRA
            XAS                   ; TURN OFF THE SK CLOCK
            LBI       GSTATE
            STII      15
            LBI       GSTATE
            OMG                   ; DESELECT THE COP452L — G2 HIGH
            LBI       0, 0        ; NOW WRITE RB/CB WITH 002F HEX TO GIVE
            STII      15          ; 150 μs PULSE WIDTH
            STII      2
            STII      0
            STII      0
            STII      0
            STII      2
            JSRP      WRDATA
            LBI       0, 0
            STII      4           ; TRANSFER RB TO CB
            STII      2
            JSRP      WRCMND
            LBI       0, 0        ; NOW WRITE RA/CA WITH 0443 HEX FOR THE DELAY
            STII      3
            STII      4
            STII      4
            STII      0
            STII      1
            STII      2
            JSRP      WRDATA
            LBI       0, 0
            STII      5
            STII      2
            JSRP      WRCMND      ; TRANSFER RA TO CA
            LBI       0, 0
            STII      9
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            STII      2           ; SET OSCILLATOR DIVIDER TO DIVIDE BY 4
            JSRP      WRCMND
            LBI       0, 0
            STII      1           ; SET TRIGGERED PULSE MODE
            STII      3
            JSRP      WRCMND
; ALL COMPLETE AT THIS POINT. ROUTINES WRCMND AND WRDATA ASSUMED
; IN PAGE 2 AND ARE THE SAME AS GIVEN IN SOFTWARE INTERFACE SECTION.
; THE COP452L WILL NOW GENERATE THE 150 μs PULSE DELAYED BY 2.0833 ms
; FROM EVERY ZERO CROSSING. THE USER CAN NOW IGNORE THE TRIAC CONTROL
; AND DO WHATEVER ELSE IS REQUIRED IN THE SYSTEM. FURTHER ATTENTION
; IS REQUIRED ONLY WHEN THE DATA IN THE COP452 MUST BE CHANGED.
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Applications Information (Continued)

Let us now compute the minimum and maximum delays from the true zero crossing in this application. As indicated earlier, the period of the internal frequency here is 1.9075 μs. Counter A contains 0443 hex (decimal 1091). R_S is 150k and the peak input voltage is 180V. A 60 Hz sine wave is assumed. As given earlier, the minimum time is:

$$T_{MIN} = (A+1.5)t - \frac{1}{2\pi f}\arcsin\left(0.15\frac{R_S+2.6k}{V_{IN}\times 2.6k}\right)+0.3\ \mu s$$

Substituting we have:

$$T_{MIN} = 1092.5t - \frac{1}{120\pi}\arcsin\left(0.15\frac{152.6k}{180\times 2.6k}\right)+0.3\ \mu s$$

$$= 2093.9\ \mu s - 129.7\ \mu s + 0.3\ \mu s$$

$$T_{MIN} = 1954.5\ \mu s$$

Similarly, the maximum time is given as:

$$T_{MAX} = (A + 1.5)t + \frac{1}{2\pi f}\arcsin\left(0.15\frac{R_S + 2.6k}{V_{IN}\times 2.6k}\right) + 0.6\ \mu s + \frac{t}{2}$$

Substituting, we have:

$$T_{MAX} = 1092.5t + \frac{1}{120\pi}\arcsin\left(0.15\frac{152.6k}{180\times 2.6k}\right) + 0.6\ \mu s + \frac{1.9075\ \mu s}{2}$$

$$= 2083.9\ \mu s + 129.7\ \mu s + 0.6\ \mu s + 0.9538\ \mu s$$

$$T_{MAX} = 2215.15\ \mu s$$

As is obvious from the preceding analysis, the parameter previously defined as X_1 is the most significant of the additional factors that define the time delay from true zero. This factor can be minimized by using as small a series resistance as possible. The frequency and input voltage will be governed by the application. The user must also remember that the minimum and maximum times calculated in this manner are absolute worst case values derived using the worst case condition.