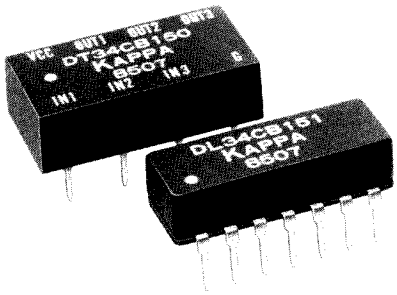
SERIES DL34/DT34 TTL SCHOTTKY • 3 INDEPENDENT DELAYS

TRIPLE DELAY LINES (14-PIN)



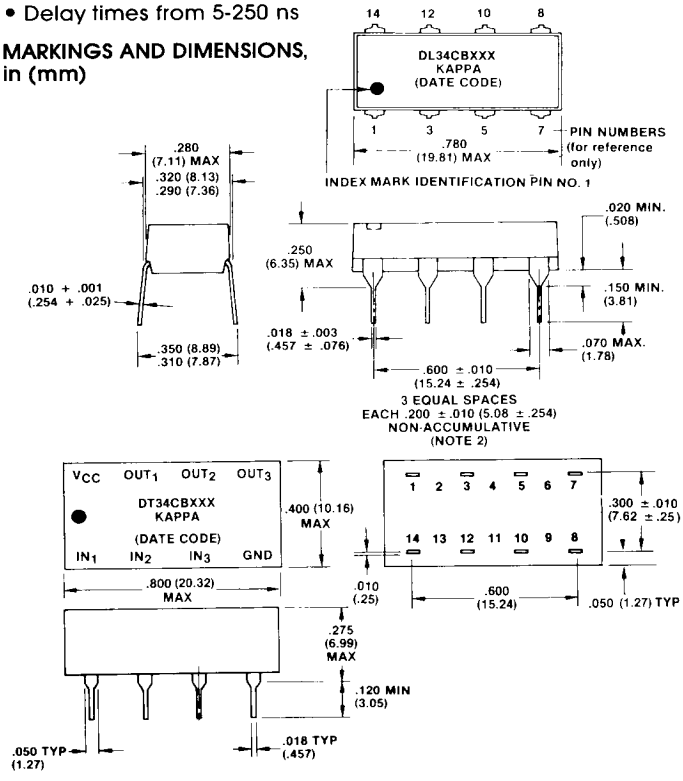
RECOMMENDED OPERATING CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	4.75	5.00	5.25	V
V_{IH}	High-Level Input Voltage	2.0			V
V_{IL}	Low-Level Input Voltage			0.8	V
I_{IK}	Input Clamp Current			−18	mA
I_{OH}	High-Level Output Current			−1.0	mA
I_{OL}	Low-Level Output Current			20	mA
T_A	Operating Free-Air Temperature	0	+25	+70	°C

DC ELECTRICAL CHARACTERISTICS		TEST CONDITIONS				
V_{OH}	High-Level Output Voltage	V_{CC} = min, V_{IH} =min, I_{OH} = max	2.7	3.4		V
V_{OL}	Low-Level Output Voltage	V_{CC} = min, V_{IL} = max, I_{OL} =max			0.5	V
V_{IK}	Input Clamp Voltage	V_{CC} = min, I_I = I_{IK}			−1.2	V
I_{IH}	High-Level Input Current	V_{CC} = max, V_{IN} = 2.7V			50	μA
		V_{CC} = max, V_{IN} = 5.25V			1.0	mA
I_{IL}	Low-Level Input Current	V_{CC} = max, V_{IN} = 0.5V			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = max, V_{OUT} = 0, one output at a time	−40		−100	mA
I_{CCH}	High-Level Supply Current	V_{CC} = max, V_{IN} = OPEN			90	mA
I_{CCL}	Low-Level Supply Current	V_{CC} = max, V_{IN} = 0			115	mA
N_H	Fanout High-Level Output	V_{CC} = max, V_{OH} = 2.7V			10	TTL load
N_L	Fanout Low-Level Output	V_{CC} = max, V_{OL} = 0.5V			10	TTL load

FEATURES

- Available in auto-insertable (DL34) and standard (DT34) 14-Pin package
- Risetime: 4 ns max(5)(6)
- 3 independent equal delays
- TTL Schottky interfaced
- Delay times from 5-250 ns

MARKINGS AND DIMENSIONS, in (mm)



Marking and dimensions notes:

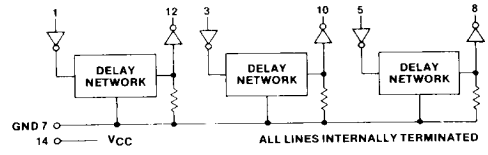
1. A notch may be substituted for PIN #1 Dot Index.
2. Each terminal is located within ±.010 of its nominal multiple of .100 along this longitudinal dimension relative to terminals 7 and 8.

INPUT PULSE TEST CONDITIONS					
E_{IN}	Pulse Voltage	3.1	3.2	3.3	V
T_{RI}	Pulse Rise-Time			2.0	ns
T_W	Pulse Width, of Total Delay	100			%
d	Duty Cycle		33.3	50	%

PART NUMBER(7)	Total Delay (ns)(1) (2)
DL34/DT34CB250	25
DL34/DT34CB500	50
DL34/DT34CB750	75
DL34/DT34CB101	100
DL34/DT34CB251	250

Notes:

1. Delays measured at 1.5V level on leading edge only.
2. Delay tolerances: ±5% or ±2 ns, whichever is greater, referenced from input and guaranteed only under the following test conditions: V_{CC} = Typ, T_A = Typ, E_{IN} = Typ, T_{RI} = max, T_W = min, P_{RR} = 1MHz (or d/tw, whichever is less), R_L 1 megohm and C_L 2pf.
3. Temperature coefficient of delay will vary, depending upon total delay, according to the formula: $T_{PTA} = (100 + (25{,}000/T_{PLH}))$.
4. Delay will inversely vary about 4% for every 5% change in supply voltage.
5. Risetime measured from 0.75V to 2.4V level.
6. Measured with no loads.
7. **Other delays also available upon request.**



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