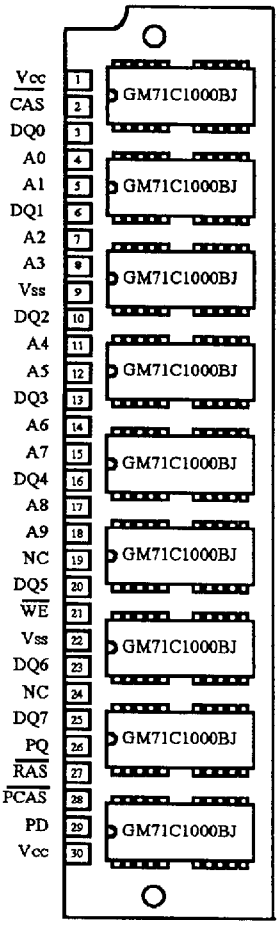
Description

The GMM791000BS is an 1M x 9 bits Dynamic RAM Module which is assembled 9 pieces of 1M bit DRAM (GM71C1000BJ, 1Mx1) in 20/26 pin small out-line J-form on a 30 pin single in-line package. These are a socket type memory module, suitable for easy change or addition of module, and provide common data inputs and outputs. It's module board has decoupling capacitors mounted under each DRAM. The GMM791000BS provides separate I/O on parity bit for parity check.

• **GMM791000BS** (Single Side)



Features

- High Density JEDEC standard 30 pin mounting 9 pcs of 1M DRAM
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

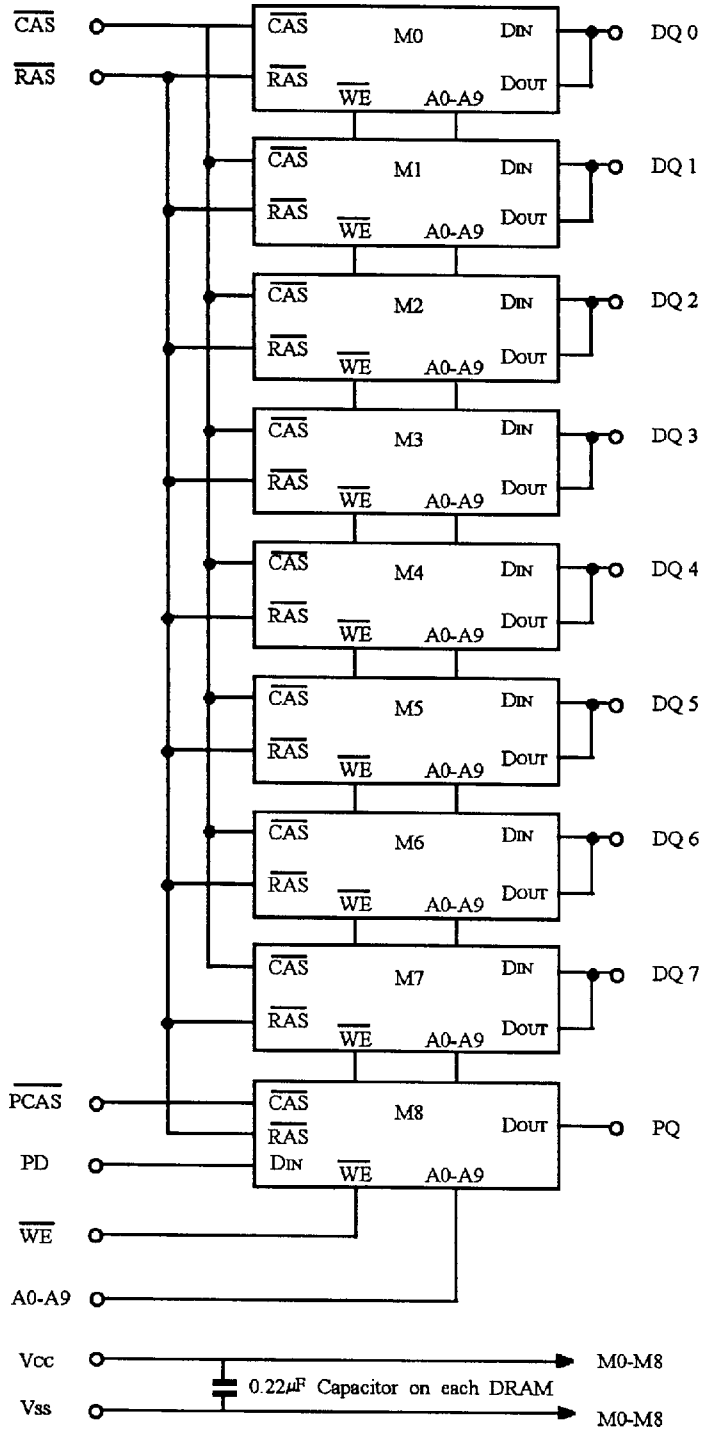
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM791000BS-60	60	20	120	40
GMM791000BS-70	70	20	130	50
GMM791000BS-80	80	25	160	55

- Low Power
  Active : 4,455/3,960/3,465mW (MAX)
  Standby : 49.5mW (CMOS level : MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms

Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	Vss
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	PQ
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{PCAS}$
9	Vss	19	NC	29	PD
10	DQ2	20	DQ5	30	Vcc

Bolck Diagram



Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	PD1-PD4	Presence Detect
DQ0-DQ31	Data Input/Output	V_{CC}	Power (+5V)
$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Read/Write Enable		

Presence Detect Pins (Optional)

Pin	60ns	70ns	80ns
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	2	W

*Note: 1. Stress greater than above "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended DC Operating Conditions (T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	-	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	1

*Note: 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70℃$)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	-	810	mA	1, 2
		70ns	-	720		
		80ns	-	630		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		-	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	-	810	mA	2
		70ns	-	720		
		80ns	-	630		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling : t_{PC} = t_{PC} min)	60ns	-	720	mA	1, 3
		70ns	-	630		
		80ns	-	450		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} \geq V_{CC}$-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	720	mA	
		70ns	-	630		
		80ns	-	540		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	45	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$) All Other Pins Not Under Test = 0V	PD, $\overline{PCAS}$	-10	10	μA	
		ADDR, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	-90	90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)	PQ	-10	10	μA	
		DQ	-20	20		

Note: 1. I_{CC} depends on output load condition when the device is selected. I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25℃$, $f = 1MHz$)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	60	pF	1
C_{I2}	Input Capacitance (Clocks)	-	75	pF	1, 2
C_{I3}	Input Capacitance (PD)	-	10	pF	1
C_{I4}	Input Capacitance ($\overline{PCAS}$)	-	10	pF	1
$C_{I/O}$	I/O Capacitance (DQ0~DQ7)	-	17	pF	1, 2
C_O	Output Capacitance (PQ)	-	12	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70℃$, Notes 1, 14)

The GMM791000BS writes data only in early write cycle ($t_{WCS} \geq t_{WCS}(min)$).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	GMM791000 BS-60		GMM791000 BS-70		GMM791000 BS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120	-	130	-	160	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	50	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	12	-	ns	
t_{ASC}	Coumn Address Setup Time	0	-	0	-	0	-	ns	
t_{CAH}	Coumn Address Hold Time	15	-	15	-	20	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	22	55	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	70	-	80	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period (512 Cycles)	-	8	-	8	-	8	ms	

Read Cycle

Symbol	Parameter	GMM791000 BS-60		GMM791000 BS-70		GMM791000 BS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	2, 3
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	3, 4
t_{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	3, 5
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	-	10	-	10	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{OFF}	Output Buffer Turn-off Time	0	20	0	20	0	20	ns	6

Write Cycle

Symbol	Parameter	GMM791000 BS-60		GMM791000 BS-70		GMM791000 BS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	
t_{WP}	Write Command Pulse Width	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-in Hold Time	15	-	15	-	20	-	ns	11

Refresh Cycle

Symbol	Parameter	GMM791000 BS-60		GMM791000 BS-70		GMM791000 BS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	15	-	15	-	20	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time in Normal Mode	10	-	10	-	10	-	ns	

Fast Page Mode Cycle

Symbol	Parameter	GMM791000 BS-60		GMM791000 BS-70		GMM791000 BS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	-	50	-	55	-	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	50	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	45	-	50	-	ns	

Notes:

1. AC measurements assume $t_T = 5$ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$ defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} is defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.

Timing Waveforms

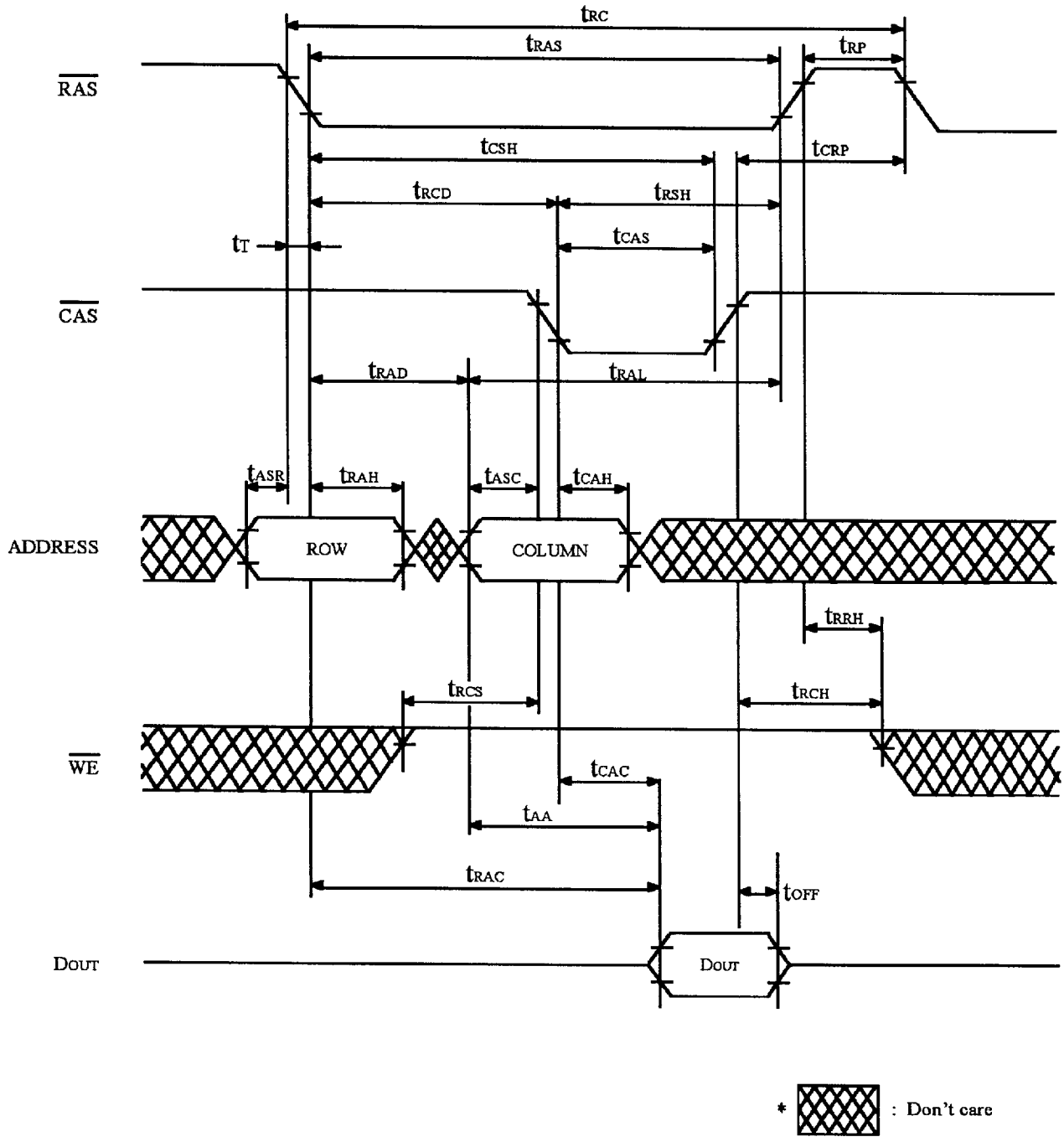


FIGURE 1. READ CYCLE

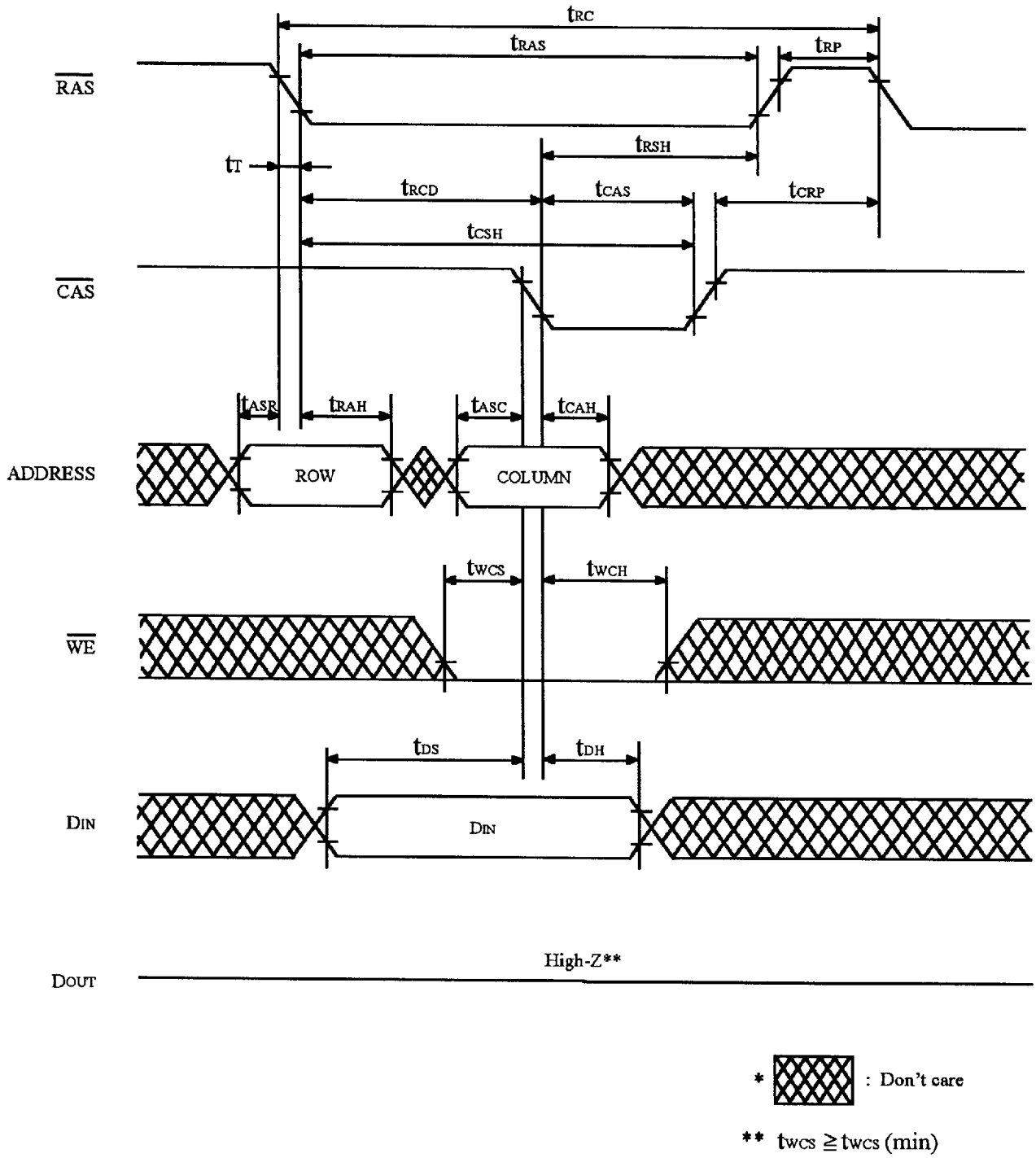


FIGURE 2. EARLY WRITE CYCLE

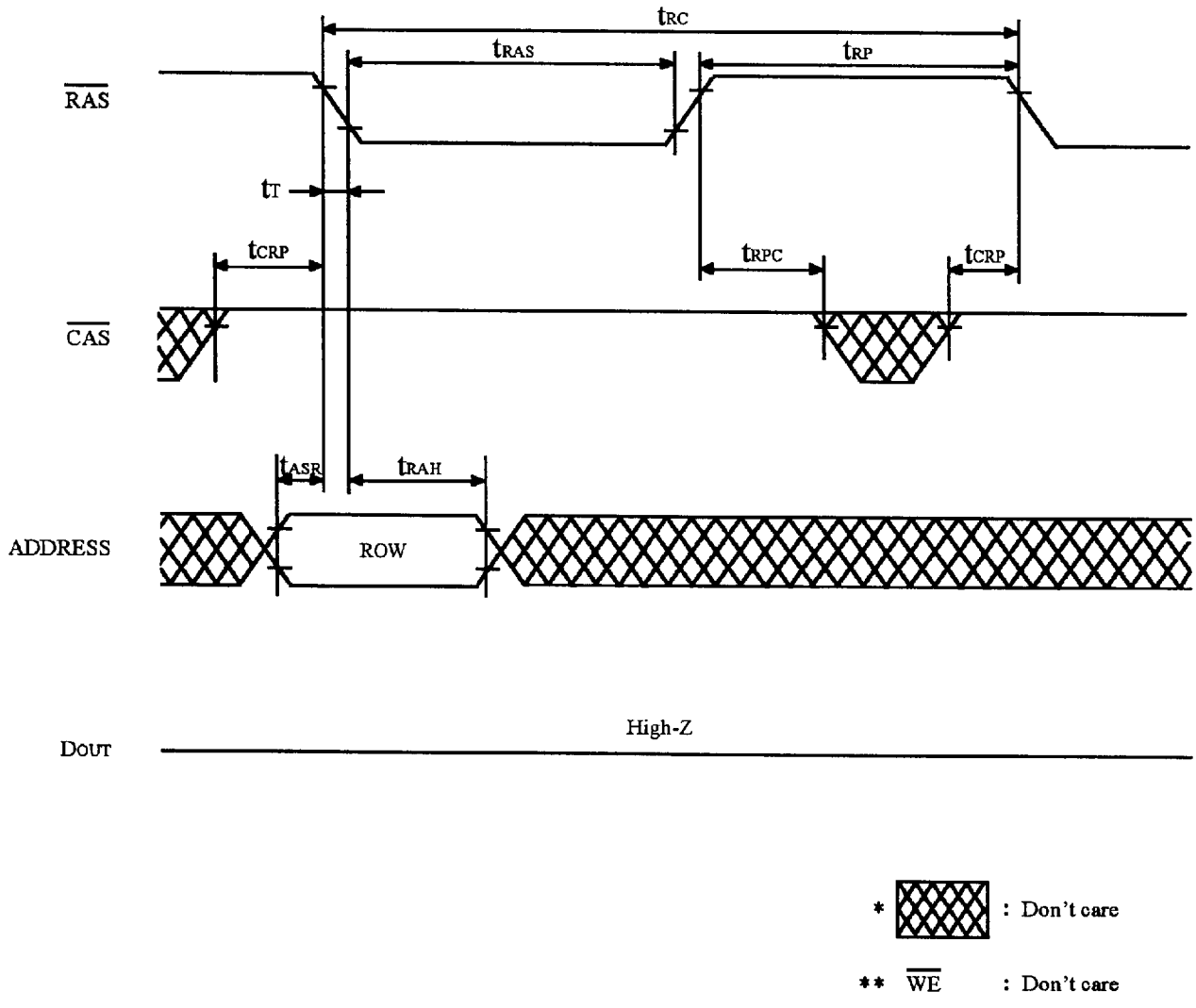
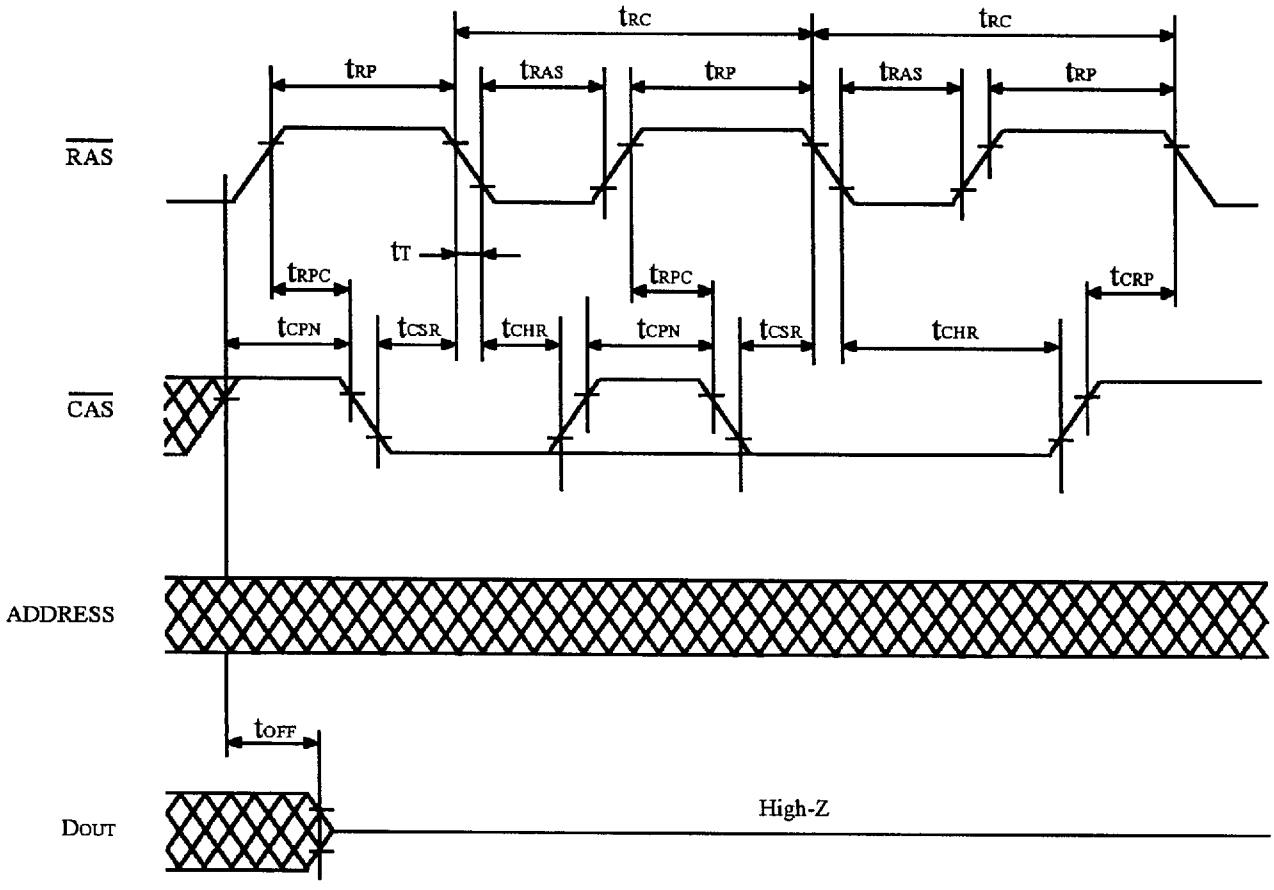


FIGURE 3. $\overline{RAS}$ ONLY REFRESH CYCLE



* : Don't care

* * $\overline{WE}$: V_{IH}

FIGURE 4. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

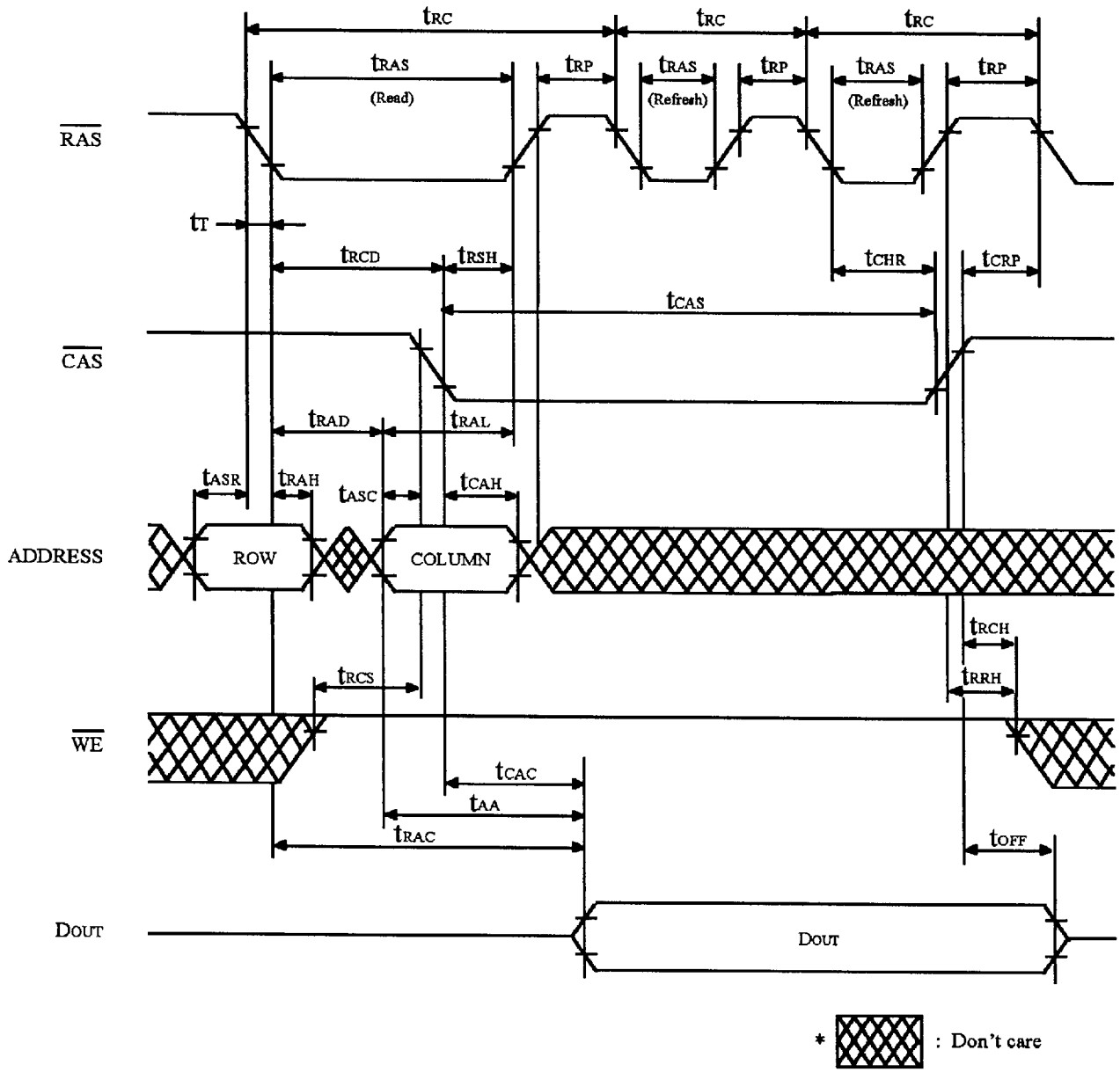


FIGURE 5. HIDDEN REFRESH CYCLE

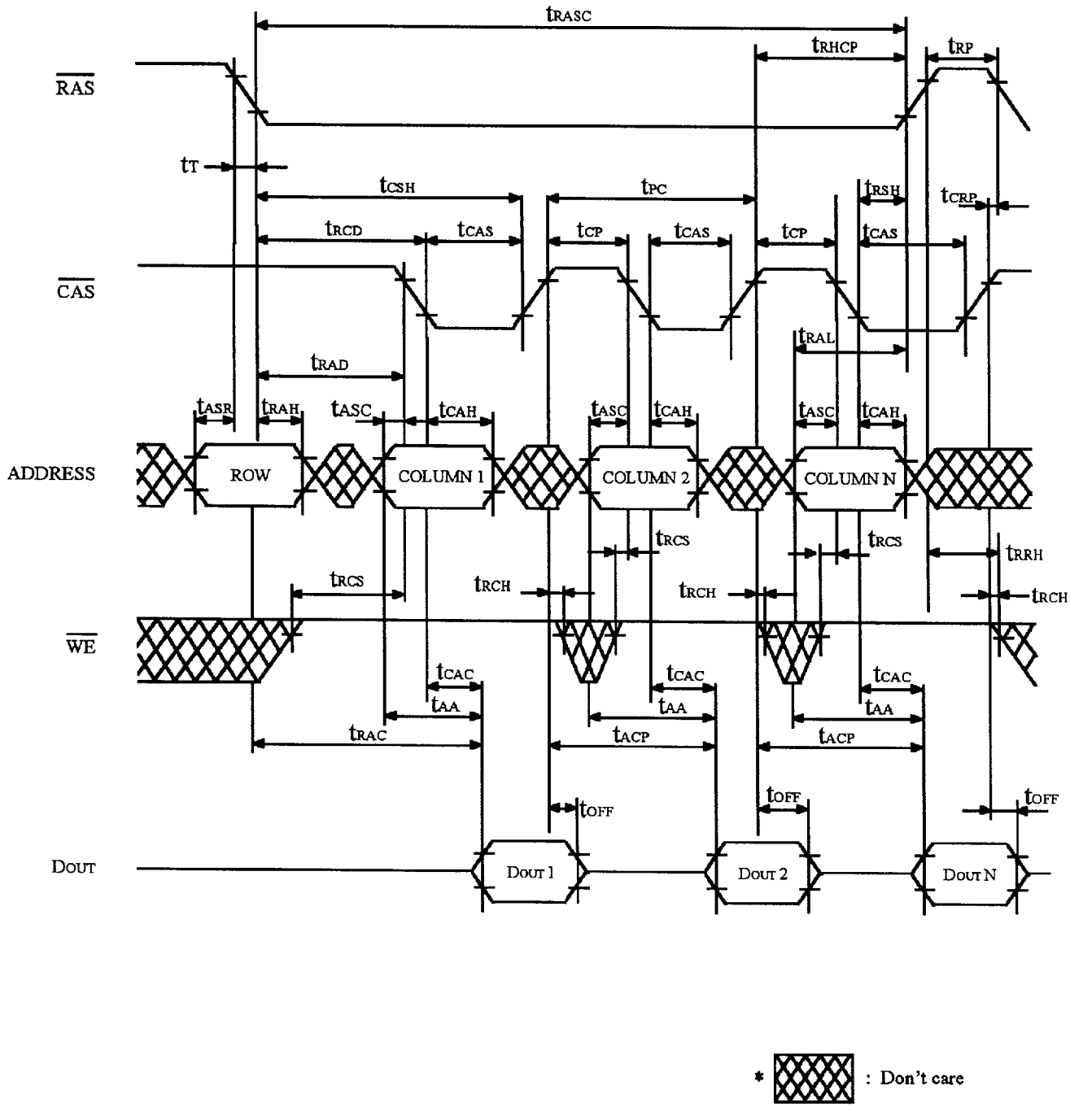


FIGURE 6. FAST PAGE MODE READ CYCLE

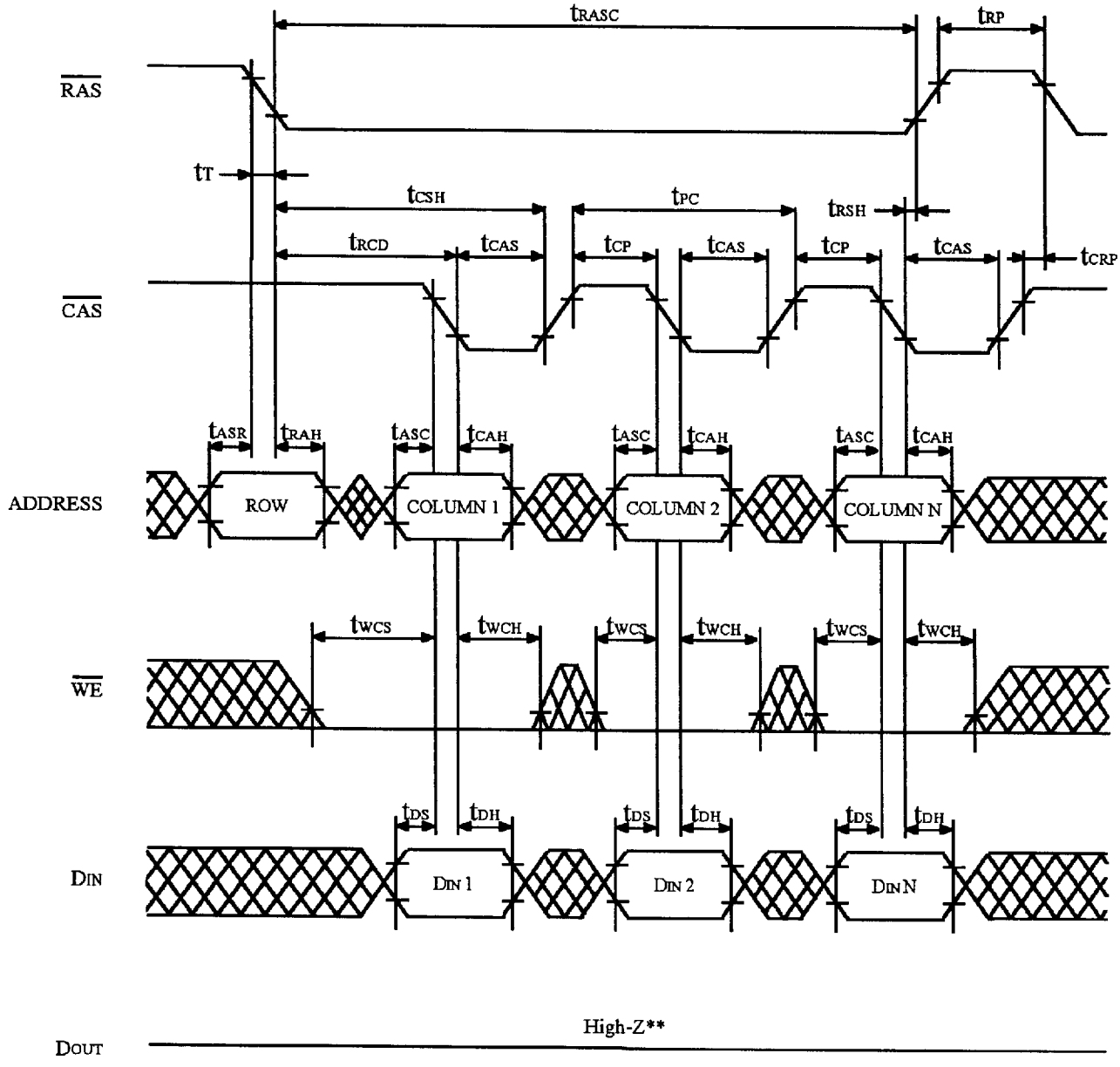


FIGURE 7. FAST PAGE MODE EARLY WRITE CYCLE