HB56D232B Series

T-46-23-18

2,097,152-Word x 32-Bit High Density Dynamic RAM Module

DESCRIPTION

The HB56D232B is a 2M x 32 dynamic RAM module, mounted 16 pieces of 4Mbit DRAM (HM514400JP) sealed in SOJ package. An outline of the HB56D232B is 72-pin single in-line package. Therefore, the HB56D232B makes high density mounting possible without surface mount technology. The HB56D232B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

FEATURES

- 72-pin Single In-line Package
  - Lead Pitch 1.27mm
- Single 5V (±5%) Supply
- High Speed
  - Access Time .....80 ns/100 ns/120 ns (max)
- Low Power Dissipation
  - Active Mode.....3.99W/3.57W/3.15W (max)
  - Standby Mode .....168 mW (max)
- Fast Page Mode Capability
- 1,024 Refresh Cycles .....(16 ms)
- 2 Variations of Refresh
  - $\overline{RAS}$ Only Refresh
  - $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- TTL Compatible

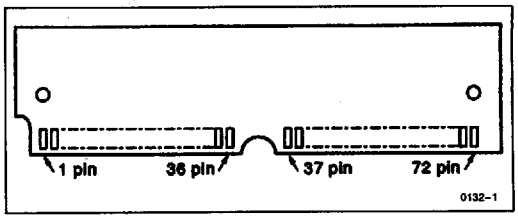
ORDERING INFORMATION

Part No.	Access Time	Package
HB56D232B-8	80 ns	72-pin SIP Socket Type
HB56D232B-10	100 ns	
HB56D232B-12	120 ns	

PRESENCE DETECT PINOUT

Pin No.	Pin Name	HB56D132BR		
		80 ns	100 ns	120 ns
67	PD_1	V_{SS}	V_{SS}	V_{SS}
68	PD_2	V_{SS}	V_{SS}	V_{SS}
69	PD_3	NC	V_{SS}	NC
70	PD_4	V_{SS}	V_{SS}	NC

PIN OUT



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	19	NC	37	NC	55	DQ_{11}
2	DQ_0	20	DQ_4	38	NC	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS3}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS1}$	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS1}$	63	DQ_{14}
10	V_{CC}	28	A_7	46	NC	64	DQ_{31}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_8	67	PD_1
14	A_2	32	A_9	50	DQ_{24}	68	PD_2
15	A_3	33	$\overline{RAS3}$	51	DQ_9	69	PD_3
16	A_4	34	$\overline{RAS2}$	52	DQ_{25}	70	PD_4
17	A_5	35	NC	53	DQ_{10}	71	NC
18	A_6	36	NC	54	DQ_{26}	72	V_{SS}

PIN DESCRIPTION

Pin Name	Function
A_0–A_9	Address Input
A_0–A_9	Refresh Address Input
DQ_0–DQ_{31}	Data-in/Data-out
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobe
$\overline{WE}$	Read/Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
PD_1–PD_4	Presence Detect Pin
NC	Non-Connection

■ BLOCK DIAGRAM

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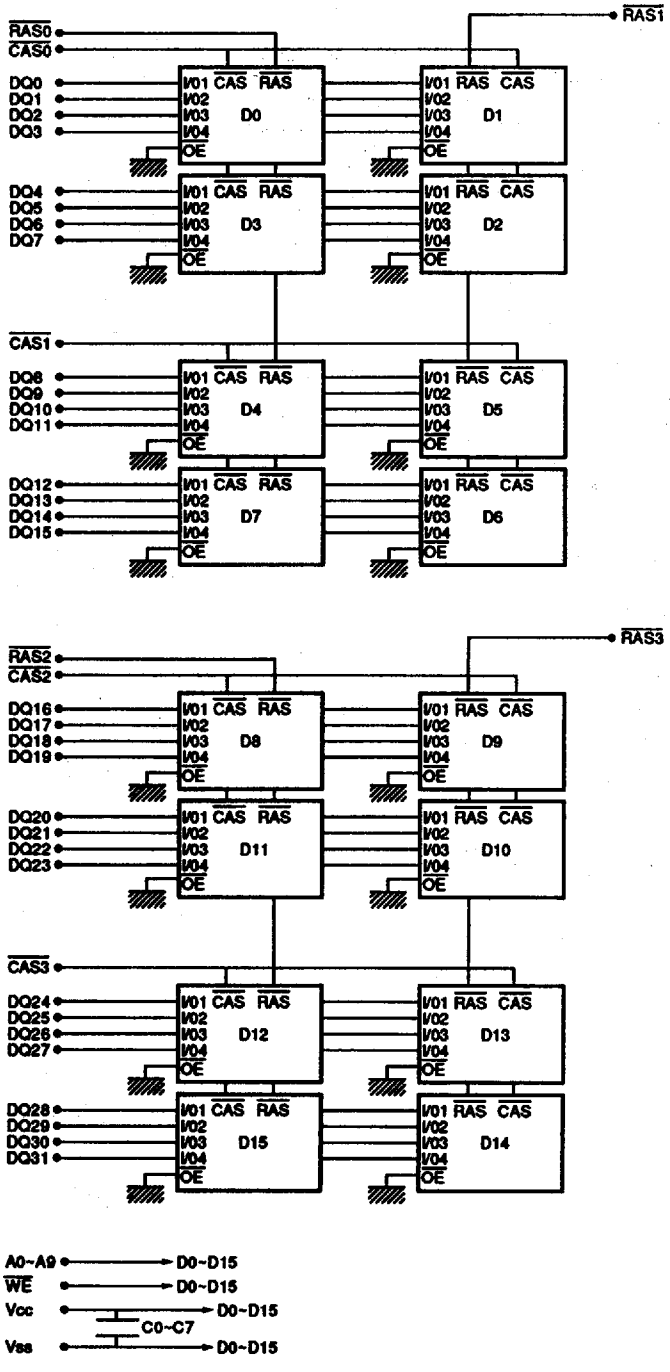


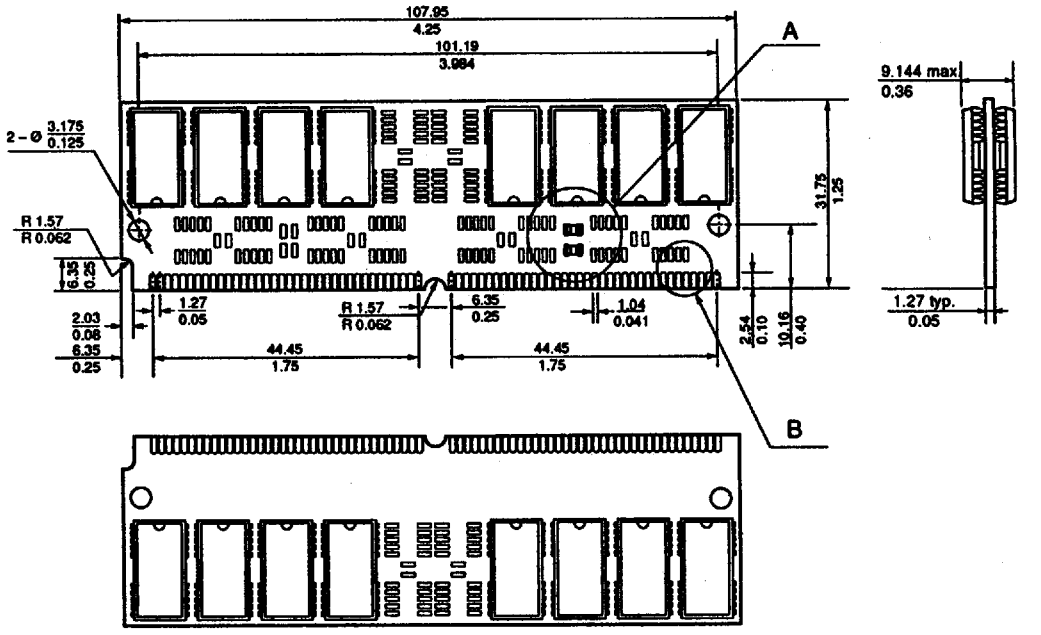
* D0~D15 : HM514400JP

0132-2

■ PHYSICAL OUTLINE

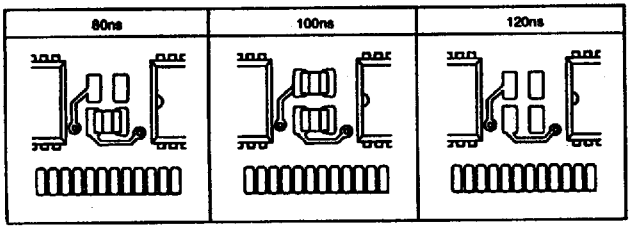
T-46-23-18

Unit: mm / inch



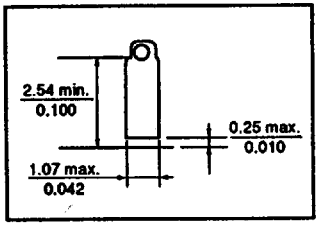
0132-3

Detail A



0132-4

Detail B



0132-5

Note: The plating of the contact finger is gold.

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■ ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	(Input)	V_{in}	−1.0 to +7.0	V
	(Output)	V_{out}	−1.0 to +7.0	V
Supply Voltage Relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short Circuit Output Current		I_{out}	50	mA
Power Dissipation		P_T	8	W
Operating Temperature		T_{opr}	0 to +70	°C
Storage Temperature		T_{stg}	−55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.4	—	5.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

• DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max			
Operating Current	I_{CC1}	—	760	—	680	—	600	mA	t_{RC} = Min	1, 2
Standby Current	I_{CC2}	—	32	—	32	—	32	mA	TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{out} = High-Z	
		—	16	—	16	—	16	mA	CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2V, D_{out} = High-Z	
$\overline{RAS}$ Only Refresh Current	I_{CC3}	—	760	—	680	—	600	mA	t_{RC} = Min	2
Standby Current	I_{CC5}	—	80	—	80	—	80	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} D_{out} = Enable	1
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	I_{CC6}	—	760	—	680	—	600	mA	t_{RC} = Min	
Page Mode Current	I_{CC7}	—	760	—	680	—	600	mA	t_{PC} = Min	1, 3
Input Leakage Current	I_{LI}	−10	10	−10	10	−10	10	µA	0V ≤ V_{in} ≤ 7V	
Output Leakage Current	I_{LO}	−10	10	−10	10	−10	10	µA	0V ≤ V_{out} ≤ 7V, D_{out} = Disable	
Output High Voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High I_{out} = −5 mA	
Output Low Voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low I_{out} = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

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• **Capacitance** (T_A = 25°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Typ	Max	Unit	Note
Input Capacitance (Address)	C_{I1}	—	121	pF	1
Input Capacitance ($\overline{WE}$)	C_{I2}	—	137	pF	1
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	48	pF	1
Output Capacitance (DQ_0–DQ_{31})	$C_{I/O}$	—	29	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{out}.

• **AC Characteristics** (T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{SS} = 0V)[1, 12]

Read, Write, and Refresh Cycles (Common Parameters)

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	12	—	15	—	15	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	10	—	10	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	15

Read Cycle

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Access Time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	—	45	—	55	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	15	—	20	—	25	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

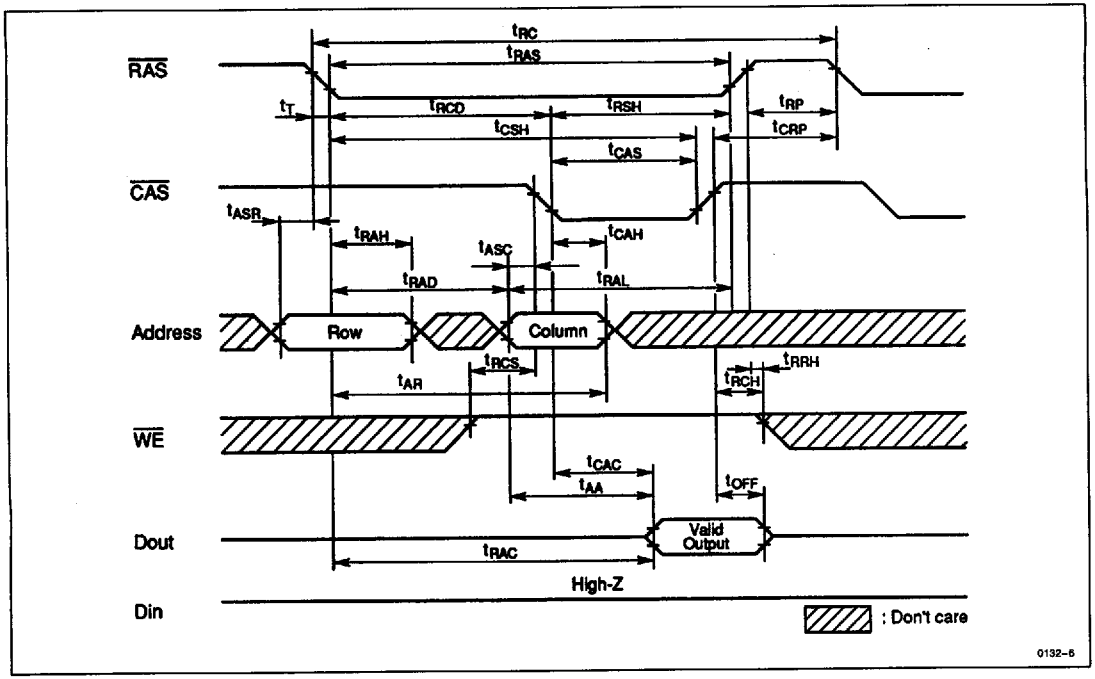
Parameter	Symbol	HB56D232B-8		HB56D232B-10		HB56D232B-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{PC}	55	—	55	—	65	—	ns	
Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	15	—	ns	
Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	50	—	50	—	50	—	ns	

Notes:
1. AC measurements assume $t_T = 5$ ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

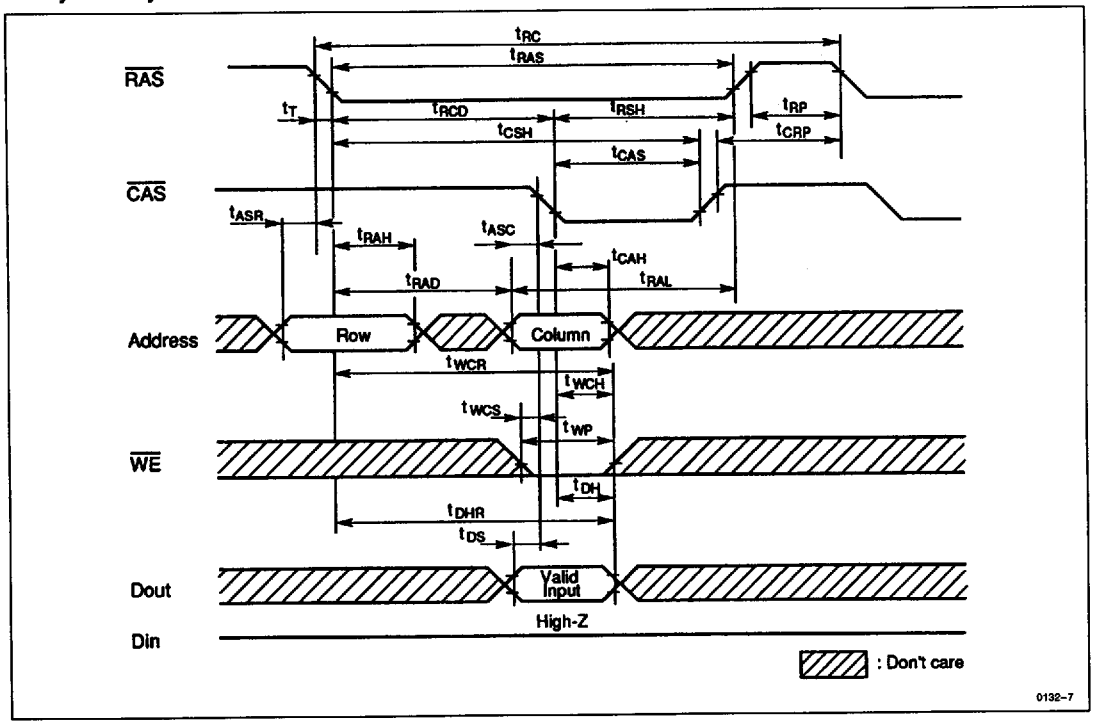
■ TIMING WAVEFORMS

T-46-23-18

• Read Cycle



• Early Write Cycle



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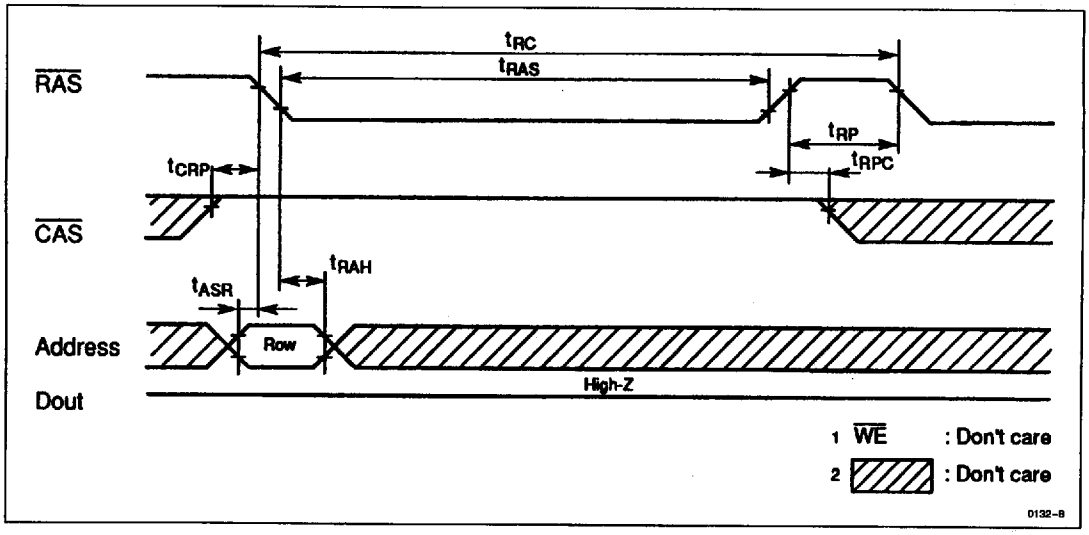
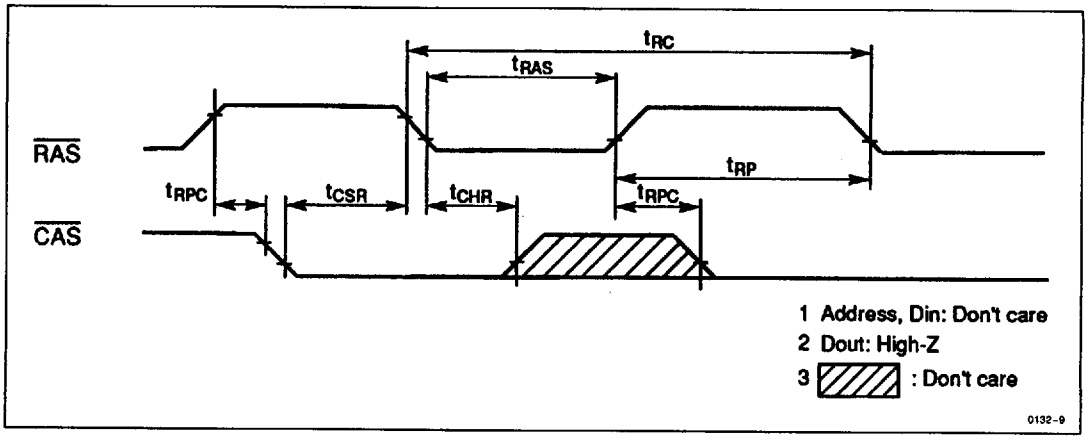
• $\overline{RAS}$ Only Refresh Cycle



• $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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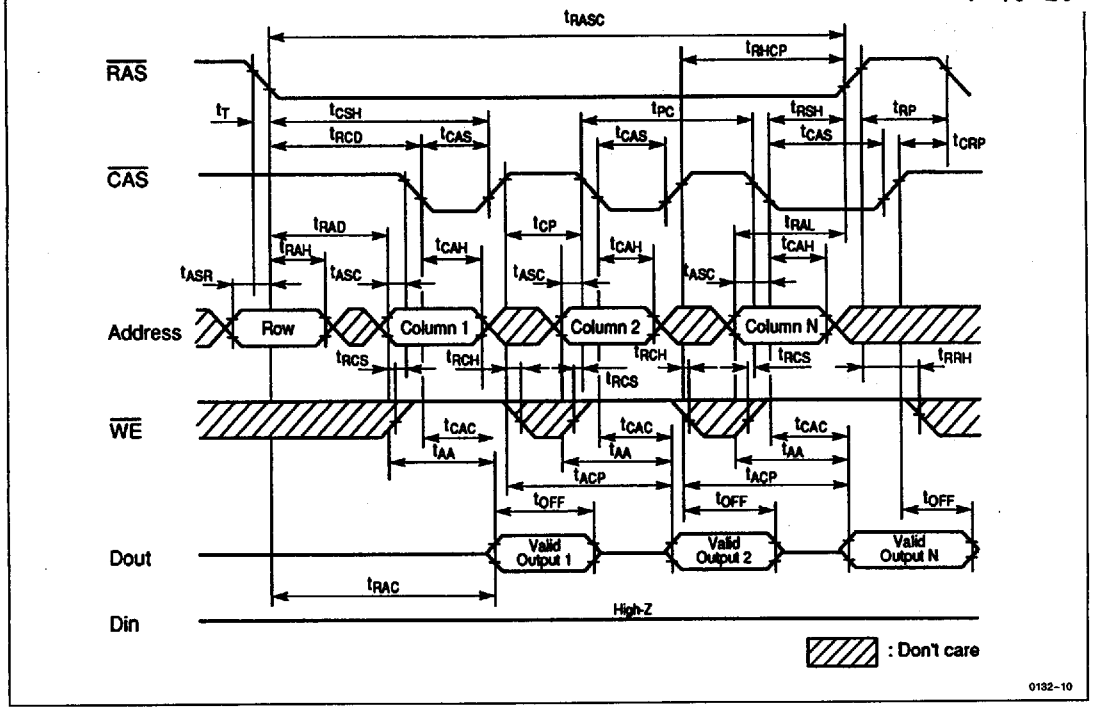
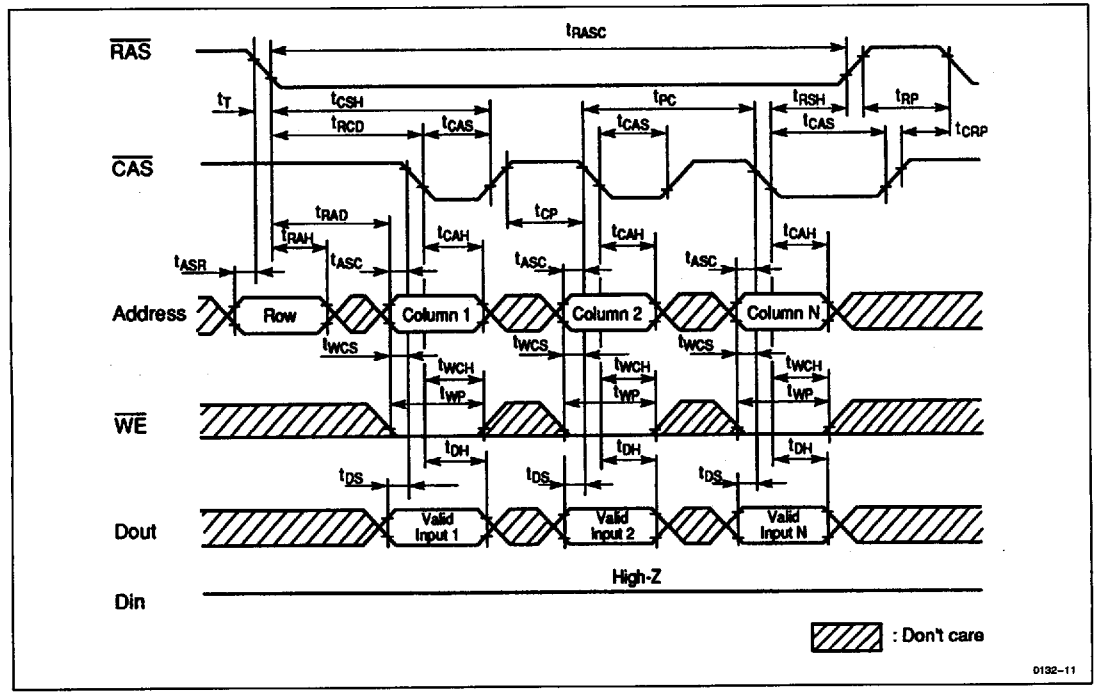
• **Fast Page Mode Read Cycle**



• **Fast Page Mode Early Write Cycle**



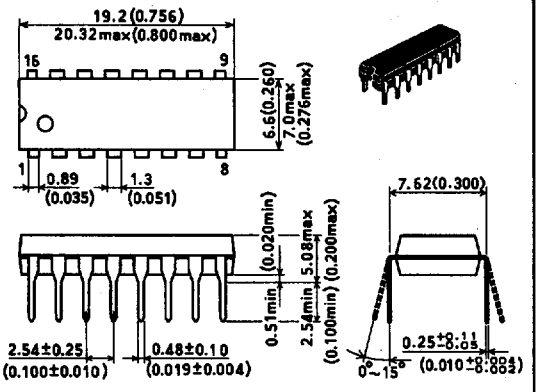
PACKAGE INFORMATION

T-90-20

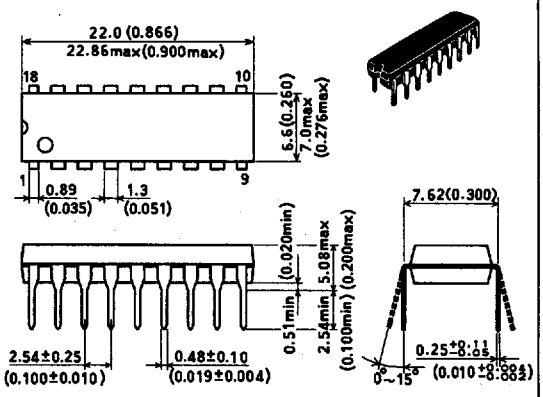
• Dual-in-line Plastic

Unit: mm (inch) Scale 3/2

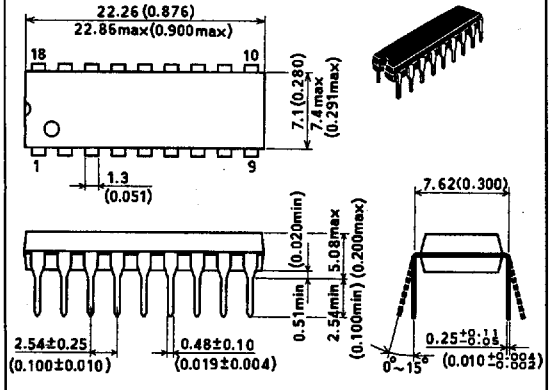
• DP-16B



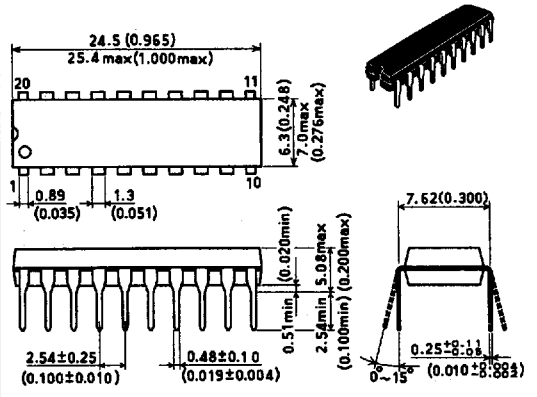
• DP-18B



• DP-18C



• DP-20N



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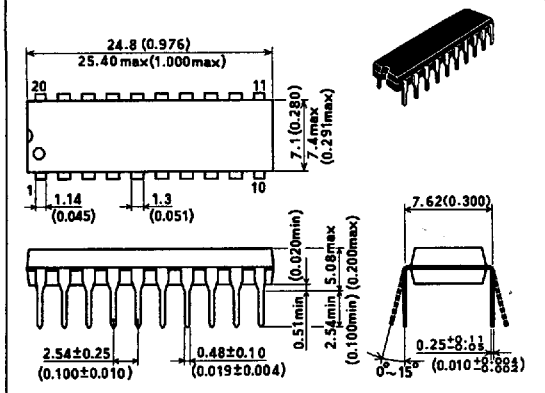
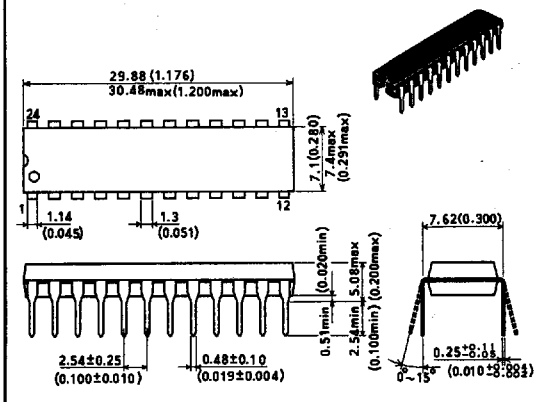


• DP-20NC

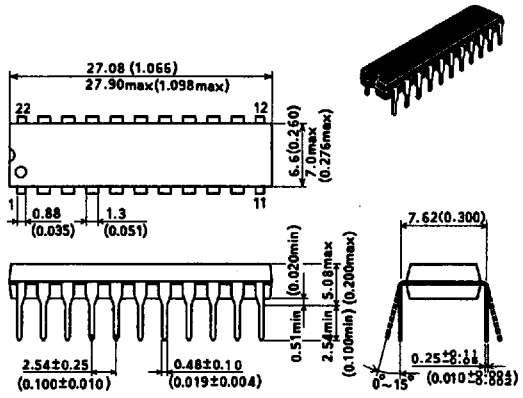


• Dual-in-line Plastic

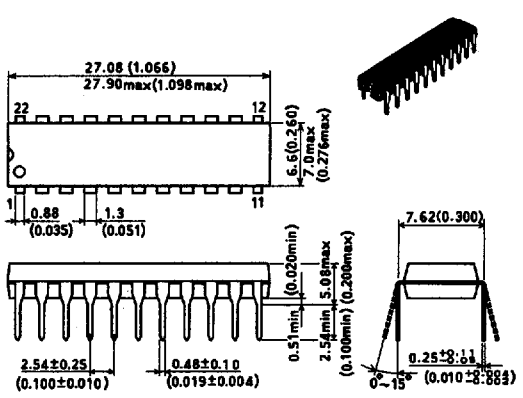
Unit: mm (inch) Scale 3/2

T-90-20

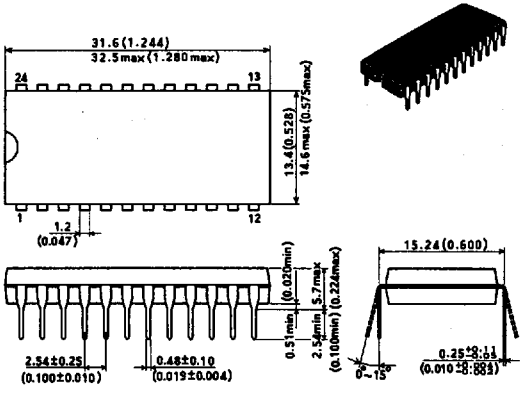
• DP-22N



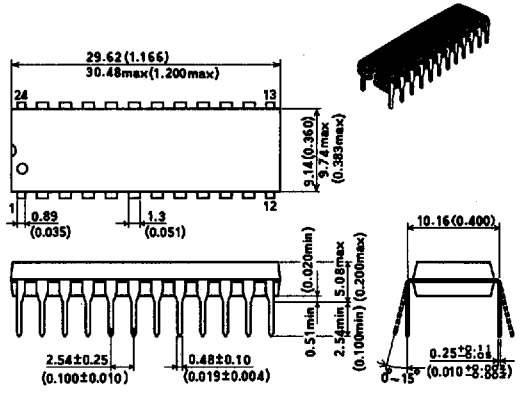
• DP-22NB



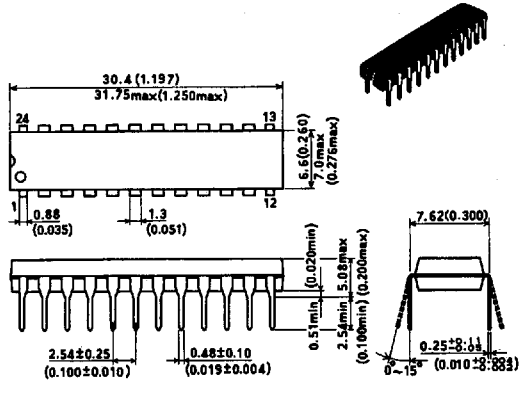
• DP-24



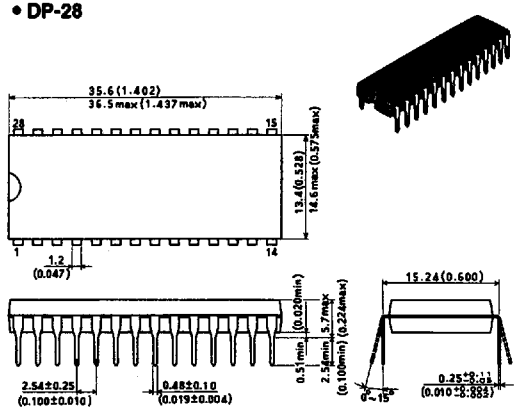
• DP-24A



• DP-24N



• DP-28



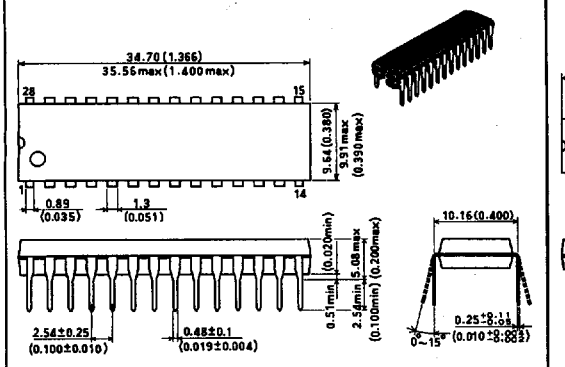
• Dual-in-line Plastic

HITACHI/ LOGIC/ARRAYS/MEM

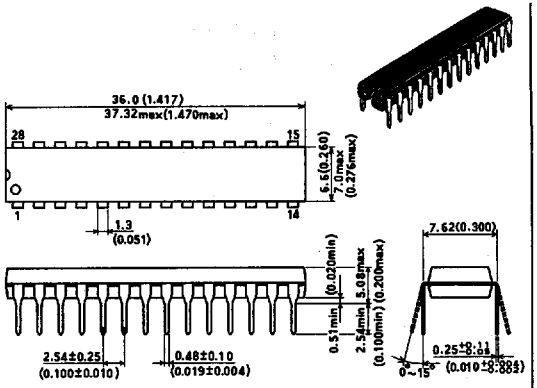
Unit: mm (inch) Scale 3/2

T-90-20

• DP-28C



• DP-28N

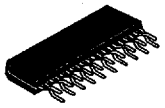


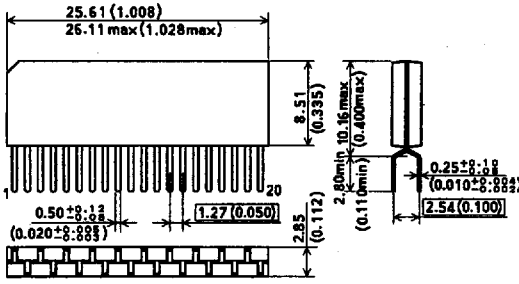
• Zigzag-in-line Plastic HITACHI/ LOGIC/ARRAYS/MEM

Unit: mm (inch) Scale 3/2

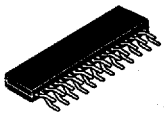
T-90-20

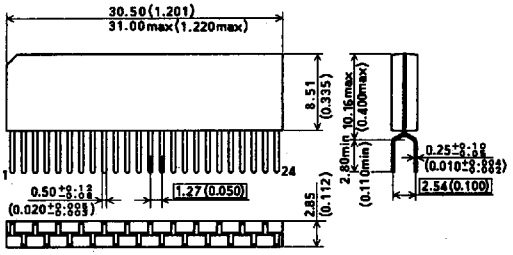
• ZP-20



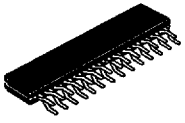


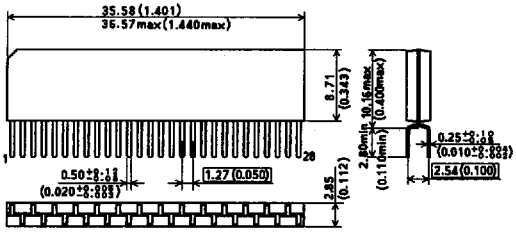
• ZP-24



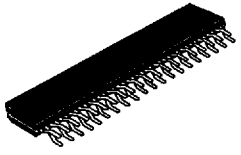


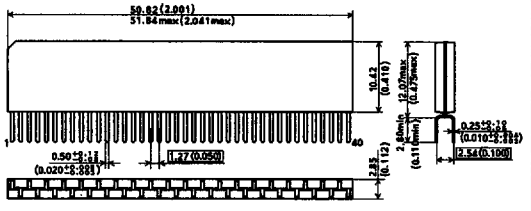
• ZP-28





• ZP-40





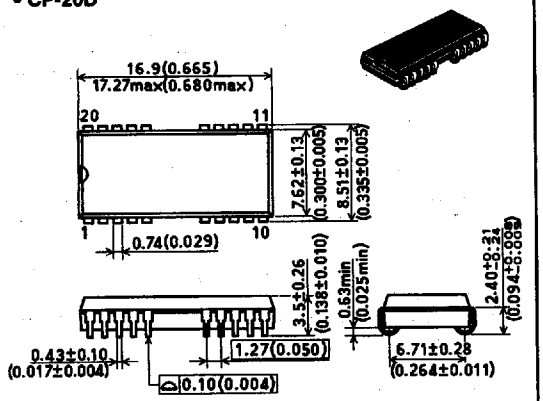
• Flat Package (J-bend Leads)

HITACHI/ LOGIC/ARRAYS/MEM

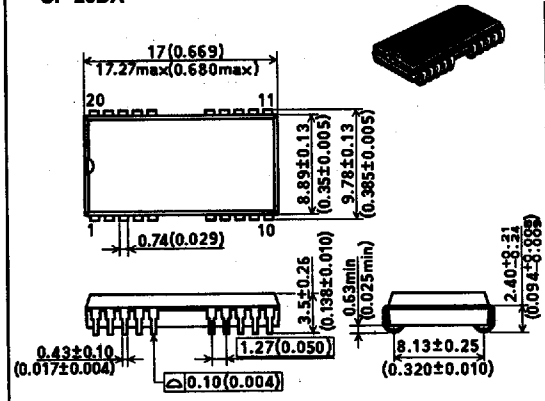
Unit: mm (inch) Scale 3/2

T-90-20

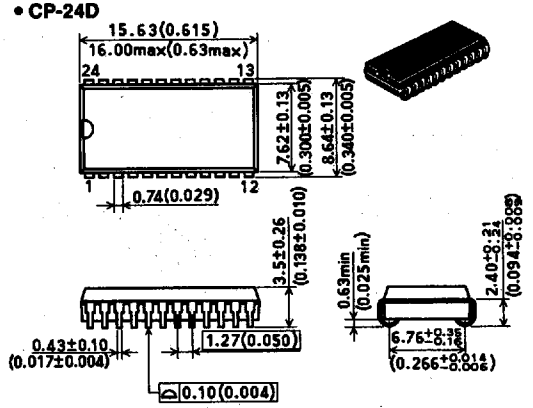
• CP-20D



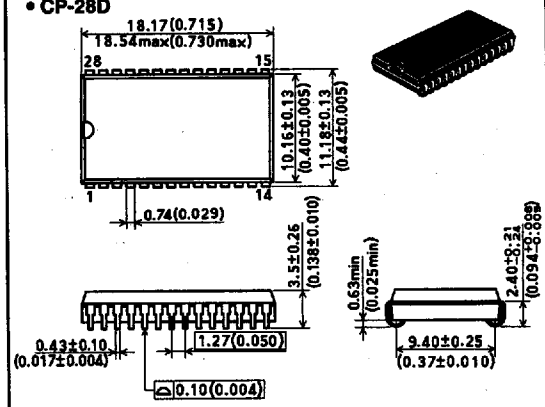
• CP-20DA



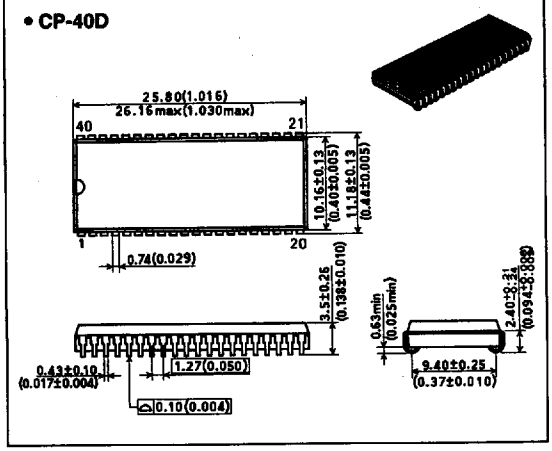
• CP-24D



• CP-28D



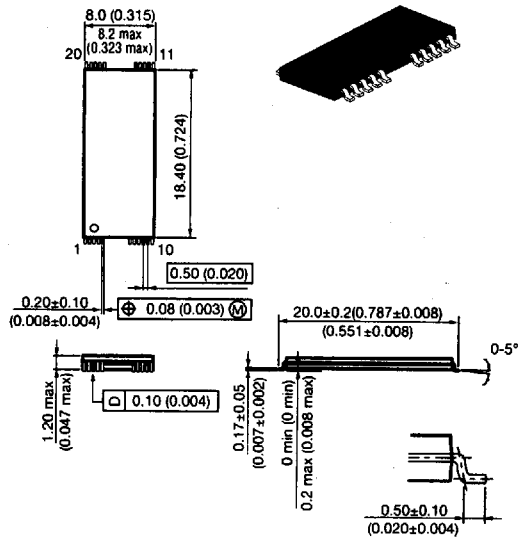
• CP-40D



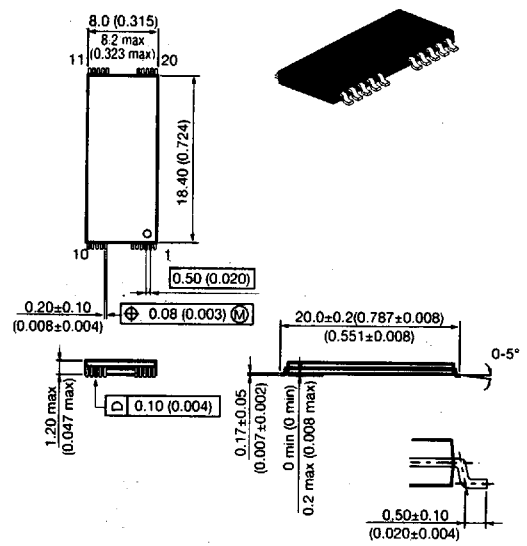
• TSOP (Thin Small Outline Package)

Unit: mm (inch) Scale 3/2

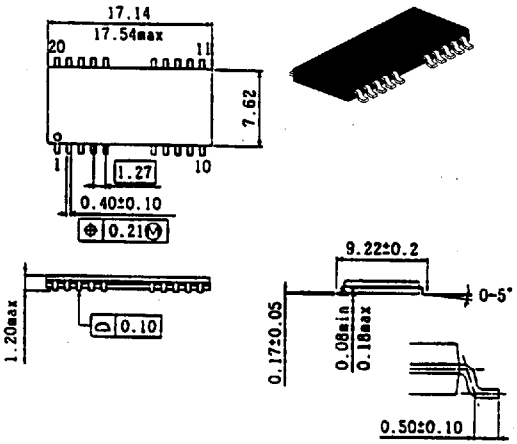
• TFP-20DA



• TFP-20DAR



• TTP-20D



• TTP-20DR