

HM514100B/BL Series

4,194,304-word × 1-bit Dynamic Random Access Memory

The Hitachi HM514100B is a CMOS dynamic RAM organized 4,194,304 words × 1 bits. HM514100B has realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514100B offers Fast Page Mode as a high speed access mode. Multiplexed address input permits the HM514100B to be packaged in standard 300-mil 20-pin plastic SOJ, standard 400-mil 20-pin plastic ZIP, 20-pin plastic TSOP I and 20-pin plastic TSOP II.

Features

- Single 5 V (±10%)
- High speed
 - Access time
60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode
605 mW/550 mW/495 mW (max)
 - Standby mode 11 mW (max)
0.55 mW (max) (L-version)
- Fast page mode capability
- 1024 refresh cycles : 16 ms
1024 refresh cycles : 128 ms (L-version)
- 3 variations of refresh
 - RAS-only refresh
 - CAS-before-RAS refresh
 - Hidden refresh
- Test function
- Battery back up operation
 - HM514100BL Series (L-version)

Ordering Information

Type No.	Access time	Package
HM514100BS/BLS-6	60 ns	300-mil 20-pin plastic SOJ (CP-20D)
HM514100BS/BLS-7	70 ns	
HM514100BS/BLS-8	80 ns	
HM514100BZ/BLZ-6	60 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514100BZ/BLZ-7	70 ns	
HM514100BZ/BLZ-8	80 ns	
HM514100BT/BLT-6	60 ns	20-pin plastic TSOP I (TFP-20DA)
HM514100BT/BLT-7	70 ns	
HM514100BT/BLT-8	80 ns	
HM514100BR/BLR-6	60 ns	20-pin plastic TSOP II reverse (TFP-20DAR)
HM514100BR/BLR-7	70 ns	
HM514100BR/BLR-8	80 ns	
HM514100BTT/BLTT-6	60 ns	20-pin plastic TSOP II (TTP-20D)
HM514100BTT/BLTT-7	70 ns	
HM514100BTT/BLTT-8	80 ns	
HM514100BRR/BLRR-6	60 ns	20-pin plastic TSOP II reverse (TTP-20DR)
HM514100BRR/BLRR-7	70 ns	
HM514100BRR/BLRR-8	80 ns	

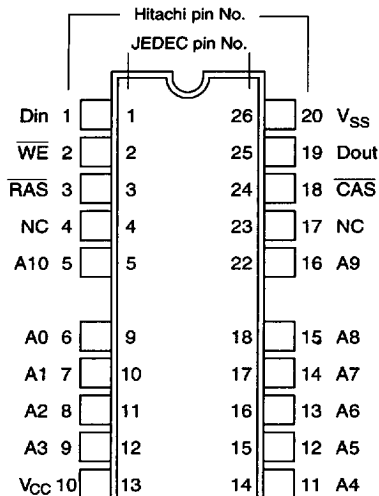
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HM514100B/BL Series

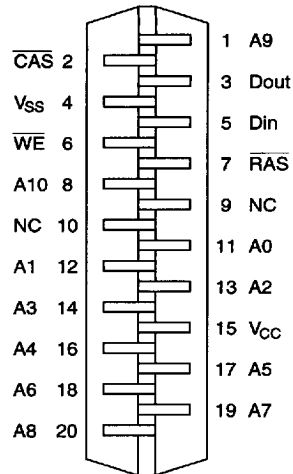
Pin Arrangement

HM514100BS/BLS Series



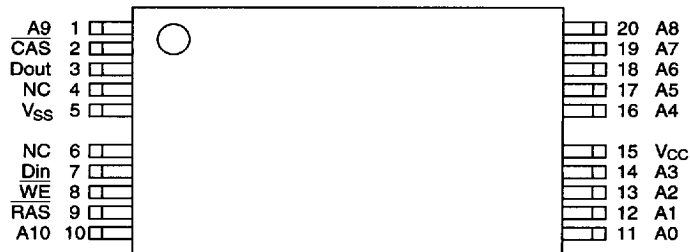
(Top view)

HM514100BZ/BLZ Series



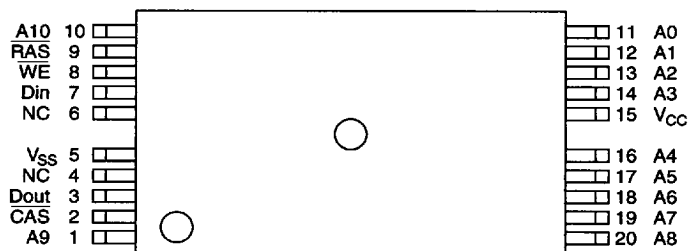
(Bottom view)

HM514100BT/BLT Series



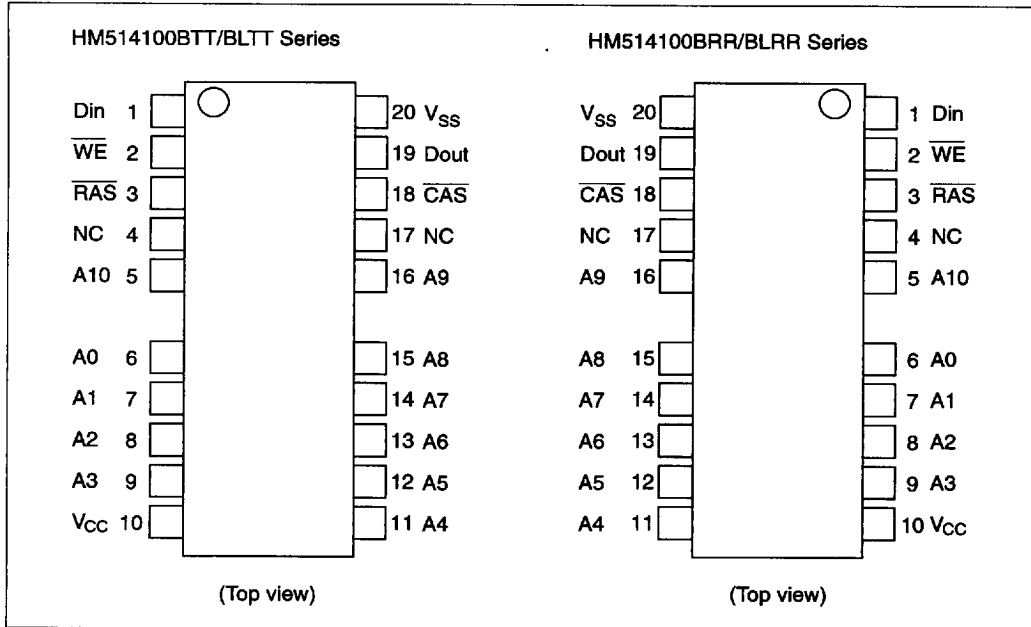
(Top view)

HM514100BR/BLR Series



(Top view)

Pin Arrangement (cont.)

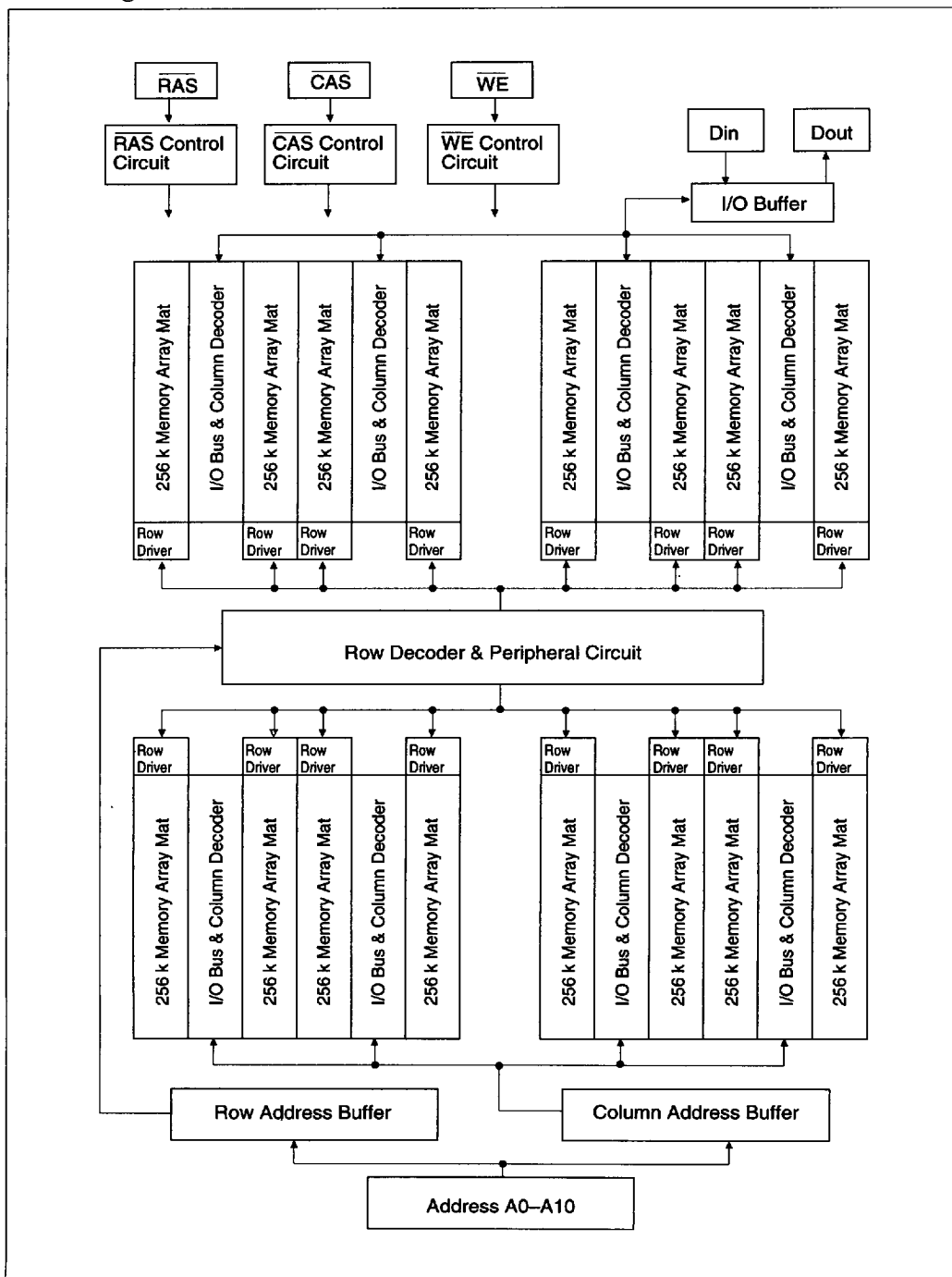


Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A9	Refresh address input
Din	Data-in
Dout	Data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
V _{CC}	Power (+5 V)
V _{SS}	Ground
NC	No connection

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Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note : 1. All voltage referred to V_{SS} .

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DC Characteristics ($T_a = 0 \text{ to } +70^\circ\text{C}$, $V_{CC} = 5 \text{ V} \pm 10\%$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Test condition	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	110	—	100	—	90	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling $t_{RC} = \text{min}$	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$ Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{\text{RAS}}$, $\overline{\text{CAS}} \geq$ $V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
Standby current (L-version)		—	100	—	100	—	100	μA	CMOS interface $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$ $\overline{\text{WE}}$, Address, Din $= V_{IH}$ or V_{IL} Dout = High-Z	4
$\overline{\text{RAS}}$ -only refresh current	I_{CC3}	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{\text{RAS}} = V_{IH}$ $\overline{\text{CAS}} = V_{IL}$ Dout = enable	1
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh current	I_{CC6}	—	110	—	100	—	90	mA	$t_{RC} = \text{min}$	
Fast page mode current	I_{CC7}	—	110	—	100	—	90	mA	$t_{PC} = \text{min}$	1, 3
Battery back up operating current (Standby with CBR refresh) (L-version)	I_{CC10}	—	200	—	200	—	200	μA	$t_{RC} = 125 \mu\text{s}$ $t_{RAS} \leq 1 \mu\text{s}$ $\overline{\text{WE}} = V_{IH}$, $\overline{\text{CAS}} = V_{IL}$ Address, Din $= V_{IH}$ or V_{IL} Dout = High-Z	4
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{in} \leq 7 \text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{out} \leq 7 \text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

- Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed twice or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
4. $V_{CC} - 0.2\text{ V} \leq V_{IH} \leq 6.5\text{ V}$ and $0\text{ V} \leq V_{IL} \leq 0.2\text{ V}$

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address, Data-in)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-out)	C_O	—	7	pF	1, 2

- Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS} = V_{IH}$ to disable Dout

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AC Characteristics ($T_a = 0$ to $+70^{\circ}\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$) *1, *12, *15

Test Conditions

Input rise and fall times : 5 ns

Input timing reference levels : 0.8 V, 2.4 V

Output load : 2 TTL gate + C_L (100 pF)

(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	18
$\overline{\text{CAS}}$ pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	19
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	8
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	9
$\overline{\text{RAS}}$ hold time	t_{RSH}	15	—	20	—	20	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	
Refresh period (L-version)	t_{REF}	—	128	—	128	—	128	ms	

Read cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3, 16
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	—	20	—	20	ns	3, 4, 14, 16
Access time from address	t_{AA}	—	30	—	35	—	40	ns	3, 5, 14, 16
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	17
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	17
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	40	—	ns	
Output buffer turn-off time	t_{OFF}	0	15	0	20	0	20	ns	6

Write cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15	—	20	—	20	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	15	—	ns	11

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Read-modify-write cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t _{RWC}	130	—	155	—	175	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	60	—	70	—	80	—	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	15	—	20	—	20	—	ns	10
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	30	—	35	—	40	—	ns	10

Refresh cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ setup time (CBR refresh cycle)	t _{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ hold time (CBR refresh cycle)	t _{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	t _{RPC}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ precharge time in normal mode	t _{CPN}	10	—	10	—	10	—	ns	

Fast page mode cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t _{PC}	40	—	45	—	50	—	ns	
Fast page mode $\overline{\text{CAS}}$ precharge time	t _{CP}	10	—	10	—	10	—	ns	
Fast page mode $\overline{\text{RAS}}$ pulse width	t _{RASC}	—	100000	—	100000	—	100000	ns	13
Access time from $\overline{\text{CAS}}$ precharge	t _{ACP}	—	35	—	40	—	45	ns	3, 14, 16
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	35	—	40	—	45	—	ns	

Fast page mode read-modify-write cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode read-modify-write cycle time	t _{PCM}	60	—	70	—	75	—	ns	
CAS precharge to $\overline{\text{WE}}$ delay time	t _{CPW}	35	—	40	—	45	—	ns	10

Test mode cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Test mode $\overline{\text{WE}}$ setup time	t _{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{\text{WE}}$ hold time	t _{WH}	10	—	10	—	10	—	ns	

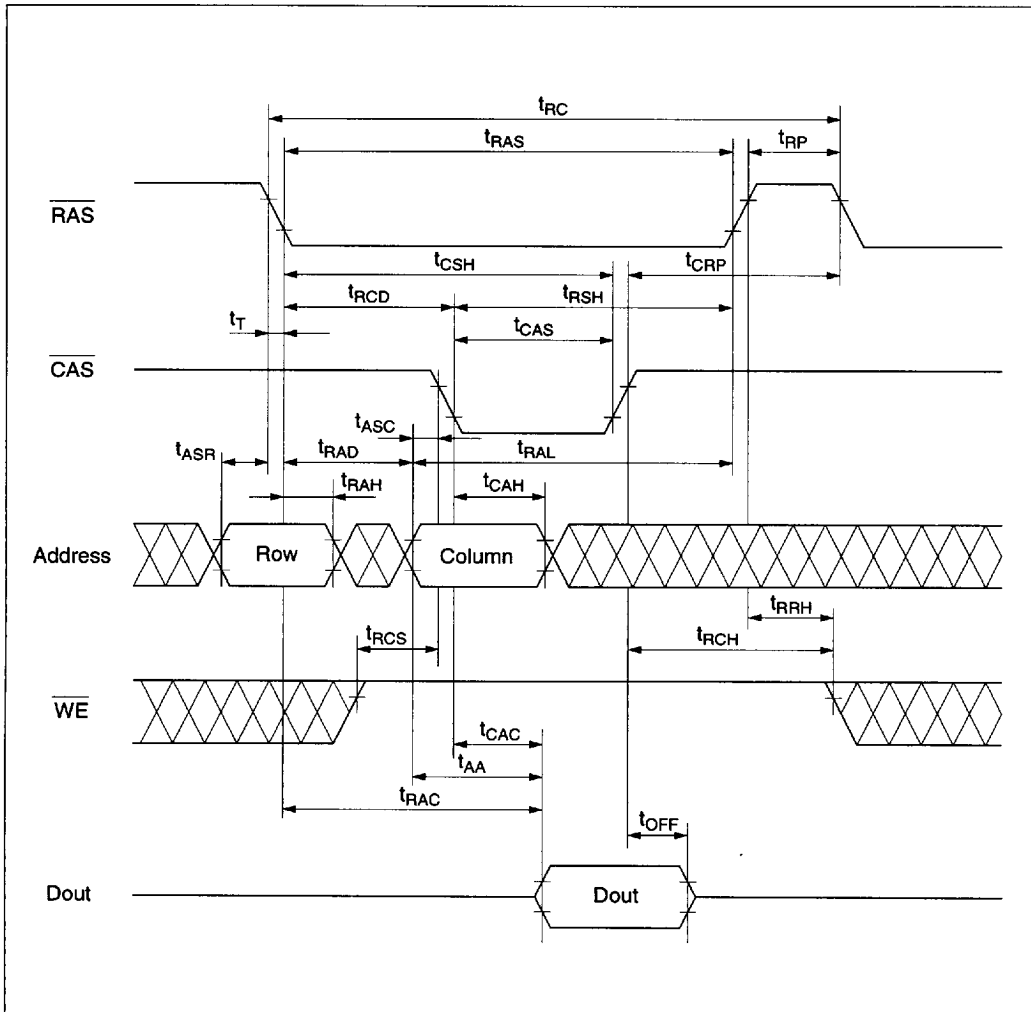
Counter test cycle

Parameter	Symbol	HM514100 B/BL-6		HM514100 B/BL-7		HM514100 B/BL-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CAS precharge time in counter test cycle	t _{CPT}	40	—	40	—	40	—	ns	

- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or read-modify-write cycle.
 12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 13. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits - - - RA10, CA10 and CA0. This test mode operation can be performed by $\overline{\text{WE}}$ -and- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle or a $\overline{\text{RAS}}$ -only refresh cycle.
 16. In a test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
 17. Either t_{RCH} or t_{RRH} must be satisfied
 18. $t_{RAS}(\text{min}) = t_{RWD}(\text{min}) + t_{RWL}(\text{min}) + t_T$ in read-modify-write cycle
 19. $t_{CAS}(\text{min}) = t_{CWD}(\text{min}) + t_{CWL}(\text{min}) + t_T$ in read-modify-write cycle

Timing Waveforms *20

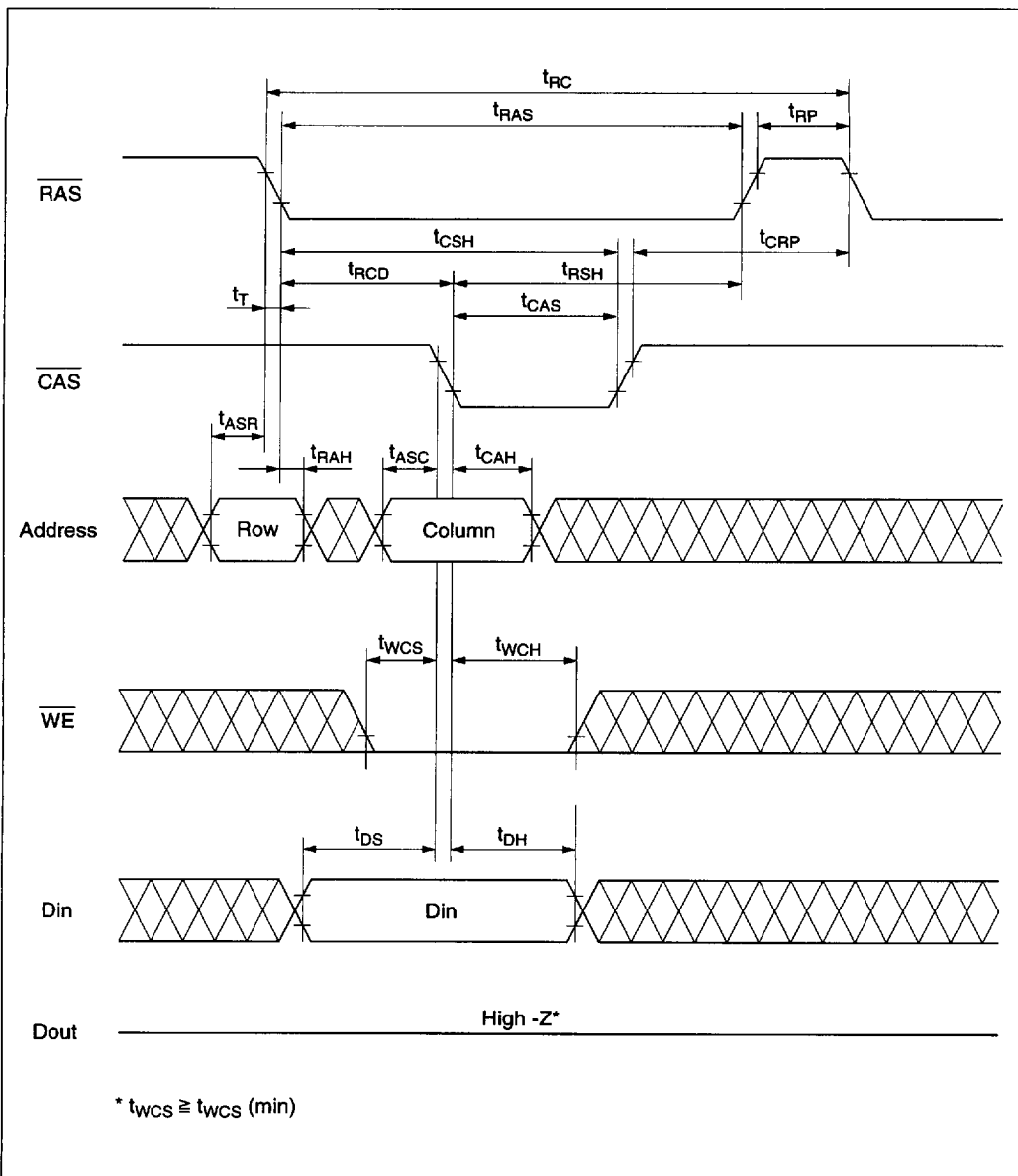
Read Cycle



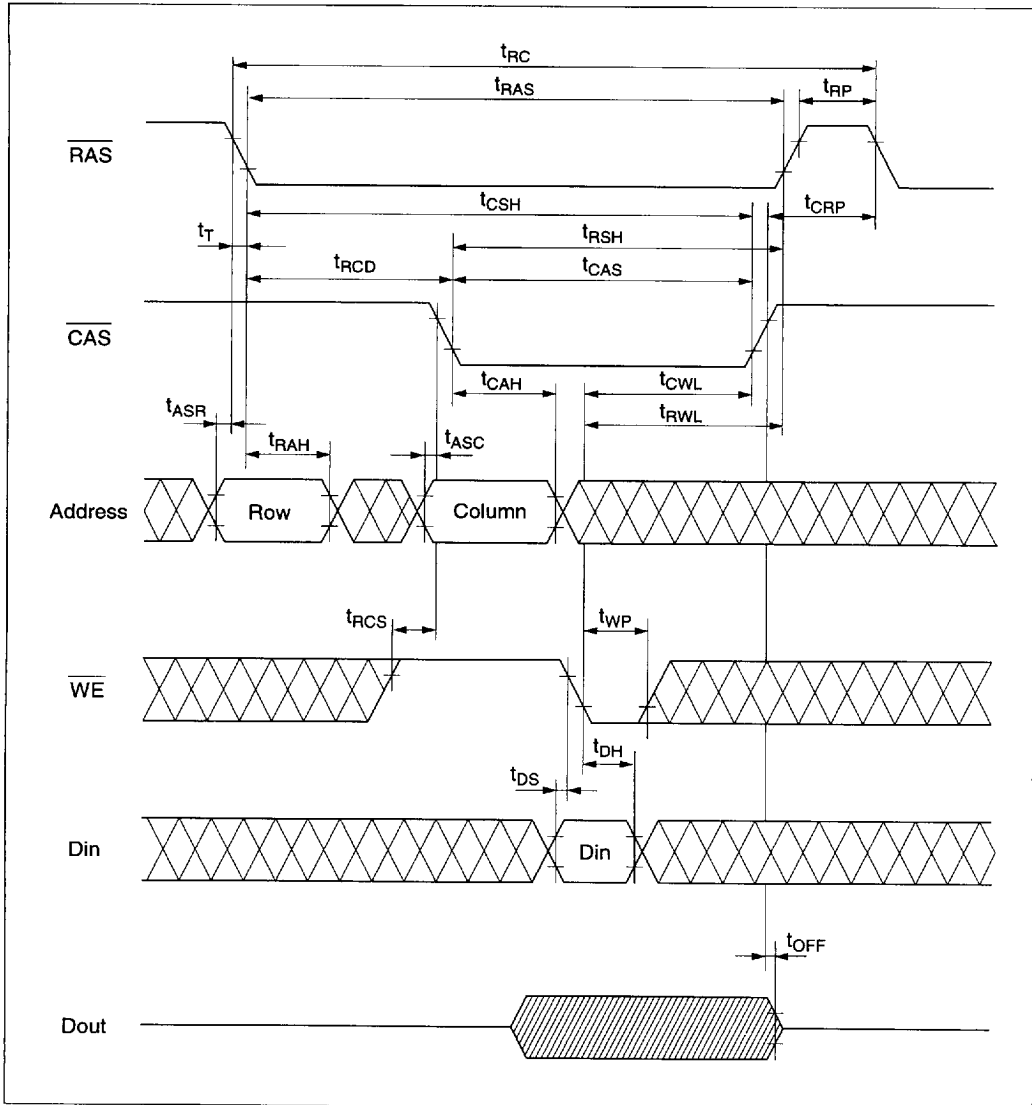
Notes: 20.  : H or L (H : $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L : $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)
 : Invalid Dout

HM514100B/BL Series

Early Write Cycle

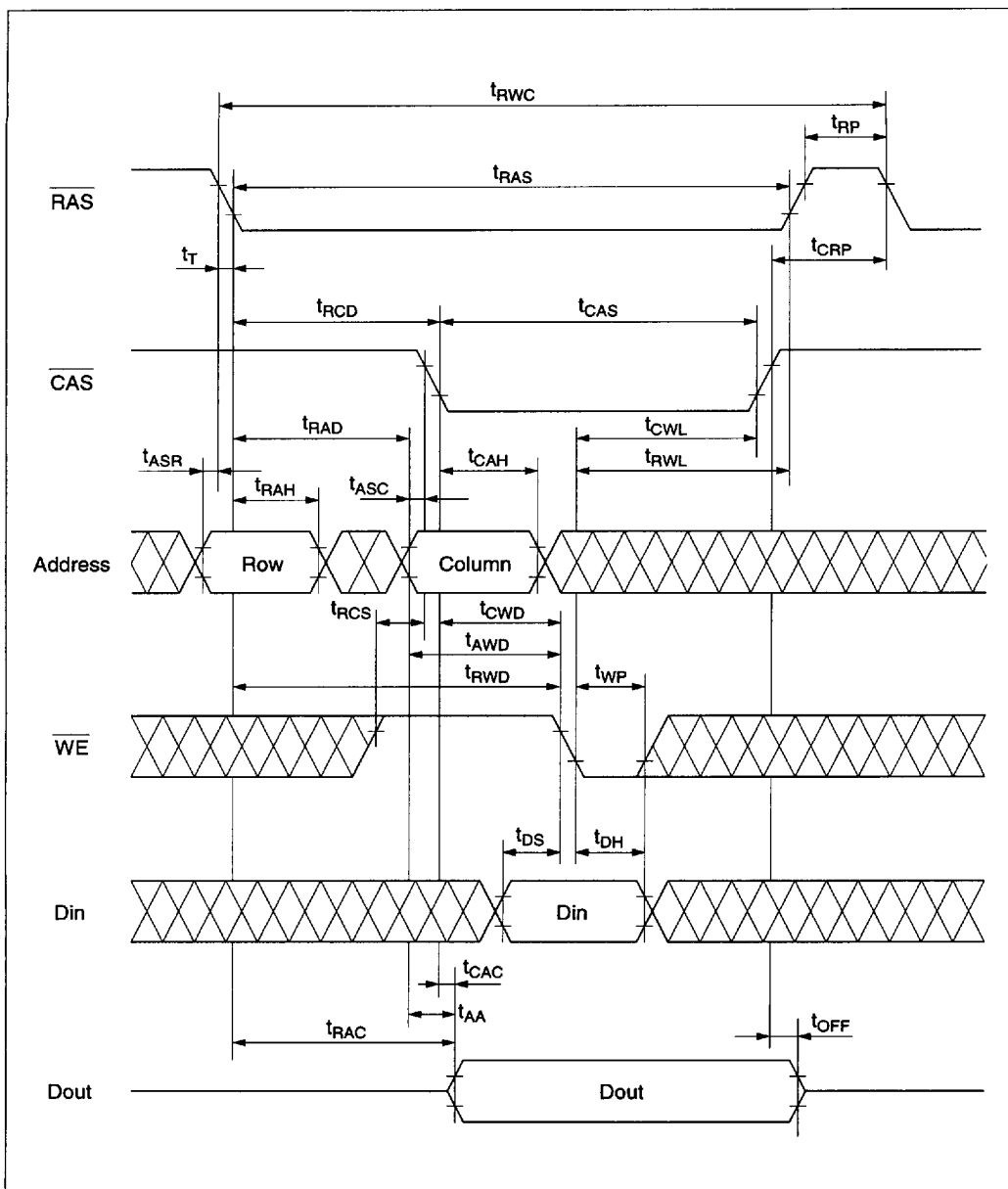


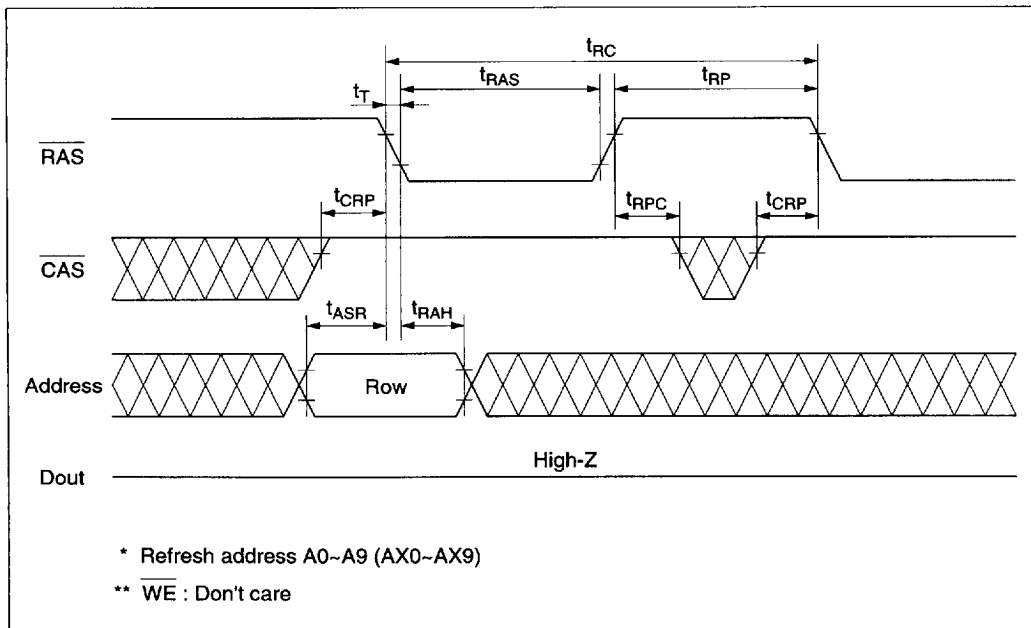
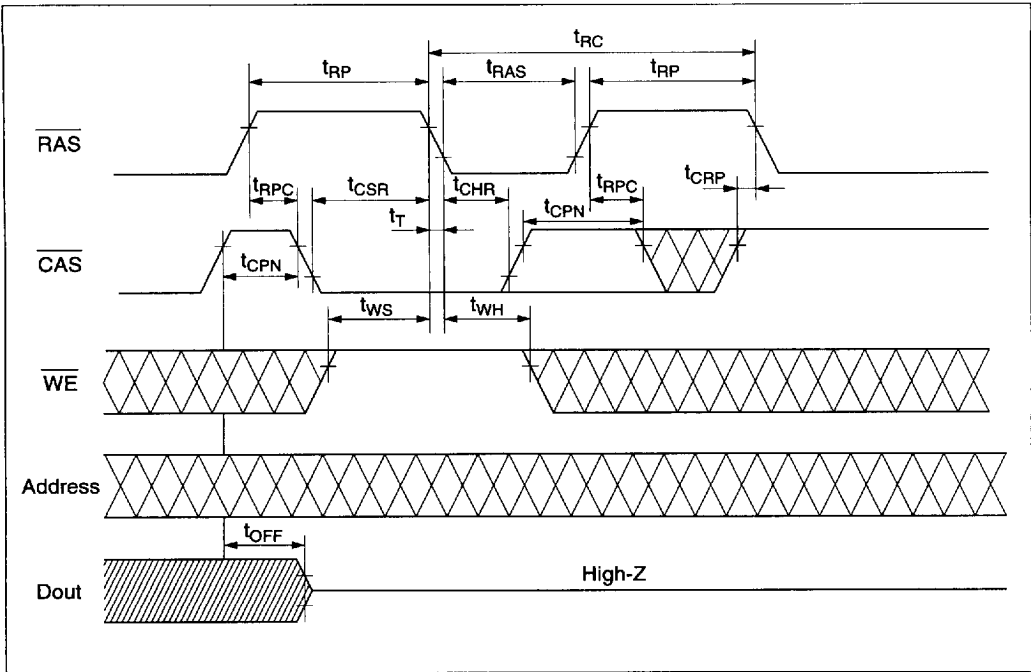
Delayed Write Cycle



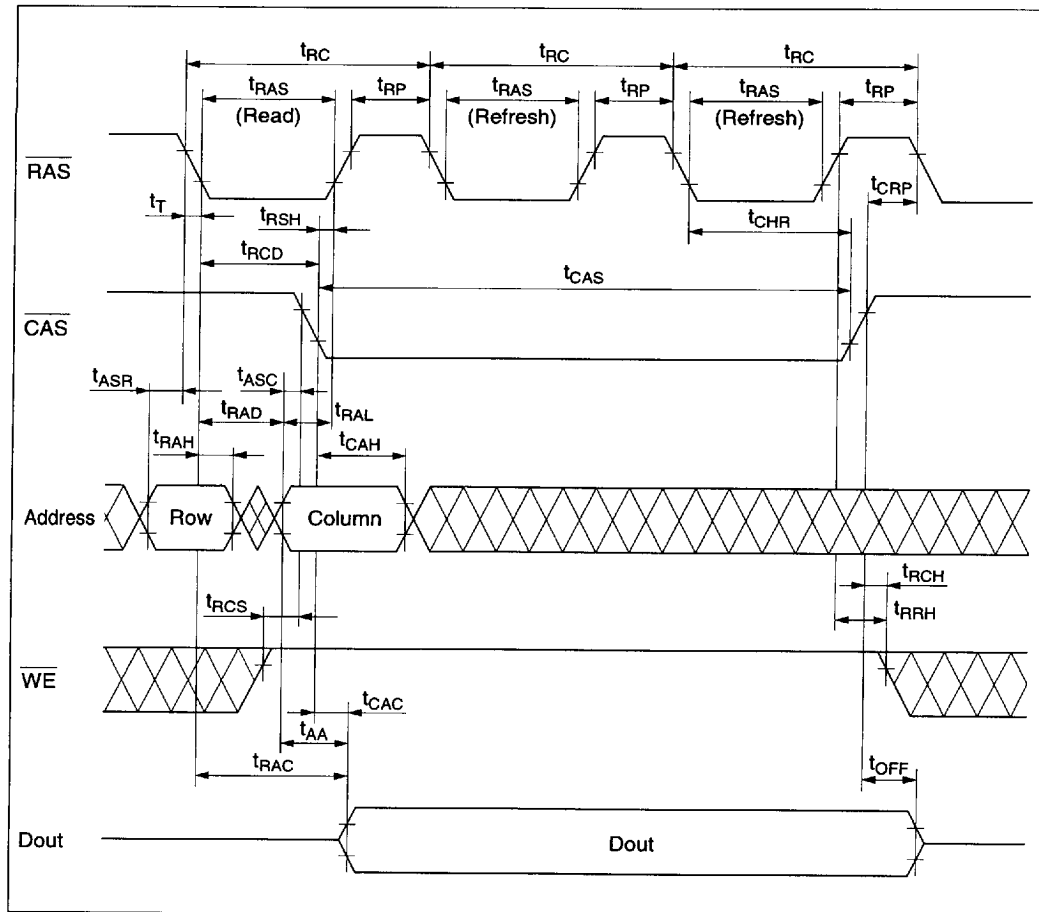
HM514100B/BL Series

Read-Modify-Write Cycle

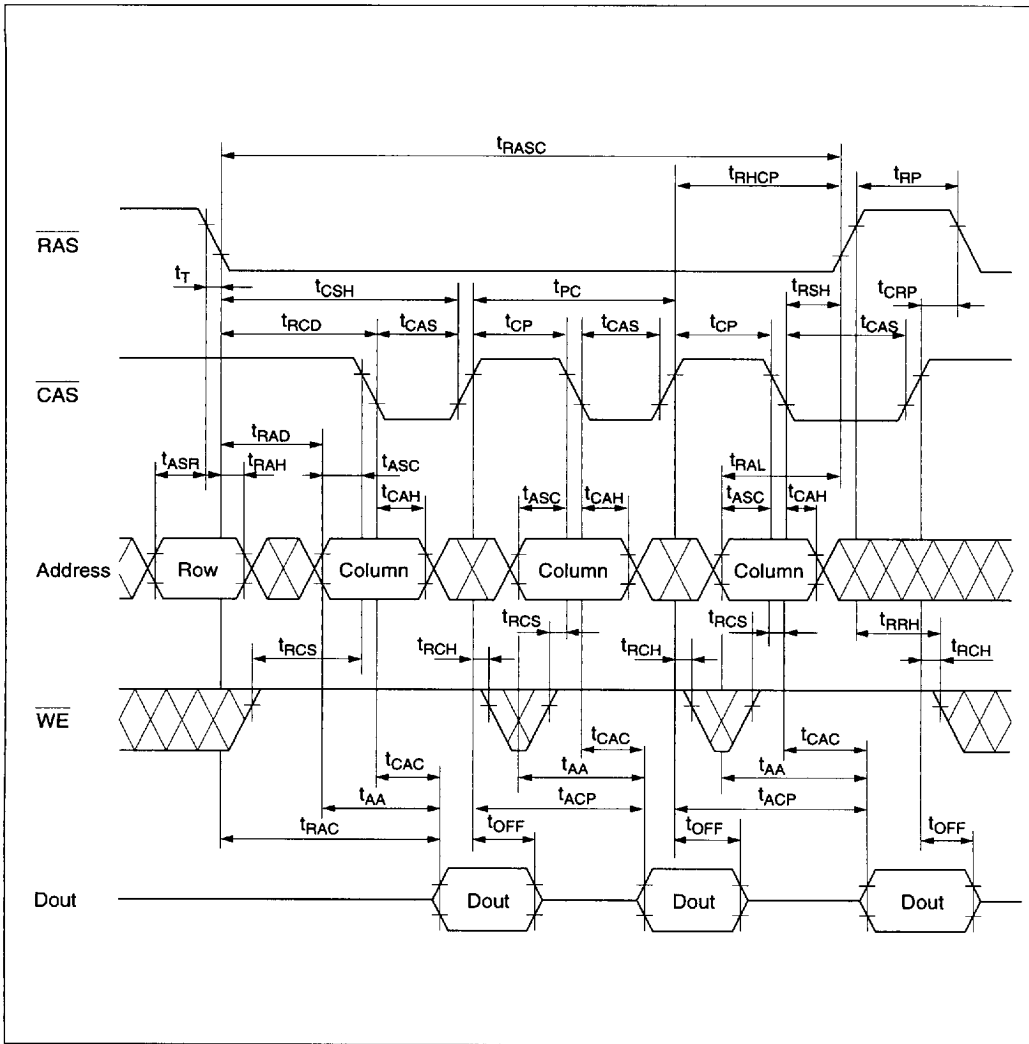




Hidden Refresh Cycle



Fast Page Mode Read Cycle

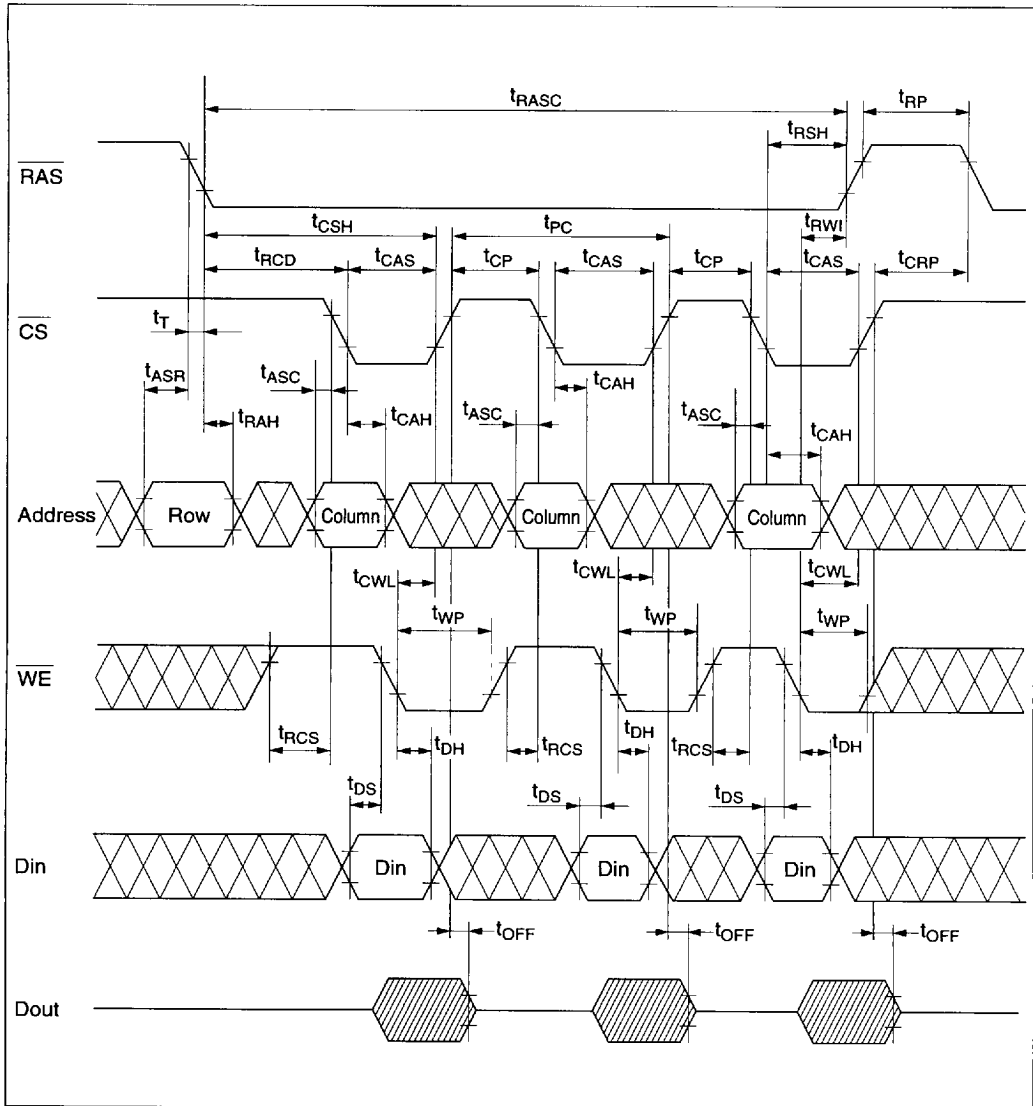


Fast Page Mode Early Write Cycle



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Fast Page Mode Delayed Write Cycle

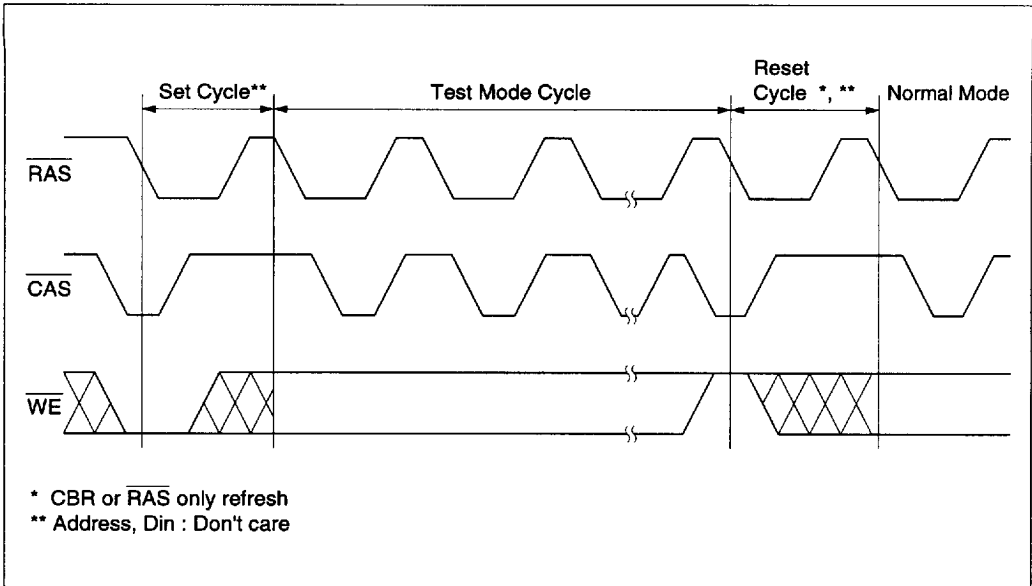


Fast Page Mode Read-Modify-Write Cycle



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Test Mode Cycle



Test Mode Set Cycle

