LH538500C

CMOS 8M (1M × 8/512K × 16)
Mask-Programmable ROM

FEATURES

- 1,048,576 words × 8 bit organization
  (Byte mode)
  524,288 words × 16 bit organization
  (Word mode)
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH538500C is an 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

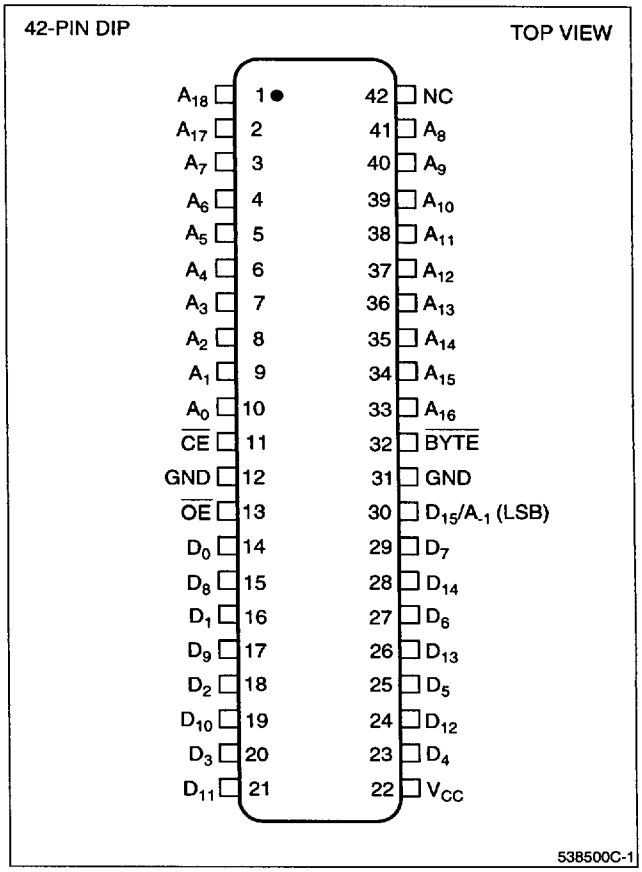


Figure 1. Pin Connections for DIP Package

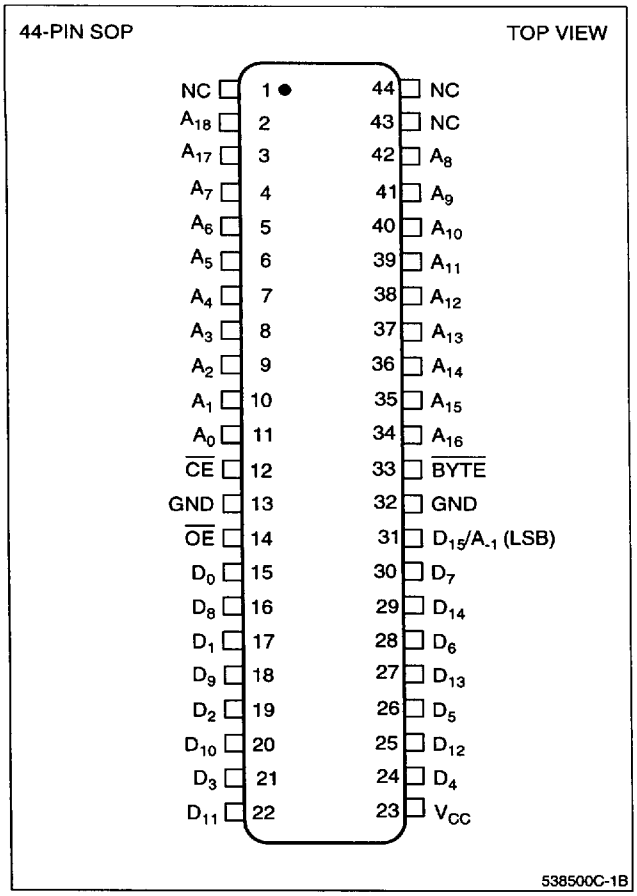


Figure 2. Pin Connections for SOP Package

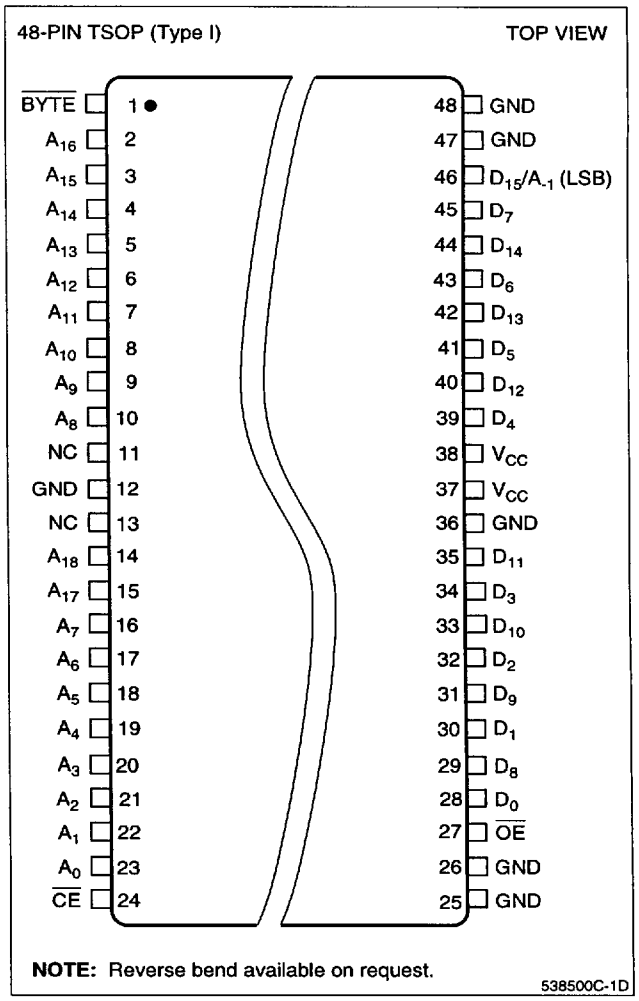


Figure 3. Pin Connections for TSOP (Type I) Package

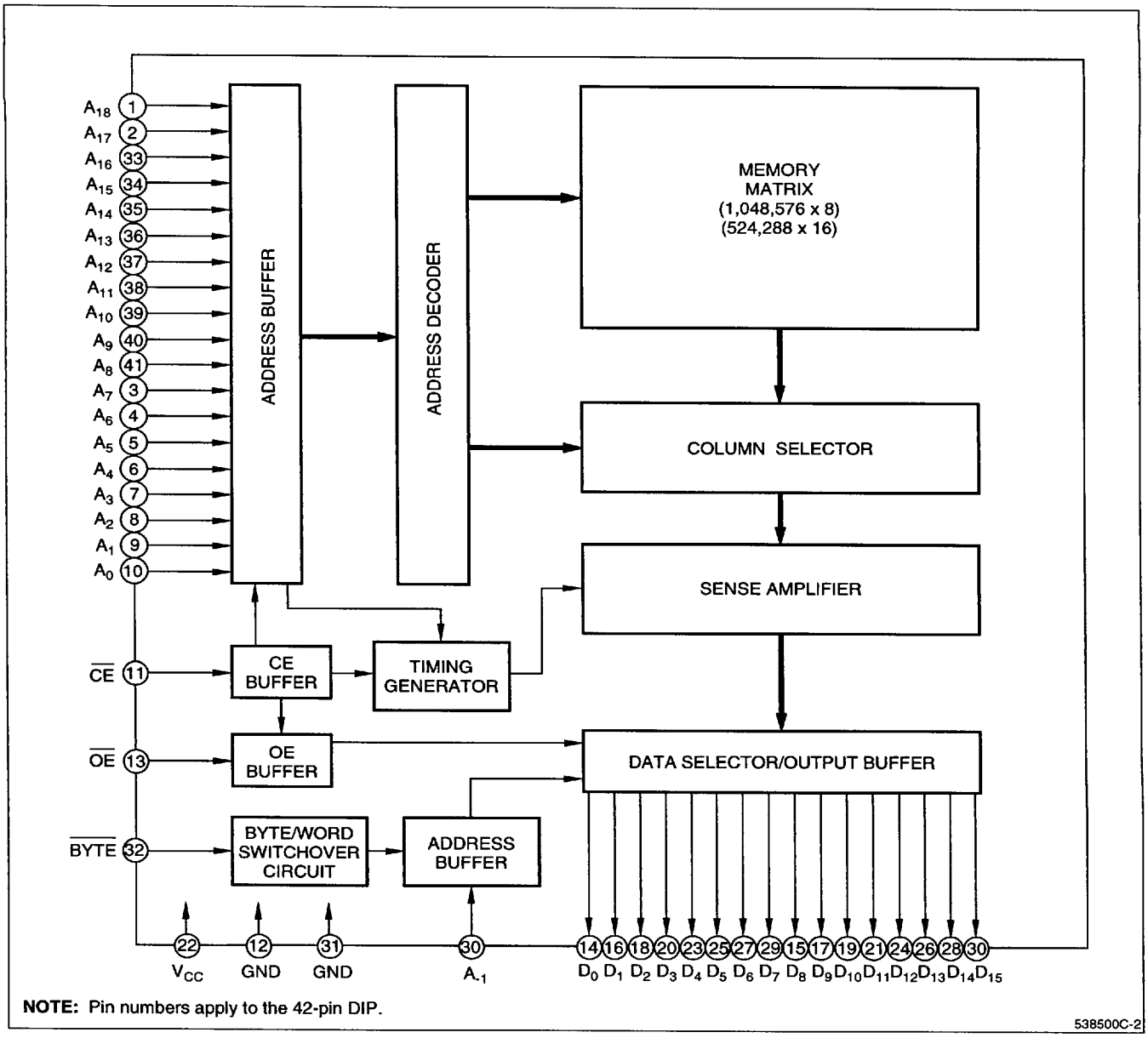


Figure 4. LH538500C Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
$A_{-1} - A_{18}$	Address input	1
$D_0 - D_{15}$	Data output	1
$\overline{BYTE}$	Byte/word mode switch	1
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output enable input	
V_{CC}	Power supply (+5 V)	
GND	Ground	
NC	No connection	

NOTE:

1. The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be LOW in byte mode, and data output (D_{15}) when set to be HIGH in word mode.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT	NOTE
				$D_0 - D_7$	$D_8 - D_{15}$	LSB	MSB		
H	X	X	X	High-Z	High-Z	–	–	Standby (I_{SB})	1
L	H	X	X	High-Z	High-Z	–	–	Operating (I_{CC})	1
L	L	H	–	$D_0 - D_7$	$D_8 - D_{15}$	A_0	A_{18}	Operating (I_{CC})	
L	L	L	L	$D_0 - D_7$	High-Z	A_{-1}	A_{18}	Operating (I_{CC})	
L	L	L	H	$D_8 - D_{15}$	High-Z	A_{-1}	A_{18}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		−0.3		0.8	V	
Input 'High' voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = −400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} − 0.2 V			100	µA	
Input capacitance	C_{IN}	f = 1 MHz, T_A = 25°C			10	pF	
Output capacitance	C_{OUT}				10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH} or V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable delay time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			60	ns	1
OE to output in High-Z	t_{OHZ}			60	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

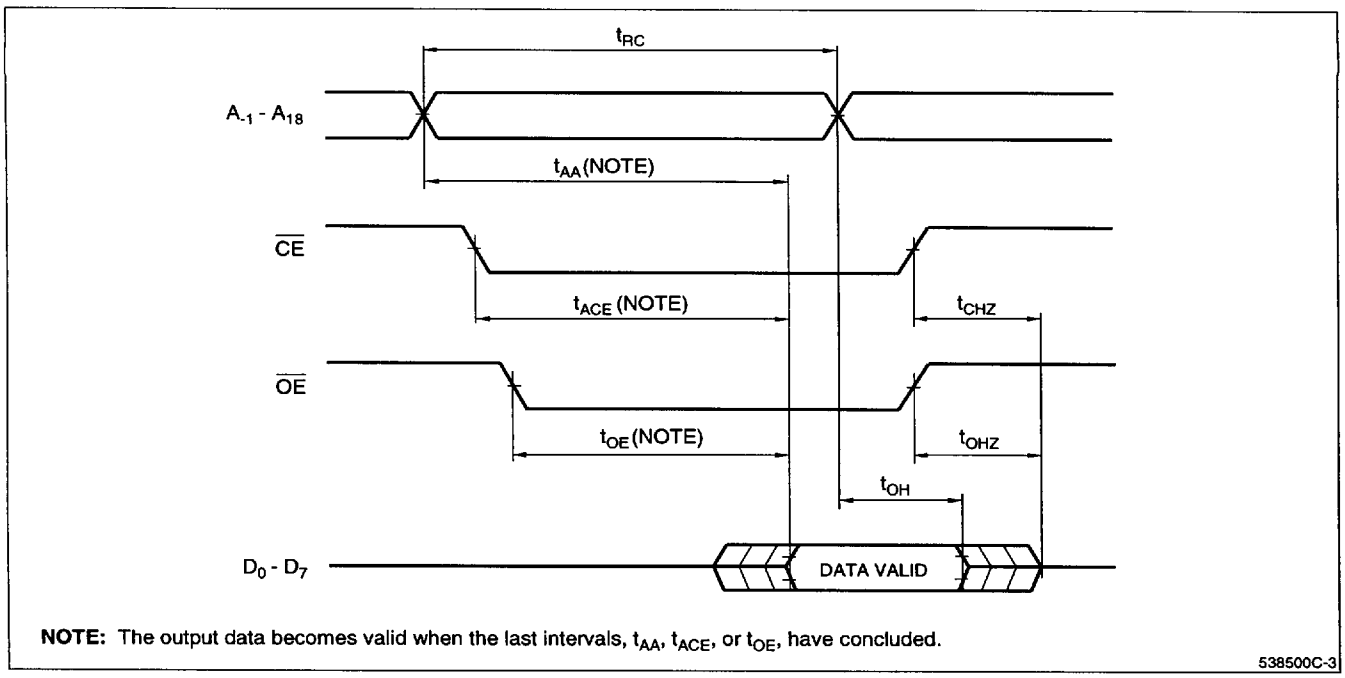


Figure 5. Byte Mode ($\overline{BYTE}$ = V_{IL})

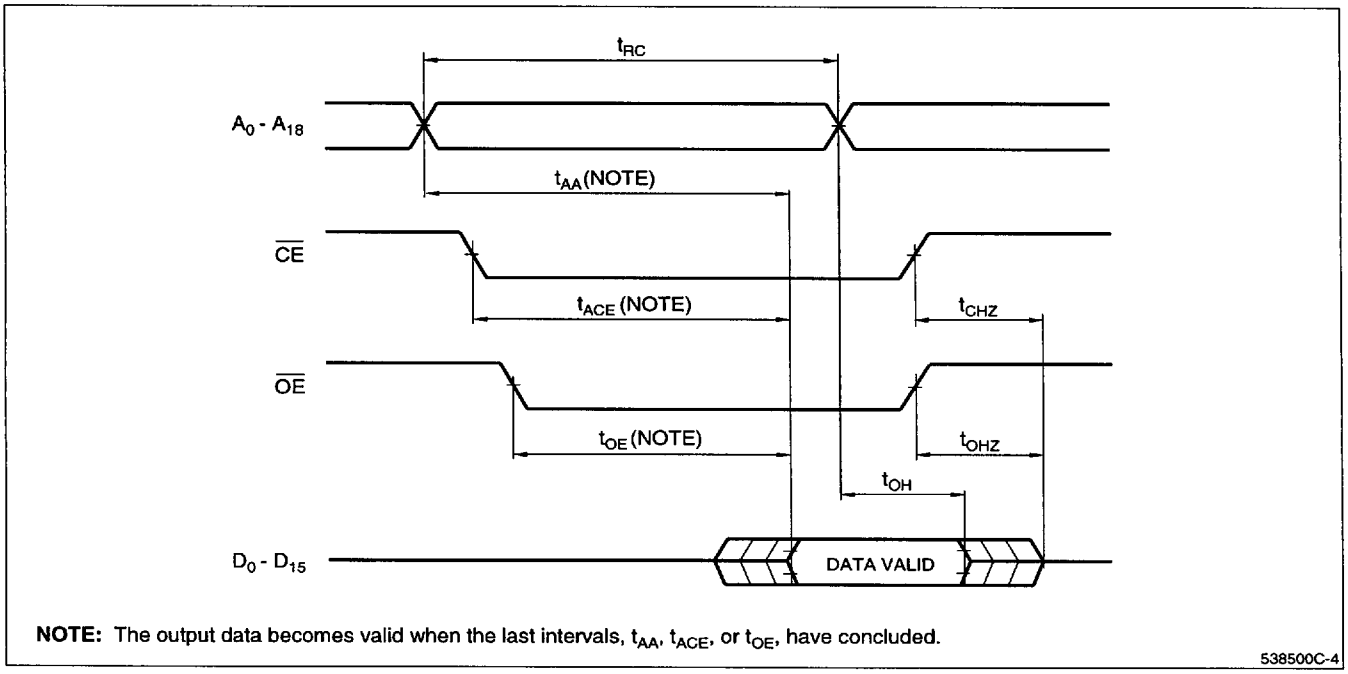
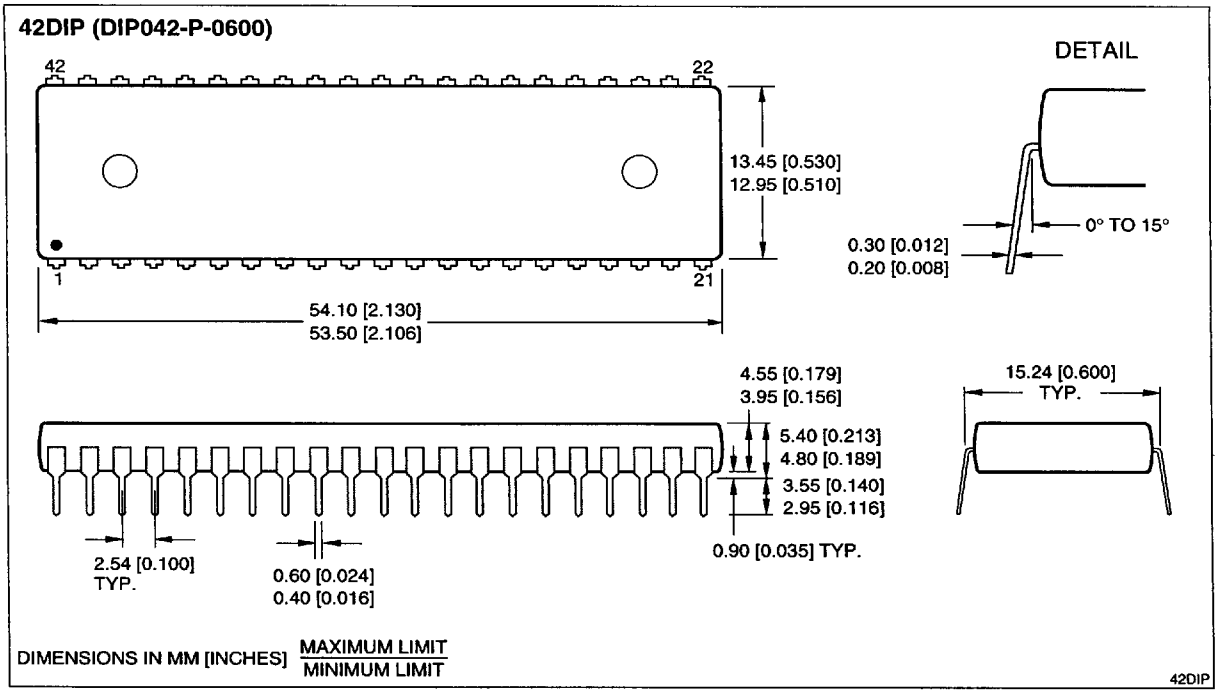
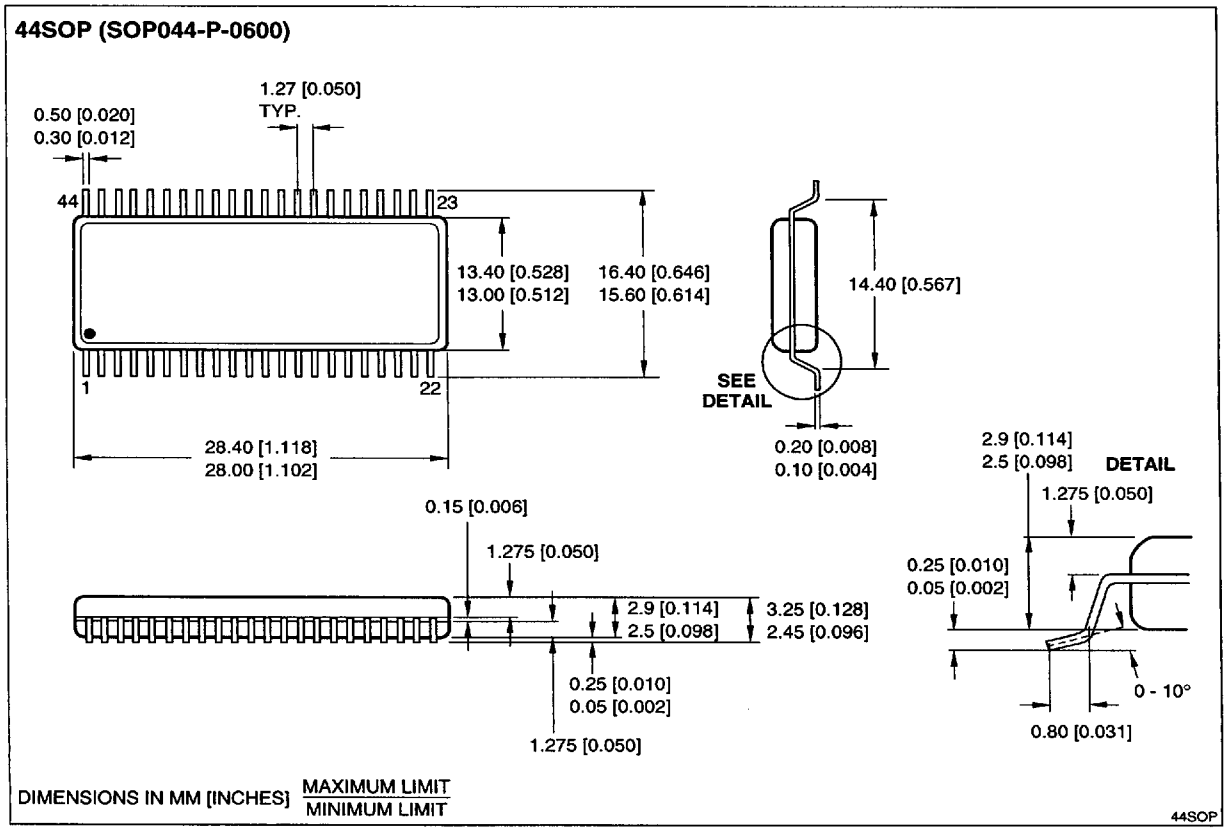


Figure 6. Word Mode ($\overline{BYTE}$ = V_{IH})

PACKAGE DIAGRAMS

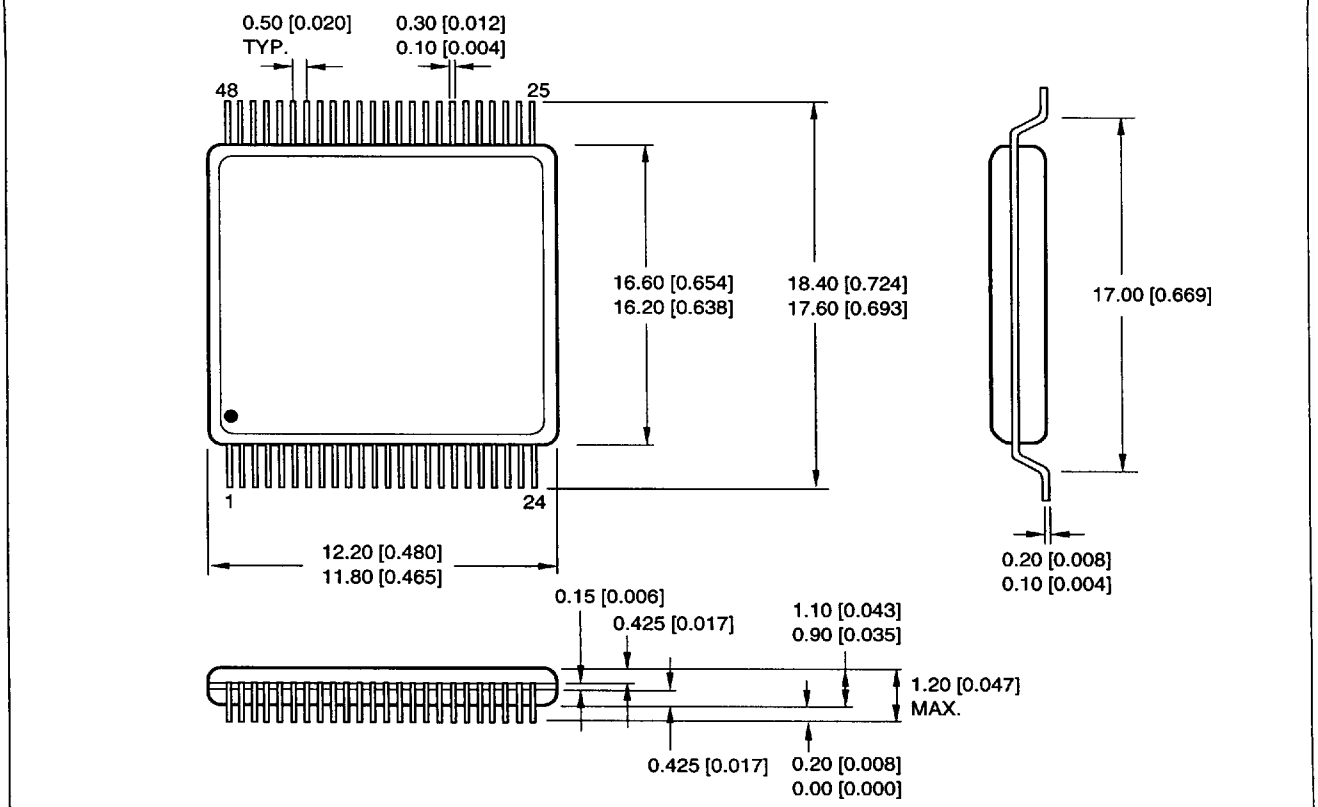


42-pin, 600-mil DIP



44-pin, 600-mil SOP

48TSOP (TSOP048-P-1218)



48-pin, 12 × 18 mm² TSOP (Type I)

ORDERING INFORMATION

LH538500C — Device Type

X — Package

- D 42-pin, 600-mil DIP (DIP042-P-0600)
- N 44-pin, 600-mil SOP (SOP044-P-0600)
- T 48-pin, 12 x 18 mm² TSOP (Type I) (TSOP048-P-1218)
- TR 48-pin, 12 x 18 mm² TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 8M (1M x 8 or 512K x 16) Mask-Programmable ROM

Example: LH538500CD (CMOS 8M (1M x 8 or 512K x 16) Mask-Programmable ROM, 42-pin, 600-mil DIP)

538500C-5