LH5P8512

PRELIMINARY

CMOS 4M (512K × 8) Pseudo-Static RAM

FEATURES

- 524,288 × 8 bit organization
- Access time: 60/70/80 ns (MAX.)
- Cycle time: 110/130/150 ns (MIN.)
- Power supply:
  5 V ± 10% for operation
  3.0 V to 5.5 V for data retention
- Power consumption:
  Operating: 500 mW (MAX.)
  Standby: 550 µW (MAX.)
  Self refresh:
  550 µW (MAX.) V_{CC} = 5.5 V
  275 µW (MAX.) V_{CC} = 3.0 V
- TTL compatible I/O
- Available for address refresh, auto-refresh and self-refresh modes
- 2,048 refresh cycles/32 ms
- Non-multiplexed address input
- Read-Modify-Write capability
- Compatible with JEDEC standard 4M SRAM pinout
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 400-mil TSOP II *
  (normal/reverse bend pins)

DESCRIPTION

The LH5P8512 is a 4M bit Pseudo-Static RAM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo-static operation which eliminates external clock inputs, while having the same pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, existing 512K × 8 SRAM sockets can be filled with the LH5P8512 with little changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8512 PSRAM can be used for data memory of compact systems such as palm-top terminal equipment, electronic organizers and notebook personal computers, in place of a low power SRAM, or a slow-refresh DRAM, by offering low cost, low power standby, high density and simple interface.

* Consult factory for availability.

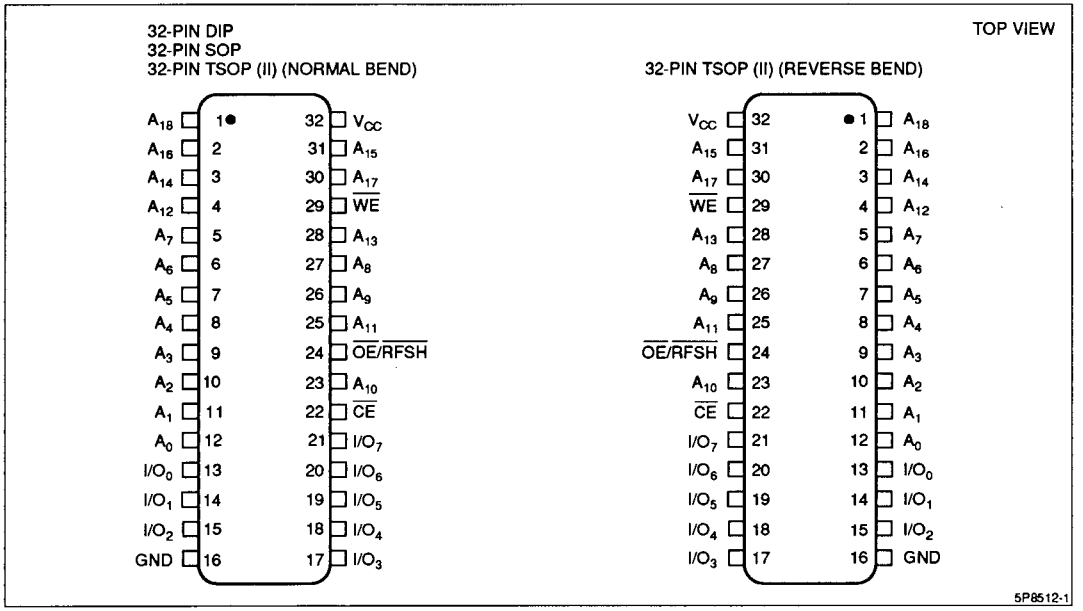


Figure 1. Pin Connections for DIP, SOP and TSOP II Packages

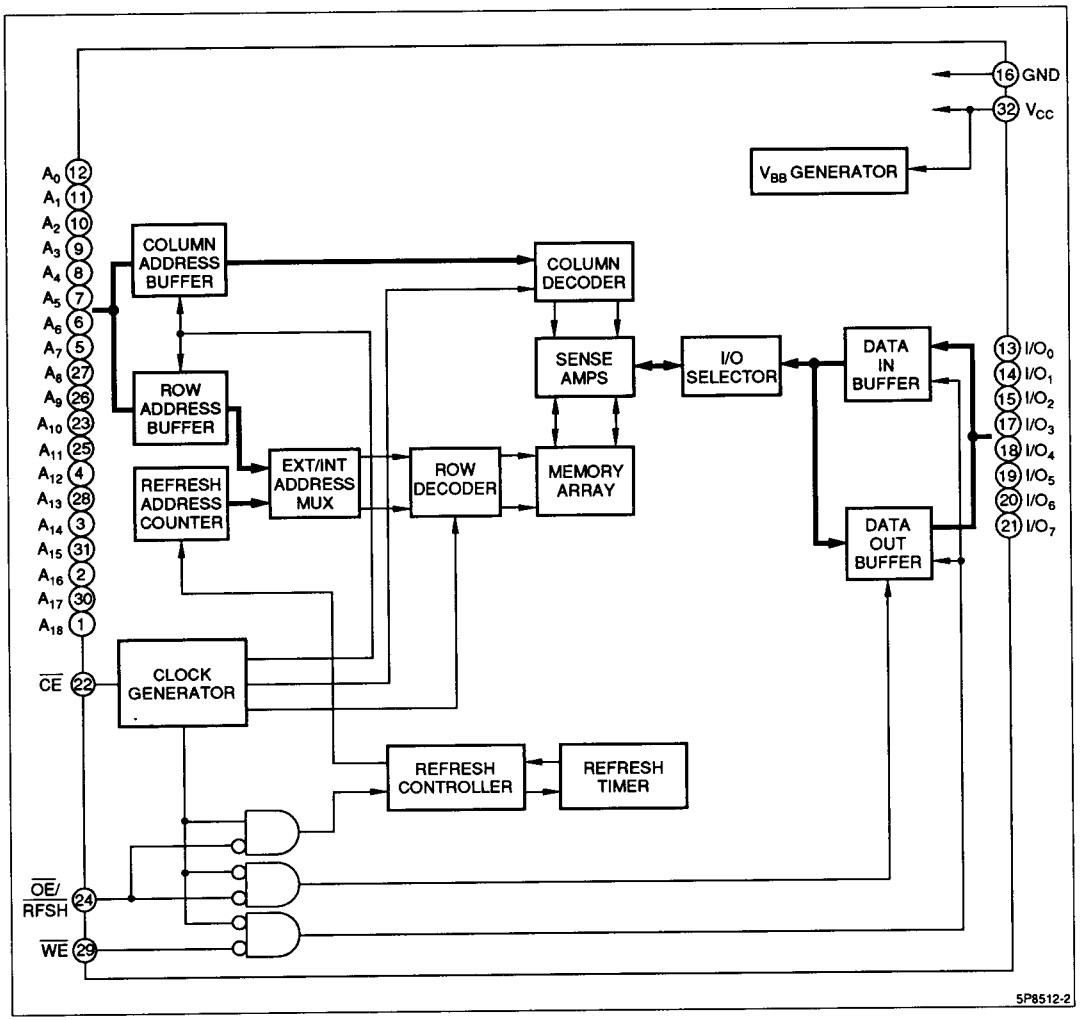


Figure 2. LH5P8512 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{18}	Address input
$\overline{WE}$	Write Enable input
$\overline{OE}/\overline{RFSH}$	Output Enable input/Refresh input

SIGNAL	PIN NAME
$\overline{CE}$	Chip Enable input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power consumption	P_D	1	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		6.5	V
	V_{IL}	1.0		0.8	V

DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LH5P8512-60L		UNIT	NOTE
			MIN.	MAX.		
Operating current	I_{CC1}	tRC = t_{RC} (MIN.)		100	mA	1,2
Standby current	I_{CC2}	$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{IH} (MIN.)		1.0	mA	1,2
		$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{CC} - 0.2 V		100	µA	1
Address refresh average current	I_{CC3}	VIH (MIN.)/V_{IL} (MAX.) on all inputs, t_{RC} = 15.625 µs		1.5	mA	1
		V_{CC} - 0.2 V/0.2 V on all inputs, t_{RC} = 15.625 µs		600	µA	1,2
Auto refresh average current	I_{CC4}	VIH (MIN.)/V_{IL} (MAX.) on all inputs, t_{FC} = 15.625 µs		1.5	mA	1,2
		V_{CC} - 0.2 V/0.2 V on all inputs, t_{FC} = 15.625 µs		600	µA	1,2
Self refresh average current	I_{CC5}	$\overline{CE}$ = V_{IH} (MIN.), $\overline{OE}$/$\overline{RFSH}$ = V_{IL} (MAX.), V_{CC} = 5.5 V		1.0	mA	1,2
		$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{OE}$/$\overline{RFSH}$ = 0.2 V, V_{CC} = 5.5 V		100	µA	1
		$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{OE}$/$\overline{RFSH}$ = 0.2 V, V_{CC} = 3.0 V		50	µA	1
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V, 0 V on all other test pins	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ 6.5 V, Outputs in High-Z state	-10	10	µA	
Output HIGH voltage	V_{OH}	I_{OH} = -1.0 mA	2.4		V	
Output LOW voltage	V_{OL}	I_{OL} = 2.1 mA		0.4	V	
Data retention voltage	V_R		3.0	5.5	V	

NOTES:

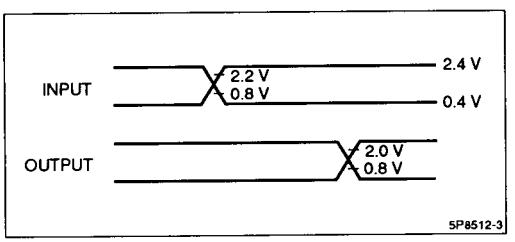
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC2}, I_{CC3} and I_{CC4} depend on the cycle time.

AC CHARACTERISTICS [1,2,3,4] (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER	SYMBOL	LH5P8512-60L		UNIT	NOTE
		MIN.	MAX.		
Random read, write cycle time	t_{RC}	110		ns	
Read modify write cycle time	t_{RMW}	165		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	ns	
$\overline{CE}$ precharge time	t_P	40		ns	
Address setup time	t_{AS}	0		ns	
Address hold time	t_{AH}	15		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
$\overline{CE}$ access time	t_{CEA}		60	ns	
$\overline{OE}$ access time	t_{OEA}		30	ns	
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		ns	
Chip disable to output in High-Z	t_{CHZ}	0	20	ns	5
Output disable to output in High-Z	t_{OHZ}	0	20	ns	5
Write enable to output in High-Z	t_{WHZ}	0	20	ns	5
$\overline{OE}$ setup time	t_{OES}	0		ns	
$\overline{OE}$ hold time	t_{OEH}	15		ns	
Write command pulse width	t_{WP}	20		ns	
Write command setup time	t_{WCS}	20	10,000	ns	
Write command hold time	t_{WCH}	60	10,000	ns	
Data setup time from write	t_{DSW}	20		ns	
Data setup time from $\overline{CE}$	t_{DSC}	20		ns	
Data hold time from write	t_{DHW}	0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		ns	
Transition time (rise and fall)	t_T	3	50	ns	
Refresh time interval	t_{REF}		32	ms	
Auto refresh cycle time	t_{FC}	110		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	15		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	ns	6
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	6
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	6
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		ns	6
V_{CC} recovery time after data retention	t_R	5		ms	

NOTES:

1. In order to initialize the circuit, $\overline{CE}$ should be kept in V_{IH} for 100 µs after power-up.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right):
4. Measured with a load equivalent to 1TTL + 100 pF.
5. t_{CHZ}, t_{OHZ}, and t_{WHZ} define the time at which the output achieve the open circuit condition and are not referenced to output voltage levels.
6. Auto refresh and self refresh are defined by $\overline{RFSH}$ pulse width during $\overline{CE}$ = V_{IH}. If $\overline{RFSH}$ pulse width is less than t_{FAP} (MAX.), the cycle is an auto refresh cycle and memory cells are refreshed by the internal counter. If $\overline{RFSH}$ pulse width is more than t_{FAS} (MIN.), the cycle is a self refresh cycle and memory cells are refreshed by the internal clock automatically.



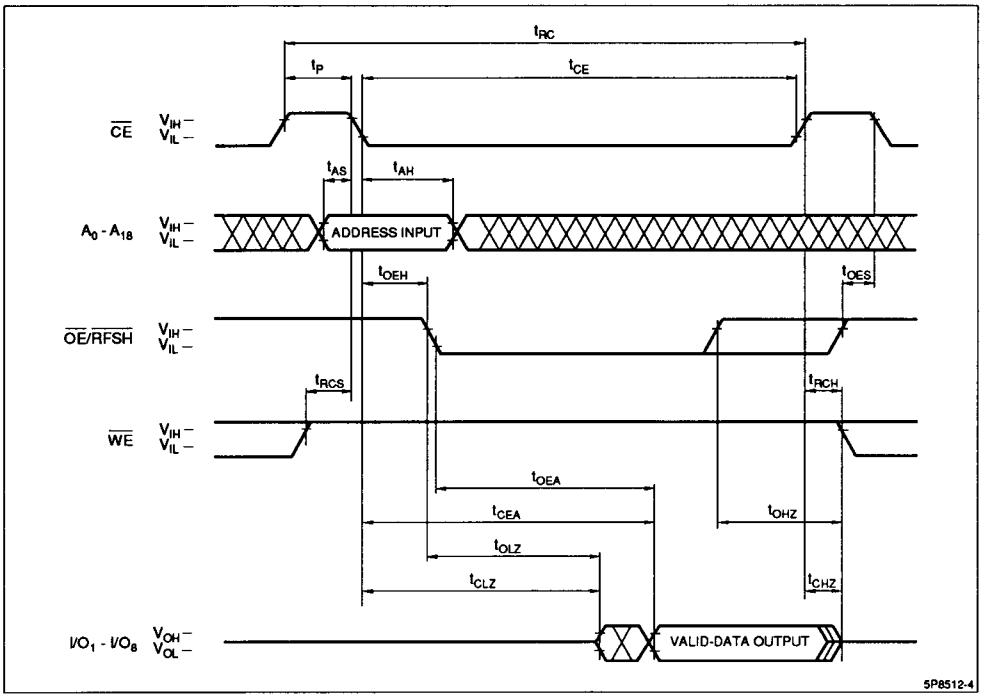


Figure 3. Read Cycle

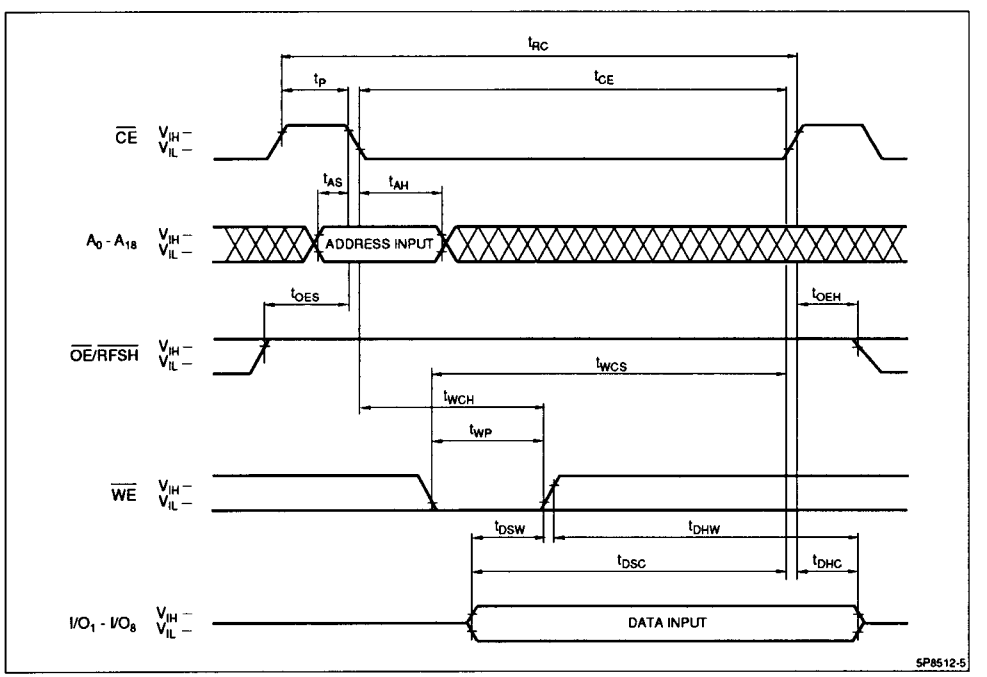


Figure 4. Write Cycle

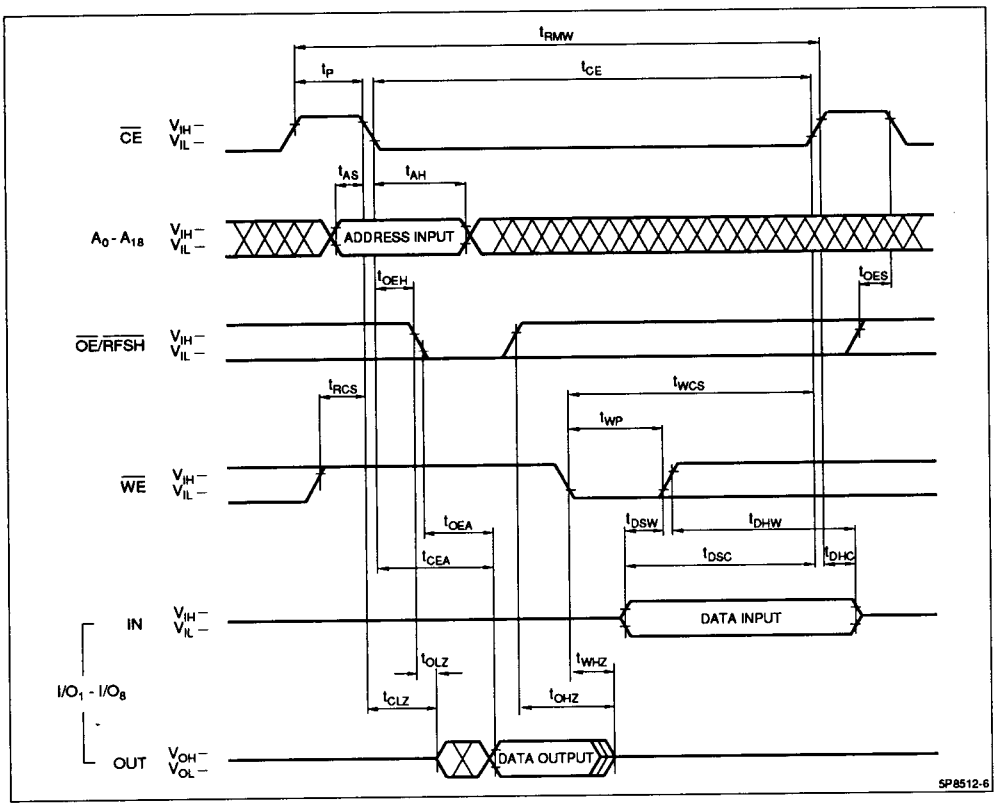


Figure 5. Read Write/Read-Modify-Write Cycle

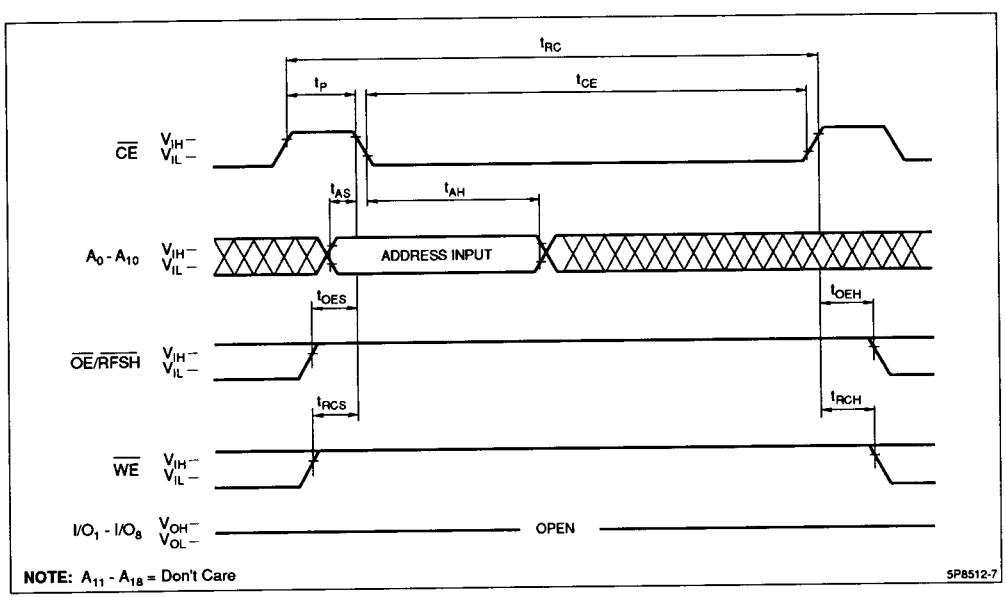


Figure 6. Address Refresh Cycle

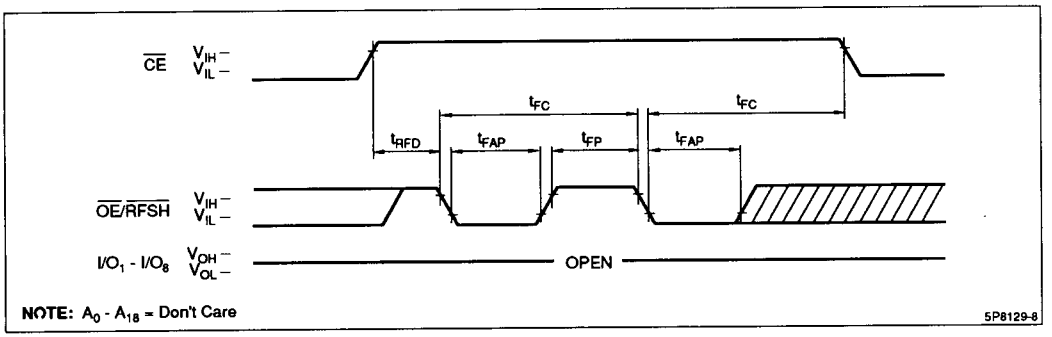


Figure 7. Auto Refresh Cycle

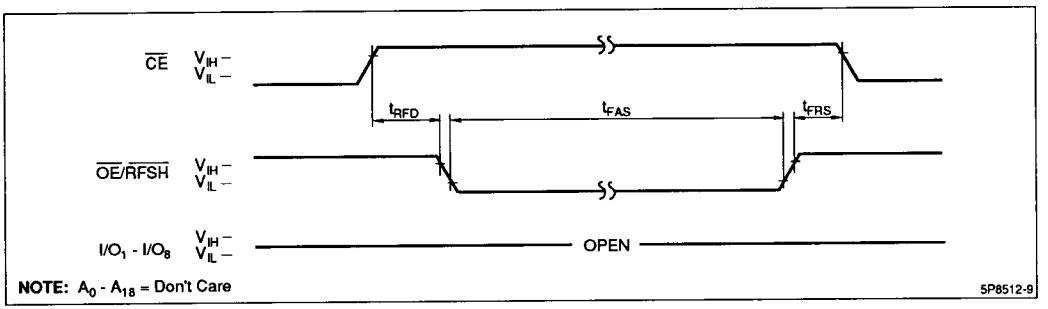


Figure 8. Self Refresh Cycle

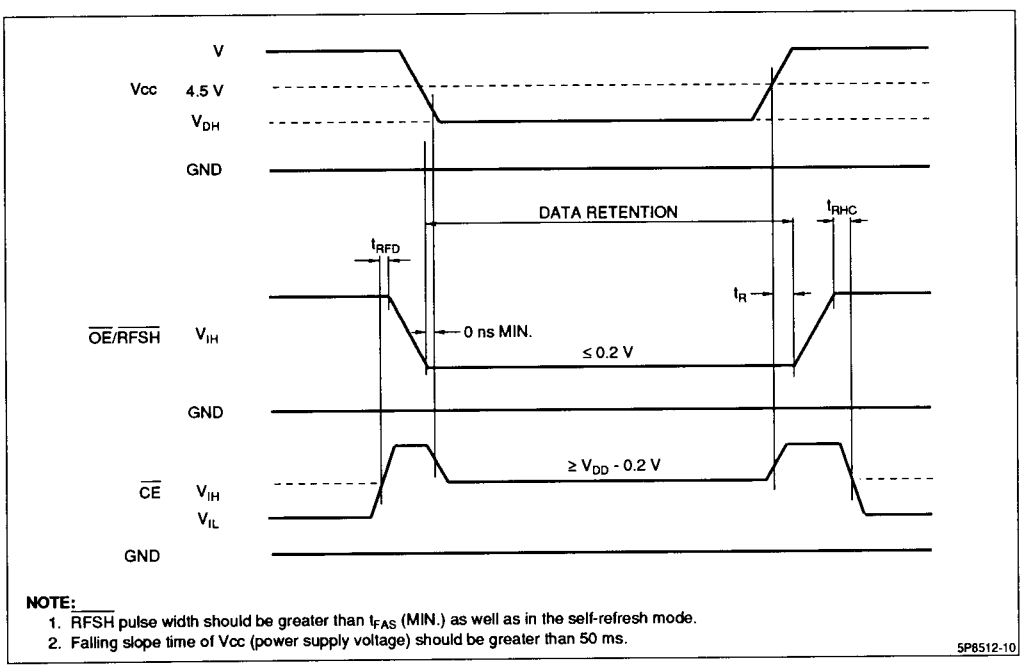
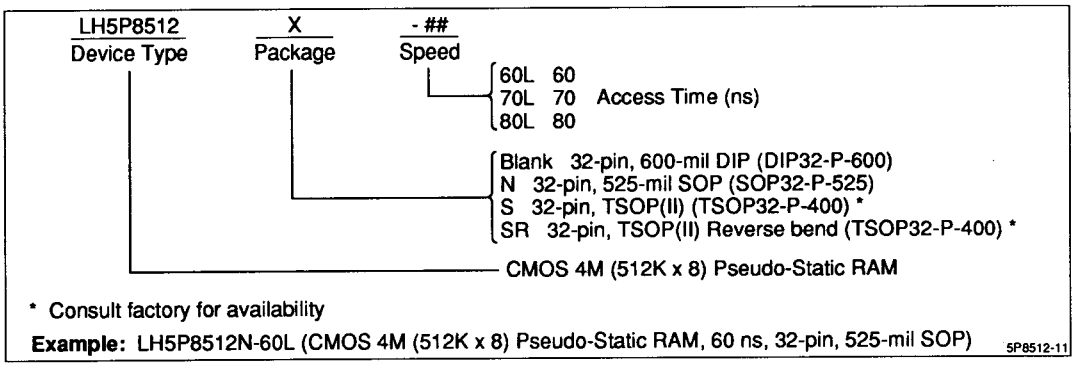


Figure 9. Data Retention Mode

ORDERING INFORMATION



* Consult factory for availability

Example: LH5P8512N-60L (CMOS 4M (512K x 8) Pseudo-Static RAM, 60 ns, 32-pin, 525-mil SOP) 5P8512-11