MT88E46

Bellcore Compliant Calling Number Identification Circuit

Advance Information

DS5350 ISSUE 1 March 2000

Ordering Information

MT88E46AS 20 Pin SOIC

-40 to +85 °C

Features

- Compatible with Bellcore GR-30-CORE, SR-TSV-002476; TIA/EIA-716 and TIA/EIA-777
- Pin compatible with MT88E45
- Differential input amplifiers with adjustable gains for Tip/Ring and 4-wire side connections
- TIA (Telecommunications Industry Association) MEI (Multiple Extension Interworking) compatible architecture: CAS (CPE Alerting Signal) detection is selectable between Tip/Ring and 4-wire side
- 4-wire side CAS detection is Bellcore talkoff and talkdown compliant when near end speech is attenuated 8dB or better, and is close to talkoff compliant even without near end speech attenuation
- Tip/Ring side CAS detection typically meets talkdown condition 1 (the average case)
- 1200 baud Bell 202 and CCITT V.23 FSK demodulation
- Selectable 3-wire FSK data interface (serial bit stream or 1 byte buffer) with facility to monitor stop bit for framing error check
- FSK carrier detect status output
- 3 to 5V ± 10% supply voltage
- Uses 3.579545MHz crystal
- Low power CMOS with power down mode

Applications

- Bellcore compliant CIDCW (Calling Identity Delivery on Call Waiting) and CWD (Call Waiting Deluxe) telephones
- CIDCW and CWD telephone adjunct boxes
- Computer Telephony Integrated (CTI) systems

Description

The MT88E46 is a CMOS integrated circuit suitable for receiving the FSK and CAS signals in North American (Bellcore) CIDCW, CWD and CID (Calling Identity Delivery) services. It provides an optimal solution for the CIDCW (also known as Type 2) and CWD (Type 2.5) telephone set applications by providing separate input op-amps for Tip/Ring and 4-wire side (receive pair of the telephone hybrid or speech IC) connections. The Tip/Ring connection is compatible with TIA's MEI scheme and can be used for FSK demodulation and 'on hook mode' CAS detection. The 4-wire side connection is for 'off hook mode' CAS detection. The CAS detection modes - on hook and off hook - use different algorithms which are optimized for the CPE states. In 'off hook mode' the CAS detector is Bellcore compliant when near end speech is attenuated 8dB or better. 'On hook mode' is optimized for talkdown only and typically meets talkdown condition 1 (the average case) without speech attenuation at Tip/Ring such as in the on hook state MEI CPE.

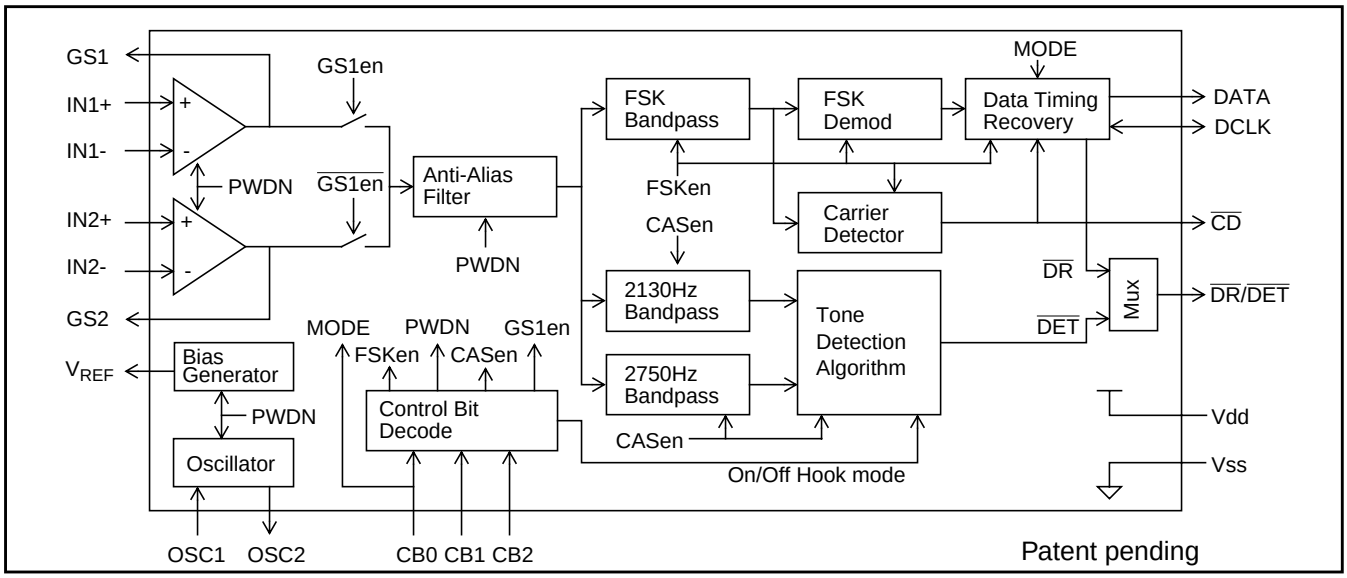


Figure 1 - Functional Block Diagram

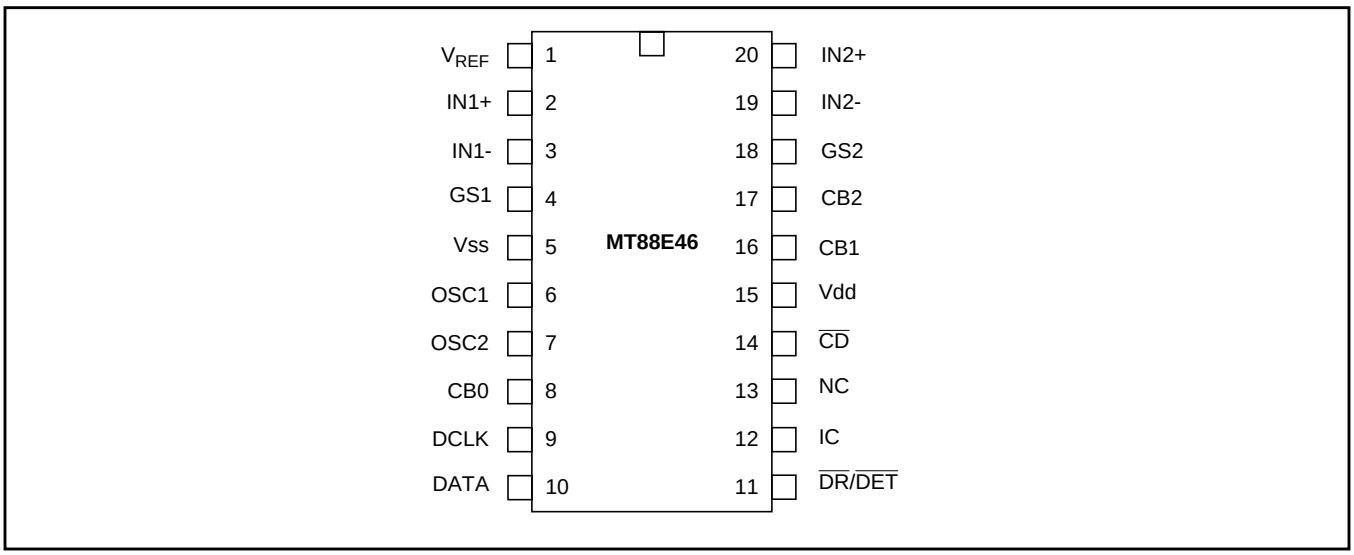


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	V_{REF}	**Voltage Reference (Output).** Nominally Vdd/2. It is used to bias the GS1 (Tip/Ring connection) and GS2 (telephone hybrid or speech IC receive pair connection) input op-amps.
2	IN1+	**GS1 Op-Amp Non-inverting Input.** The op-amp is for connecting the MT88E46 to Tip/Ring.
3	IN1-	**GS1 Op-Amp Inverting Input.** The op-amp is for connecting the MT88E46 to Tip/Ring.
4	GS1	**Gain Select 1 (Output).** This is the output of the GS1 op-amp. The op-amp should be used to connect the MT88E46 to Tip and Ring. The Tip/Ring signal can be amplified or attenuated at GS1 via selection of the feedback resistor between GS1 and IN1-. FSK demodulation or 'on hook mode' CAS detection of the GS1 signal can be selected via the CB1 and CB2 pins. See Tables 1 and 2.
5	Vss	**Power Supply Ground.**
6	OSC1	**Oscillator Input.** Crystal connection. This pin can also be driven directly from an external clock source.
7	OSC2	**Oscillator Output.** Crystal connection. When OSC1 is driven by an external clock, this pin should be left open circuit.
8	CB0	**Control Bit 0 (CMOS Logic Input).** This pin is used primarily to select the 3-wire FSK data interface mode. When it is low, interface mode 0 is selected where the FSK bit stream is output directly at the DATA pin. When it is high, interface mode 1 is selected where the FSK byte is stored in a 1 byte buffer which can be read serially by the application's microcontroller. The FSK interface is consisted of the DATA, DCLK and $\overline{DR}/\overline{DET}$ pins. See the 3 pin descriptions to understand how CB0 affects the FSK interface. This pin is also used with CB1 and CB2 to put the MT88E46 into a power down state drawing virtually no power supply current. See Tables 1 and 2.
9	DCLK	**3-Wire FSK Interface Data Clock (Schmitt Logic Input/CMOS Logic Output).** In interface mode 0 (when the CB0 pin is logic low) this is a CMOS output whose rising edge denotes the nominal mid-point of a bit in the FSK data byte. In interface mode 1 (when the CB0 pin is logic high) this is a Schmitt trigger input used to shift the FSK data byte out of an on chip buffer to the DATA pin.

Pin Description

Pin #	Name	Description
10	DATA	**3-Wire FSK Interface Data (CMOS Logic Output).** Mark frequency corresponds to logical 1. Space frequency corresponds to logical 0. In interface mode 0 (when the CB0 pin is logic low) the FSK serial bit stream is output to DATA directly. In interface mode 1 (when the CB0 pin is logic high) the start bit is stripped off, the data byte and the trailing stop bit are stored in a 9 bit buffer. At the end of each word indicated by the $\overline{DR}$ signal at the $\overline{DR}/\overline{DET}$ pin, the microcontroller should shift the byte out to DATA by applying 8 read pulses to the DCLK pin. A 9th DCLK pulse will shift out the trailing stop bit for framing error checking.
11	$\overline{DR}/\overline{DET}$	**3-Wire FSK Interface Data Ready/CAS Detect (CMOS Logic Output).** Active low. This is a dual purpose pin which indicates the end of an FSK word or the end of CAS. **Data Ready:** When FSK demodulation is enabled this pin denotes the end of a word. In both FSK interface modes 0 and 1, it is normally high and goes low for half a bit time at the end of a word. In mode 1 if DCLK starts while $\overline{DR}$ is low, the first rising edge of the DCLK input will return $\overline{DR}$ to high. This feature allows an interrupt requested by a low going $\overline{DR}$ to be cleared upon reading the first DATA bit. **CAS Detect:** When CAS detection is enabled, this pin goes low after the end of CAS for 416µs (nominal) to indicate that CAS has been detected.
12	IC	**Internal Connection.** Must be left open circuit.
13	NC	**No Connection.** This pin is not bonded to the die and is unaffected by external connections.
14	$\overline{CD}$	**Carrier Detect (CMOS Logic Output).** Active low. A logic low indicates that an FSK signal is present. A 10ms time hysteresis has been provided to allow for momentary signal discontinuity. The demodulated FSK data is ignored until carrier detect has been activated.
15	Vdd	**Positive Power Supply.** A decoupling capacitor should be connected directly across the Vdd and Vss pins.
16	CB1	**Control Bit 1 (CMOS Logic Input).** Together with CB2 this pin enables FSK demodulation or CAS detection. See Tables 1 and 2.
17	CB2	**Control Bit 2 (CMOS Logic Input).** Together with CB1 this pin enables FSK demodulation or CAS detection. See Tables 1 and 2.
18	GS2	**Gain Select 2 (Output).** This is the output of the GS2 op-amp. The op-amp should be used to connect the MT88E46 to the receive pair of the telephone hybrid or speech IC. The signal can be amplified or attenuated at GS2 via selection of the feedback resistor between GS2 and IN2-. When the application is a telephone adjunct box where there is no hybrid or speech IC, if the GS2 gain with respect to Tip/Ring is to be set to the same as that of GS1, the GS2 op-amp can be connected as a voltage follower to the GS1 op-amp output (see Figure 5). The GS2 signal is used for 'off hook mode' CAS detection only as selected via the CB1 and CB2 pins. See Tables 1 and 2.
19	IN2-	**GS2 Op-Amp Inverting Input.** The op-amp is for connecting the MT88E46 to the receive pair of the telephone hybrid or speech IC.
20	IN2+	**GS2 Op-Amp Non-Inverting Input.** The op-amp is for connecting the MT88E46 to the receive pair of the telephone hybrid or speech IC.

Control Bit (CB0/1/2) Functionality

CB0	CB1	CB2	FSK Interface	Input Op-Amp	Function
0/1	1	1	Set by CB0	GS1	**FSK Demodulation.** $\overline{DR}/\overline{DET}$ pin is the $\overline{DR}$ signal.
0/1	1	0	Set by CB0	GS2	**'Off hook mode' CAS Detection.** $\overline{DR}/\overline{DET}$ pin is the $\overline{DET}$ signal. The off hook mode algorithm is Bellcore talkoff and talkdown compliant when near end speech level is attenuated 8dB or better. It should be used for the off hook state CPE.
0/1	0	1	Set by CB0	GS1	**'On hook mode' CAS Detection.** $\overline{DR}/\overline{DET}$ pin is the $\overline{DET}$ signal. When the line is in use, a TIA Multiple Extension Interworking (MEI) compatible Type 2 CPE must be able to detect CAS even though the CPE itself is on hook. Since in most telephone designs the hybrid or speech IC is not operational when the CPE itself is on hook, this mode provides Tip Ring CAS detection for the on hook state MEI CPE. The on hook mode algorithm is optimized for talkdown only and typically meets talkdown condition 1 (the average case) without near end speech attenuation. It must not be used when the CPE itself is off hook. See 'On Hook Mode CAS Detection' section in 'Functional Description'.
1	0	0	Mode 1	-	**Power Down.** $\overline{DR}/\overline{DET}$ pin is logic high. The MT88E46 is disabled and draws virtually no power supply current. Note that the DCLK pin becomes an input pin because FSK interface mode 1 is selected by CB0=1.
0	0	0	Mode 0	-	Reserved for factory testing.

Table 1 - CB0/1/2 Function Table

The number of control bits (CB) required to interface the MT88E46 to the microcontroller depends on the functionality of the application.

Functionality Group	Controls	Description
FSK, Off Hook mode CAS (Non MEI compatible)	CB2	CB0 is connected to Vdd or Vss to select the FSK interface mode. CB1 connected to Vdd. The microcontroller uses CB2 to select between the 2 functions.
FSK, Off Hook mode CAS, On Hook mode CAS	CB1 CB2	CB0 is connected to Vdd or Vss to select the FSK interface mode. The microcontroller uses CB1 and CB2 to select between the 3 functions.
FSK (Interface mode 1), Off Hook mode CAS, On Hook mode CAS, Power Down	CB1 CB2	CB0 is connected to Vdd to select FSK interface mode 1. The microcontroller uses CB1 and CB2 to select between the 4 functions.
FSK (Interface mode 0), Off Hook mode CAS, On Hook mode CAS, Power Down	CB0 CB1 CB2	All 3 pins are required.

Table 2 -Control Bit Functionality Groups

Functional Overview

In the Calling Identity Delivery on Call Waiting (CIDCW) and Call Waiting Deluxe (CWD) services offered by North American telephone operating companies, a dual tone known as CAS (CPE Alerting Signal) is sent from the central office to notify the near end CPE, which is already engaged in an established call, that the central office wishes to deliver calling identity information of a waited call. The signalling protocol is specified in Bellcore GR-30-CORE, the CPE (Customer Premises Equipment) requirements in SR-TSV-002476.

In the GR-30-CORE off hook protocol, the central office mutes the far end connection (the other end of the established call) just before CAS is transmitted. When the near end CPE detects the CAS, it mutes the handset and checks whether there is any parallel off hook CPE. If there is no parallel off hook CPE, it acknowledges CAS reception by sending ACK, which is a predefined DTMF digit, back to the central office. When the central office receives ACK, it transmits the calling party information in 1200 baud Bell 202 format FSK to the near end CPE which then typically displays the information to the user.

When CAS is transmitted from the central office, even though the far end has been muted the near end user (the end which is to receive the caller ID information) may be speaking. Therefore, the CAS must be detected in the presence of near end speech, noise or music. Failure to detect the CAS and reply with ACK within a defined interval is known as ‘talkdown’. Talkdown is undesirable because the central office will not deliver the calling information, hence the quality of the CIDCW or CWD service will be degraded.

Since CAS can be transmitted anytime during an established call, the CAS detector is therefore subjected to speech, noise or music - which can imitate CAS - from both the near end and the far end throughout the call. False detection followed by ACK is known as ‘talkoff’. Talkoff is undesirable because it annoys the far end user by the near end CPE’s sending ACK and because the near end CPE is muted in anticipation of the FSK signal.

Bellcore has specified talkdown and talkoff immunity performance requirements in SR-TSV-002476. If the CPE is a telephone, one way to achieve good CAS speech immunity is to put CAS detection on the receive pair of the telephone hybrid or speech IC instead of on Tip and Ring. Compared to a Tip/Ring connection, talkdown immunity improves because the near end speech is attenuated on the hybrid / speech IC receive pair while the CAS level is the same as on Tip/Ring. Talkoff immunity is also better because the near end speech is attenuated.

In the GR-30-CORE issue 1 off hook protocol, the near end CPE must not ACK if there is a parallel off hook CPE. Otherwise the ACK will not be detected reliably at the central office. This restriction is modified by a protocol known as MEI (Multiple Extension Interworking) developed by the TIA (Telecommunications Industry Association) in conjunction with Bellcore. MEI allows a CPE to ACK if all off hook CPEs are MEI compatible. MEI is described in the TIA/EIA-777 standard.

MEI introduces the concept of the ACK-Sender and the Backup ACK-Sender.

- On a per call basis, the ACK-Sender is the first CPE to go off hook for the call. It retains its status even if it returned on hook while the line remains in use. The ACK-Sender must give up its status if a Type 3 (Analog Display Services Interface) CPE asserts its ACK-Sender status.
- The Backup ACK-Sender is the CPE to last respond to CAS with an ACK and successfully received FSK data. It retains its status from call to call but must give up its Backup ACK-Sender status when another CPE successfully completes the CAS-ACK-FSK sequence.

When CAS is sent from the central office, all MEI compatible off hook CPEs detect CAS and go back on hook. After the ACK-Sender detected CAS, it monitors the line voltage. When the line voltage has returned to the HIGH state (the voltage when the line is not terminated by any CPE), it goes off hook and sends the ACK. If there is no ACK-Sender because the first CPE to go off hook is not MEI compatible, the Backup ACK-Sender takes over and sends the ACK. Note that both the ACK-Sender and the Backup ACK-Sender can be on hook or off hook.

Because it may be the ACK-Sender or Backup ACK-Sender, an MEI compatible on hook state CPE must be able to detect CAS when the line is in use. Additionally, the TIA/EIA-777 standard requires an MEI on hook state CPE to detect CAS during a call so that it can listen in on the FSK to keep its call log consistent with the off hook CPEs. However, a CAS detector connected only to the hybrid / speech IC cannot detect CAS when the CPE itself is on hook because either the hybrid / speech IC is not operational or the signal level is severely attenuated. Therefore an MEI compatible CPE must be able to detect CAS from Tip/Ring when the CPE is on hook, and be able to detect CAS from the hybrid / speech IC when the CPE is off hook.

The MT88E46 offers an optimal solution which combines Bellcore compliant speech immunity and MEI compatibility. Two input op-amps allow the MT88E46 to be connected to both Tip/Ring and to the receive pair of the telephone hybrid or speech IC (the 4-wire side). Each connection can be differential or single ended. FSK demodulation is available only at the Tip/Ring connection. The CAS detector operates in 'on hook mode' and 'off hook mode' using different algorithms optimized for the CPE states. On hook mode is available only at the Tip/ Ring connection, while off hook mode is available only at the 4-wire side connection.

The 'off hook mode' is Bellcore compliant when the near end speech is attenuated 8dB or better. It should be used when the CPE is off hook. The 'on hook mode' is optimized for talkdown only and typically meets talkdown condition 1 (the average case) without near end speech attenuation to provide Tip/Ring CAS detection for the on hook state MEI CPE. It should be used when the CPE itself is on hook but the line is in use.

The FSK demodulator is suitable for both Bell 202 and CCITT V.23 formats transparently, and is compatible with Bellcore and TIA standards. The demodulated FSK data is either output directly (bit stream mode) or stored in a one byte buffer (buffer mode) which can be shifted out. In the buffer mode, the stop bit immediately following a byte is also stored and can be shifted out after the data byte. This facility allows for framing error checking as required in TIA/EIA-777 for the Type 2 CPE. In the bit stream mode, two timing signals are provided. One indicates the bit sampling instants of the data byte, the other the end of the byte. A carrier detector indicates the presence of signal and shuts off the data stream when there is no signal.

The entire chip can be put into a power down mode consuming virtually no power supply current. The input op-amps, FSK demodulator, CAS detector and the oscillator are all shut off. Furthermore, partial power down has been incorporated to minimize the operating current: when FSK is selected, the CAS detector is powered down; when CAS is selected, the FSK demodulator is powered down. The two input op-amps are not affected by partial power down and will remain operational regardless of whether FSK or CAS is selected.

	SR-TSV-002476 Requirement	**Test Result for 0dB Near End Speech Attenuation using Pre-emphasized Speech only**	**Test Result for 0dB Near End Speech Attenuation using Pre-emphasized Speech for Near End, Normal Speech for Far End**	**Test Result for 6dB Near End Speech Attenuation using Pre-emphasized Speech only**
	Vdd = 5V ± 10%, GS2 gain = 0dB			
Condition 1	1 in ≥ 45 hours	1 in **48.0** hours	1 in **96.0** hours	1 in **96.0** hours
Condition 2	1 in ≥ 10 hours	1 in 8.6 hours	1 in **10.1** hours	1 in **16.5** hours
Condition 3	1 in ≥ 35 hours	1 in **37.4** hours	1 in **43.0** hours	1 in **113.1** hours
	Vdd = 3V ± 10%, GS2 gain = -4dB			
Condition 1	1 in ≥ 45 hours	1 in 32.0 hours	TBD	1 in **192.0** hours
Condition 2	1 in ≥ 10 hours	1 in **10.6** hours	TBD	1 in **19.9** hours
Condition 3	1 in ≥ 35 hours	1 in **39.8** hours	TBD	1 in **123.0** hours

Table 3 - Typical Off Hook Mode Talkoff Immunity Performance

	SR-TSV-002476 Requirement	**Test Result for 0dB Near End Speech Attenuation**	**Test Result for 8dB Near End Speech Attenuation**
	Vdd = 5V ± 10% (GS2 gain = 0dB) and 3V ± 10% (GS2 gain = -4dB)		
Condition 1	≥ 99.5%	99.2%	**99.9%**
Condition 2	≥ 93.0%	79.6%	**93.5%**
Condition 3	≥ 99.5%	97.6%	**99.7%**

Table 4 -Typical Off Hook Mode Talkdown Immunity Performance

Preliminary Off Hook Mode CAS Detector Speech Immunity Performance

Since there is some randomness in speech immunity testing, and because the telephone hybrid / speech IC design will affect the result, the preliminary test results in Tables 3 and 4 are provided to illustrate typical performances only.

In Table 3 (talkoff results) column 3, the result was obtained using pre-emphasized speech as both the near end and far end speech sources. It is pessimistic, as recognized in SR-TSV-002476, because in reality the pre-emphasis originally imparted on the far end speech by the far end CPE's microphone would have been equalized by the subscriber loop, so that at the near end CPE Tip/ Ring terminals the far end speech would have no pre-emphasis. Table 3 column 4 shows the result for the same situation as column 3 except that pre-emphasized speech was used only as the near end speech source and normal speech was used as the far end speech source, as allowed in SR-TSV-002476.

In Table 3 column 5 and Table 4 column 4, the MT88E46 performance with a telephone hybrid / speech IC was simulated during testing by attenuating the pre-emphasized near end speech equally at all frequencies. The actual performance will depend on the telephone hybrid / speech IC design.

Functional Description

3 to 5V Operation

The MT88E46 is designed to operate from a fixed voltage power supply between 3 and 5V nominal. A ±10% variation from the nominal voltage is allowed. Its FSK and CAS reject levels are proportional to Vdd. When operated at Vdd equals 3V ± 10%, to keep the FSK and CAS reject levels as at 5V ± 10%, and for optimal speech immunity, the GS1 and GS2 op-amp gains should be reduced from those of 5V. Gains for nominal Vdd's between 3 and 5V can be obtained by interpolation between the 3V and 5V values shown in Figure 9.

Input Configuration

The MT88E46 provides an input arrangement comprised of two op-amps and a bias source (V_{REF}). V_{REF} is a low impedance voltage source which is used to bias the op-amp inputs at Vdd/2. The GS1 op-amp (IN1+, IN1-, GS1 pins) is for connecting to Tip and Ring. The GS2 op-amp (IN2+, IN2-, GS2 pins) is for connecting to the receive pair of the telephone hybrid or speech IC in the telephone set application.

Either FSK demodulation or 'on hook mode' CAS detection can be selected for the GS1 signal. Only 'off hook mode' CAS detection is available for the GS2 signal. 'On hook mode' CAS detection at the GS1 op-amp is intended for the MEI on hook CPE situation. 'Off hook mode' CAS detection at the GS2 op-amp is intended for the off hook CPE situation.

The feedback resistor connected between IN1- and GS1 can be used to adjust the Tip/Ring path input gain, and the feedback resistor between IN2- and GS2 can be used to adjust the hybrid / speech IC path input gain. When the GS1 op-amp is selected, the GS2 signal is ignored. When the GS2 op-amp is selected, the GS1 signal is ignored.

Either or both op-amps can be configured in the single ended input configuration shown in Figure 3, or in the differential input configuration shown in Figure 4.

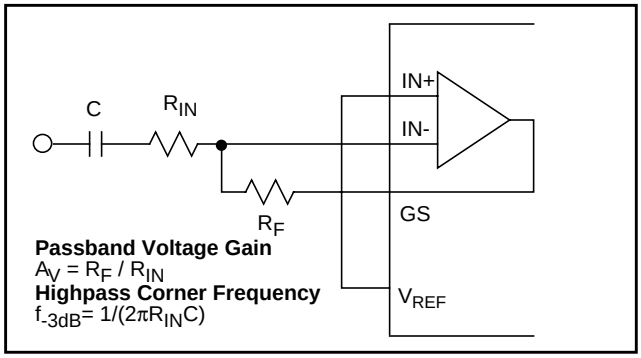


Figure 3 - Single Ended Input Configuration

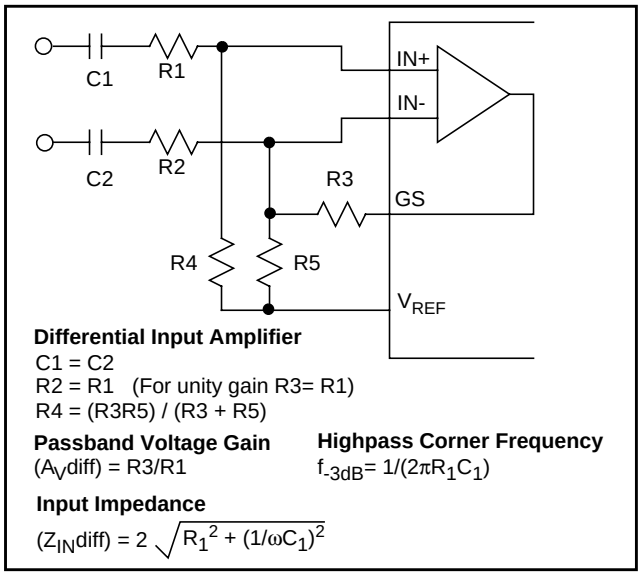


Figure 4 - Differential Input Configuration

In a telephone adjunct box application where there is no hybrid or speech IC, if the GS2 gain with respect to Tip/Ring is to be set to the same as that of GS1, the GS2 op-amp can be connected as a voltage follower to the GS1 op-amp output as shown in Figure 5.

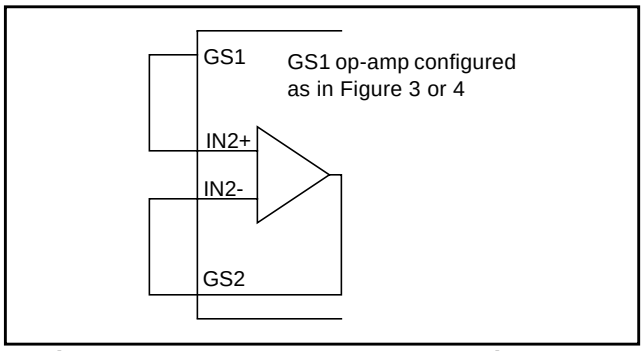


Figure 5 - GS2 Op-Amp Connected as GS1 Voltage Follower

CAS Detection

When CAS detection is selected, the dual purpose $\overline{DR}/\overline{DET}$ pin is the $\overline{DET}$ output signal. $\overline{DET}$ goes low momentarily (416 µsec nominal) after the end of CAS to indicate that CAS has been detected, as shown in Figure 13. The CAS detector operates in 'off hook mode' or 'on hook mode' as selected by the CB1 and CB2 pins (see Table 1). 'On hook mode' and 'off hook mode' use different algorithms optimized for the CPE states.

Normally $\overline{DET}$ goes low after the end of CAS. However, because of interference from speech or music, $\overline{DET}$ may go low before the end of CAS. The on hook and off hook mode algorithms ensure that $\overline{DET}$ will occur no earlier than t_{DET1} after the beginning of CAS (see Figure 13).

Similarly, speech interference can cause $\overline{DET}$ to go low later than t_{DET2} after the end of CAS (see Figure 13). In off hook mode, the detection algorithm ensures that $\overline{DET}$ will occur no later than 35ms after the end of CAS even with speech interference, as required in TIA/EIA-777. In on hook mode, although the detection algorithm does not limit the detection delay from the end of CAS, talkdown typically meets the SR-TSV-002476 talkdown condition 1 (the average case) when only the detections which occur from the beginning of CAS to 35ms after the end of CAS are counted.

Off Hook Mode CAS Detection

The 'off hook mode' is Bellcore talkdown and talkoff compliant when the near end speech is attenuated 8dB or better, such as provided by the telephone hybrid or speech IC. When near end speech is not attenuated, such as from a parallel off hook CPE or when the application is a telephone adjunct box, talkoff is close to compliant while talkdown is close to condition 1 (the average case). This mode is intended for the off hook CPE situation and is available at the GS2 (4-wire side) input op-amp only.

On Hook Mode CAS Detection

The 'on hook mode' is optimized for talkdown only. It typically meets talkdown condition 1 without near end speech attenuation. It is intended for the MEI on hook CPE situation and must not be used when the CPE itself is off hook. The input is the GS1(Tip/Ring) op-amp because in most CPE designs, to detect CAS when the CPE itself is on hook, the signal must come from the Tip/Ring connection since either the telephone hybrid / speech IC is not operational or the 4-wire side signal level is severely attenuated.

In the MEI protocol, the ACK-Sender and Backup ACK-Sender can be on hook or off hook. Therefore, if the on hook state CPE is the ACK-Sender or the Backup ACK-Sender, it must be able to detect CAS when the line is in use. Additionally, an on hook state MEI CPE must be able to detect CAS during a call so that it can listen in on the FSK to keep its call log consistent with the off hook CPEs, as required in TIA/EIA-777.

The MT88E46 on hook mode algorithm has been optimized for talkdown because of the way the MEI protocol works. In MEI, the following events (described in TIA/EIA-777) occur when CAS is detected:

- Each off hook CPE shall proceed to the on hook state not earlier than 25ms and no later than 60ms after the end of CAS as measured on Tip/Ring. (The 25ms delay is necessary to prevent the on hook transition from corrupting the CAS for other CPEs that may not have completely qualified the signal. The additional 35ms that defines the 60ms upper limit allows for variation in CAS detection delay.)
- After detecting a line HIGH state (the line voltage when the line is not terminated by any CPE), the ACK-Sender shall go off hook. The ACK-Sender shall allow the line to remain in the HIGH state for at least 5ms but not more than 8ms. If no line HIGH state is detected within 100ms after going on hook, all previously off hook CPE shall return to the off hook state.
- Following a CAS the Backup ACK-Sender shall monitor the line for a line HIGH state lasting a minimum of 15ms. Once this condition has been detected, the Backup ACK-Sender shall

immediately become the ACK-Sender, go off hook no later than 20ms after the start of the line HIGH state, complete the CAS-ACK handshake, and remain as ACK-Sender for the remainder of the call. This situation may happen if the designated ACK-Sender is not MEI compliant.

- An MEI compliant CPE that is not the designated ACK-Sender or the Backup ACK-Sender but which is off hook at the time of the CAS, shall monitor the line for a line HIGH state lasting a minimum of 30ms. Once this condition has been detected, the CPE shall immediately become the ACK-Sender, go off hook no later than 35ms after the start of the line HIGH state, complete the CAS-ACK handshake, and remain as ACK-Sender for the duration of the call. This situation can happen if the designated ACK-Sender and the Backup ACK-Sender are not MEI compliant.
- After going off hook the ACK-Sender shall begin transmission of the ACK no earlier than 30ms and no later than 40ms after the leading edge of the line HIGH voltage transition.

After the ACK-Sender or Backup ACK-Sender detected CAS, it must monitor the line for the line HIGH state, which can happen only if all off hook CPEs also detected CAS. Hence if the ACK-Sender or Backup ACK-Sender is an on hook CPE, even if it falsely detected CAS, talkoff can occur only if all off hook CPEs also falsely detected CAS. Thus in the situation where the ACK-Sender or Backup ACK-Sender is an on hook CPE using the MT88E46 on hook mode detection algorithm, talkoff protection is provided by the off hook CPEs. The on hook mode has been optimized to be more talkdown immune so that in this situation the on hook CPE will be successful in fulfilling its ACK-Sender or Backup ACK-Sender responsibility.

FSK Demodulation

The FSK demodulator is compatible with Bellcore SR-TSV-002476, TIA/EIA-716 and TIA/EIA-777 standards. It is capable of both Bell 202 and CCITT V.23 formats transparently. FSK demodulation is available at the GS1 input op-amp only.

FSK Data Interface

The MT88E46 provides a powerful dual mode 3-wire interface so that the data bytes in the demodulated FSK bit stream can be extracted without the need either for an external UART or for the CPE's microcontroller to perform the function in software.

The interface is specifically designed for the 1200 baud rate and is consisted of 3 signals: DATA, DCLK (Data Clock) and $\overline{DR}$ (Data Ready). DATA is an output pin. DCLK is an input output pin. $\overline{DR}$ uses the dual purpose output pin $\overline{DR}/\overline{DET}$. When FSK is selected it is the $\overline{DR}$ signal.

Two FSK interface modes (modes 0 and 1) are selectable via the CB0 pin. In mode 0, the FSK bit stream is output directly. In mode 1, the data byte and the trailing stop bit are stored in a 9 bit buffer. If mode 1 is used, the CB0 pin can be connected to Vdd. If mode 0 is used and full chip power down is not required, the CB0 pin can be connected to Vss.

In Bellcore's off hook protocol, a Type 2 CPE should restore the voicepath within 50ms after the end of the FSK signal. Due to noise, end of carrier detection is not always reliable. The TIA/EIA-777 standard requires the CPE to detect the end of FSK when any one of the following occurs:

- absence of carrier signal or,
- more than five framing errors (trailing stop bit a 0 instead of a 1) have been detected in the FSK message or,
- more than 150ms of continuous mark signal or space signal has been detected.

FSK Data Interface Mode 0 - Bit Stream Mode

This mode is selected when the CB0 pin is low. In this mode the FSK data is output directly to the DATA pin. DCLK and $\overline{DR}$ are timing signal outputs (see Figure 14).

For each received stop and start bit sequence, the MT88E46 outputs a fixed frequency clock string of 8 pulses at the DCLK pin. Each DCLK rising edge occurs in the middle of a DATA bit of the FSK byte. DCLK is not generated for the start and stop bits. Consequently, DCLK will clock only valid data into a peripheral device such as a serial to parallel shift register or into a microcontroller. The MT88E46 also outputs an end of word pulse $\overline{DR}$ (Data Ready). $\overline{DR}$ goes low for half a nominal bit time at the beginning of the trailing stop bit. It can be used to interrupt a microcontroller or cause a serial to parallel converter to parallel load its data into the microcontroller. If a shift register is not used, DCLK and DATA may occupy 2 bits of a microcontroller's input port. The microcontroller polls the input port and saves the DATA bit when DCLK changes from low to high. When $\overline{DR}$ goes low, the word may then be assembled from the last 8 saved bits.

Since the $\overline{DR}$ rising edge occurs in the middle of the trailing stop bit, it can be used to read the stop bit to

check for framing error. Alternatively, at the $\overline{DR}$ falling edge the microcontroller can set a timer for a 1/2400 second timeout and read the stop bit at DATA when the timer times out.

DATA may also be connected to a personal computer's serial communication port after conversion from CMOS to RS-232 voltage levels.

FSK Data Interface Mode 1 - Buffer Mode

This mode is selected when the CB0 pin is high. In this mode the received byte is stored on chip. At the end of a byte $\overline{DR}$ goes low to indicate that a new byte has become available. The microcontroller applies pulses at the DCLK input pin to read the register contents serially out of the DATA pin (see Figure 15).

Internal to the MT88E46, the start bit is stripped off, the data bits and the trailing stop bit are sampled and stored. Midway through the stop bit, the 8 data bits and the stop bit are parallel loaded into a 9 bit shift register and $\overline{DR}$ goes low. The register's contents are shifted out to the DATA pin on the supplied DCLK's rising edges in the order they were received. The last bit must be shifted out and DCLK returned to low before the next $\overline{DR}$. DCLK must be low for t_{DDS} before $\overline{DR}$ goes low and remain low for t_{DDH} after $\overline{DR}$ has gone low (see Figure 15 and 'AC Electrical Characteristics - Mode 1 FSK Data Interface Timing').

If DCLK begins while $\overline{DR}$ is low, $\overline{DR}$ will return to high upon the first DCLK rising edge. If $\overline{DR}$ interrupts a microcontroller then this feature allows the interrupt to be cleared by the first read pulse. Otherwise $\overline{DR}$ is low for half a nominal bit time (1/2400 sec).

Reading the stop bit allows the software to check for framing errors. When framing error is not checked the microcontroller only needs to send 8 DCLK pulses to shift the data byte out.

FSK Carrier Detector

The carrier detector provides an indication of the presence of a signal in the FSK frequency band. It detects the presence of a signal of sufficient amplitude at the output of the FSK bandpass filter.

The signal is qualified by a digital algorithm before the $\overline{CD}$ output is set low to indicate carrier detection. A 10ms hysteresis has been provided to allow for momentary signal dropout once $\overline{CD}$ has been activated. $\overline{CD}$ is released when there is no activity at the FSK bandpass filter output for 10ms.

When $\overline{CD}$ is inactive (high), the raw output of the FSK demodulator is ignored by the internal data timing recovery circuit. In FSK interface mode 0 the DATA, DCLK and $\overline{DR}$ outputs are forced high. In mode 1 the output shift register is not updated and $\overline{DR}$ is high; if DCLK is clocked, DATA is undefined.

Note that signals such as speech, CAS and DTMF tones also lie in the FSK frequency band and the carrier detector may be activated by these signals. They will be demodulated and presented as data. To avoid the false data, the MT88E46 should be put into CAS or power down mode when FSK is not expected. Ringing, on the other hand, does not pose a problem as it is ignored by the carrier detector.

Interrupt

The $\overline{DR}/\overline{DET}$ output can be used to interrupt a microcontroller. When the MT88E46 is the only interrupt source, $\overline{DR}/\overline{DET}$ can be connected directly to the microcontroller's interrupt input. Figure 7 shows the necessary connections when the MT88E46 is one of many interrupt sources. The diodes and resistors implement a wired-or so that the microcontroller is interrupted ($\overline{INT}$ low active or falling edge triggered) when one or more of $\overline{INT1}$, $\overline{INT2}$ or $\overline{DR}/\overline{DET}$ is low. The microcontroller can determine which one of $\overline{DR}/\overline{DET}$, $\overline{INT1}$ or $\overline{INT2}$ caused the interrupt by reading them into an input port.

Power Down

The MT88E46 can be powered down to consume virtually no power supply current via a state of the CB0/1/2 pins. Momentary transition of CB0/1/2 into the power down code will not activate power down. In power down mode both input op-amps, V_{REF} and the oscillator are not operational; DCLK becomes an input pin because to select the power down state CB0 is 1 which selects FSK interface mode 1. If the application uses FSK interface mode 0 and the MT88E46 needs to be powered down, then during power down the input state of the DCLK input must be defined, for example, by a pull down resistor (R13 in Figure 8) so that the MT88E46 will draw minimal power supply current. When the MT88E46 is powered down DATA, $\overline{DR}/\overline{DET}$, $\overline{CD}$ are high.

To reduce the operating current a partial power down feature has been incorporated. When FSK is selected, the CAS detector is powered down. When CAS is selected the FSK demodulator is powered down. The two input op-amps are not affected and both will remain operational.

The partial power down feature can also be used to reset the FSK or CAS circuits, such as upon system power up. To reset the FSK demodulator, use CB1/2 to select CAS mode for about 10µs, $\overline{DR}$ will become high. To reset the CAS detector, select FSK mode for about 10µs, $\overline{DET}$ will become high.

Oscillator

The MT88E46 requires a 3.579545MHz crystal to generate its oscillator clock. To meet the CAS detection frequency tolerance specifications the crystal must have a 0.1% frequency tolerance. The crystal specification is as follows:

Frequency:	3.579545MHz
Frequency Tolerance:	±0.1% (over temperature range of the application)
Resonance Mode:	Parallel
Load Capacitance:	18pF
Maximum Series Resistance:	150Ω
Maximum Drive Level:	2mW

e.g. CTS MP036S

Alternatively an external clock source can be used. In which case the OSC1 pin should be driven directly from a CMOS buffer and the OSC2 pin left open.

For 5V±10% applications any number of MT88E46's can be connected as shown in Figure 6 so that only one crystal is required.

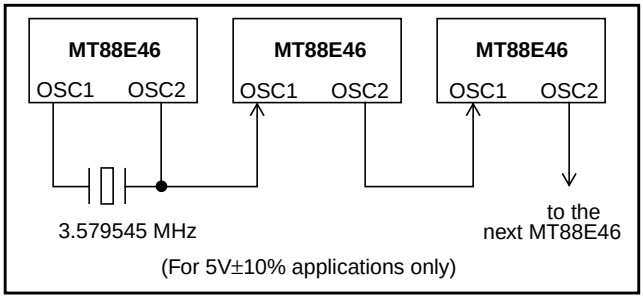


Figure 6 - Common Crystal Connection

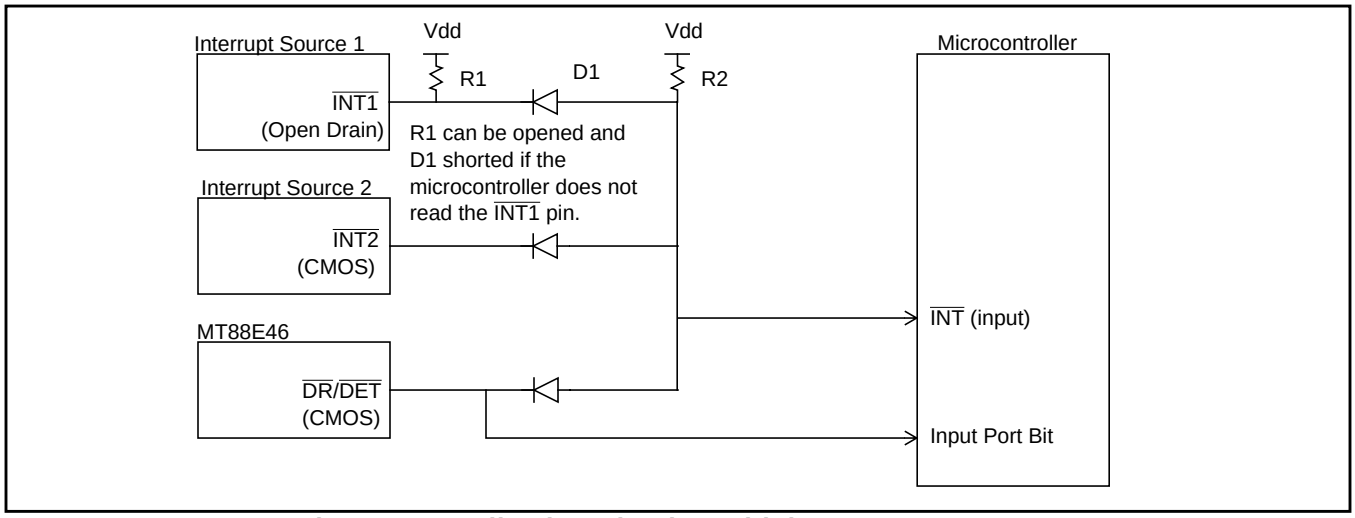
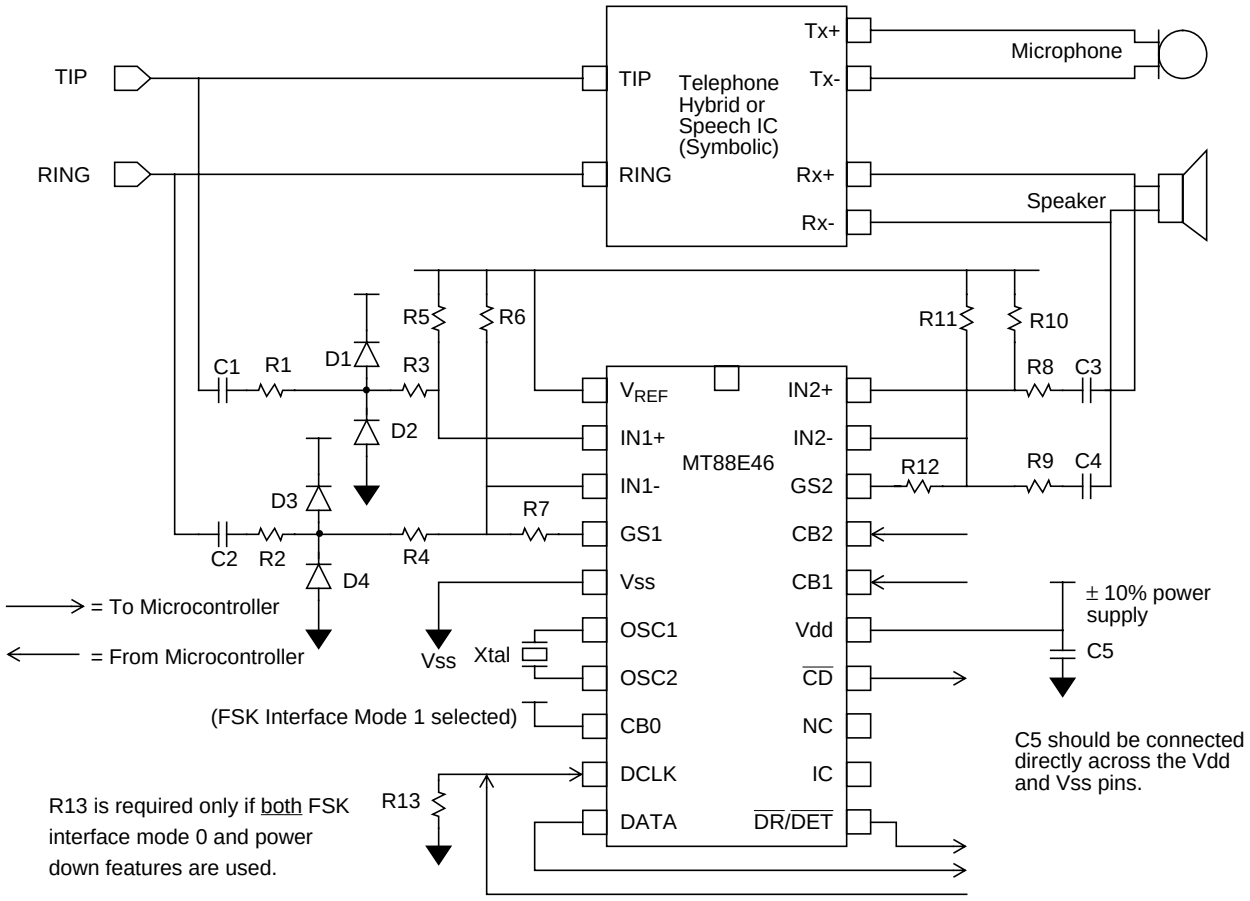


Figure 7 - Application Circuit: Multiple Interrupt Sources



Unless stated otherwise, resistors are 1%, 0.1Watt; capacitors are 5%, 6.3V.

For 1000Vrms, 60Hz isolation from Tip to Earth and Ring to Earth:

R1,R2	430K, 0.5W, 5%, 475V minimum (e.g. IRC type GS-3)	C1,C2	2n2, 1332V minimum

If the 1000Vrms is handled by other methods then this circuit has to meet the FCC Part 68 Type B Ringer requirements:

R1,R2	432K, 0.1W, 1%, 56V minimum	C1,C2	2n2, 212V minimum

Common to both sets of R1,R2 and C1,C2:

R3,R4	34K
R8, R9	464K
R13	100K, 20%. Required only if both FSK interface mode 0 and power down features are used.
C3,C4	2n2
C5	100n, 20%
D1-D4	Diodes. 1N4148 or equivalent
Xtal	3.579545MHz, 0.1% crystal

Vdd =	5V±10%	3V±10%	Vdd =	5V±10%	3V±10%
GS1 Gain	0dB	-4.0dB (preliminary)	GS2 Gain	0dB	-4.0dB (preliminary)
R5	53K6	34K0	R10	53K6	34K0
R6	60K4	38K3	R11	60K4	38K3
R7	464K	294K	R12	464K	294K

In a telephone adjunct box application where there is no hybrid or speech IC, if the GS2 gain with respect to Tip/Ring is to be set to the same as GS1, the GS2 op-amp can be connected as a voltage follower to the GS1 output as shown in Figure 5.

Figure 8 - Application Circuit: MEI Compatible Type 2 Telephone

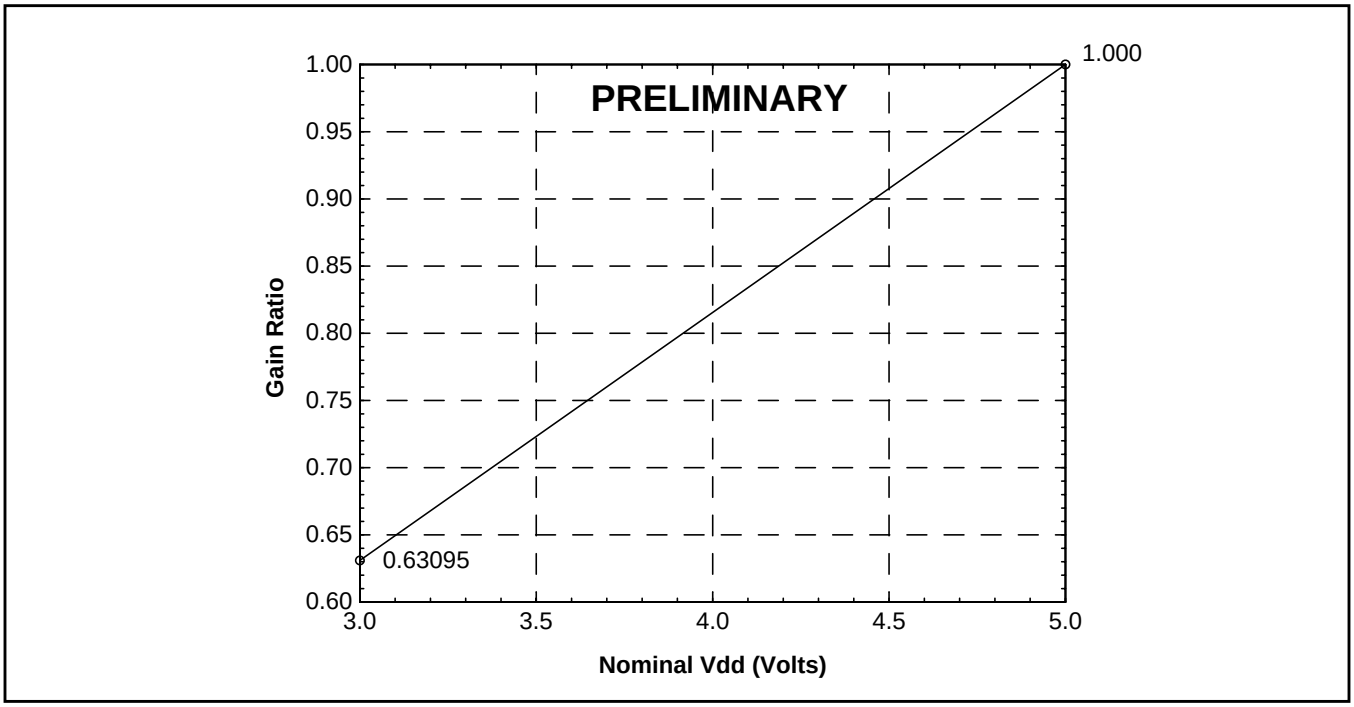


Figure 9 - GS1 and GS2 Gain Ratios as a Function of Nominal Vdd

Gain Setting Resistor Calculation for Nominal Vdd between 3 and 5V

- For the desired nominal Vdd, use Figure 9 to calculate approximate Av.
- For the GS1 op-amp, start with the 0dB gain setting resistor values of $R5_{0dB}$, $R6_{0dB}$ and $R7_{0dB}$. In Figure 8 they are 53K6, 60K4 and 464K respectively. Keep R1, R2, R3, R4, C1, C2 as in Figure 8 to keep the input highpass filter corner frequency constant for all gain settings.
- For the desired Av:

$R7_{Av} = R7_{0dB}$ x Av	Scaled for desired gain. Choose the closest standard 1% resistor value as $R7_{Av}$. Calculate Av_actual as $R7_{Av}/R7_{0dB}$.
$R5_{Av} = R5_{0dB}$ x Av_actual	Scaled for good common mode range. Choose the closest standard 1% resistor as $R5_{Av}$.
$1/R6_{Av} = 1/R5_{Av} - 1/R7_{Av}$	Calculate $R6_{Av}$ so that $R5_{Av} = R6_{Av} \parallel R7_{Av}$. Choose the closest standard 1% resistor as $R6_{Av}$.

- Repeat for R10, R11 and R12 for the GS2 op-amp.

Example:

- For the 3V gain of -4.0dB, Av = 0.63095.
- $R7_{-4dB}$ = 0.63095 x 464K = 292.76K. The closest standard 1% resistor is 294K. Av_actual is 294K/464K = 0.63362 or -3.96dB.
- $R5_{-4dB}$ = 0.63362 x 53K6 = 33.96K. The closest standard 1% resistor is 34K0.
- $1/R6_{-4dB}$ = 1/34.0K - 1/294K = 1/38.45K. The closest standard 1% resistor is 38K3.

Absolute Maximum Ratings* - Voltages are with respect to Vss unless otherwise stated

	Parameter	Sym	Min	Max	Units
1	Supply voltage with respect to Vss	Vdd	-0.3	6	V
2	Voltage on any pin other than supplies **	V_{PIN}	Vss-0.3	Vdd+0.3	V
3	Current at any pin other than supplies	I_{PIN}	-	10	mA
4	Storage Temperature	T_{ST}	-65	150	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
** Under normal operating conditions voltage on any pin except supplies can be minimum Vss-1V to maximum Vdd+1V for an input current limited to less than 200µA.

Recommended Operating Conditions - Voltages are with respect to ground (Vss) unless otherwise stated

	Characteristics	Sym	Min	Typ‡	Max	Units
1	Power Supplies	Vdd	2.7	-	5.5	V
2	Clock Frequency	f_{OSC}	-	3.579545	-	MHz
3	Tolerance on Clock Frequency	Δf_{OSC}	-0.1	-	+0.1	%
4	Operating Temperature	T_{OP}	-40	-	85	°C

‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics†

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Power Down Mode Supply Current	I_{DDQ}	-	0.1	15	µA	All inputs are at Vdd/ Vss except for oscillator pins, outputs unloaded. CB0/1/2 = 100
2		Operating Supply Current Vdd = 5V ±10% Vdd = 3V ±10%	I_{DD}	 - -	 4.3 2.7	 8 4.5	 mA mA	All inputs are at Vdd/ Vss except for oscillator pins. No analog input, outputs unloaded.
3		Power Consumption	PO	-	-	44	mW	
4	DCLK	Schmitt Input High Threshold	V_{T+}	0.48*Vdd	-	0.68*Vdd	V	
		Schmitt Input Low Threshold	V_{T-}	0.28*Vdd	-	0.48*Vdd	V	
5		Schmitt Hysteresis	V_{HYS}	0.2	-	-	V	
6	CB0 CB1 CB2	CMOS Input High Voltage	V_{IH}	0.7*Vdd	-	Vdd	V	
		CMOS Input Low Voltage	V_{IL}	Vss	-	0.3*Vdd	V	
7	DCLK DATA $\overline{DR}/\overline{DET}$ $\overline{CD}$	Output High Source Current	I_{OH}	0.8	-	-	mA	V_{OH}=0.9*Vdd

DC Electrical Characteristics† (continued)

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
8	DCLK DATA $\overline{DR}/\overline{DET}$ $\overline{CD}$	Output Low Sink Current	I_{OL}	2	-	-	mA	V_{OL}=0.1*Vdd
9	IN1+ IN1- IN2+ IN2-	Input Current	I_{IN1}	-	-	1	µA	V_{IN}=Vdd to Vss
	DCLK CB0 CB1 CB2		I_{IN2}	-	-	10	µA	V_{IN}=Vdd to Vss
10	V_{REF}	Output Voltage	V_{REF}	0.5Vdd -0.1	-	0.5Vdd +0.1	V	No Load
11		Output Resistance	R_{REF}	-	-	2	kΩ	

†DC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - CAS Detection

	Characteristics	Sym	Min	Typ‡	Max	Unit	Notes*
1	Upper Tone Frequency	f_H	2736.2	2750	2763.8	Hz	1
2	Lower Tone Frequency	f_L	2119.3	2130	2140.7	Hz	1
3	Accept Signal Level (per tone)		-32 -34.22	-	-14 -16.22	dBm dBV	1, 2, 3, 4, 5
4	'Off Hook mode' Reject Signal Level (per tone)		-	-	-45 -47.22	dBm dBV	1, 2, 4, 6
5	Twist: 20 log (V_{2130Hz}/V_{2750Hz})		-6	-	+6	dB	1, 3, 4
6	'Off Hook mode' Accept CAS Duration		75	80	85	ms	
7	'On Hook mode' Accept CAS Duration		75	-	-	ms	
8	CAS Detection Delay from Start of CAS	t_{DET1}	60	-	-	ms	See Figure 13
9	CAS Detection Delay from End of CAS - No speech	t_{DET2}	-	-	15	ms	See Figure 13
10	CAS Detection Indicator Pulse Width	t_{DW}	415	416	417	µs	See Figure 13

†AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

*Notes:
1. OSC1 frequency at 3.579545MHz ± 0.1%.
2. Tip/Ring or 4-wire side input signal level. Signal level is per tone.
   dBm = decibels above or below a reference power of 1mW into 600 ohms. 0dBm = 0.7746Vrms.
   dBV = decibels above or below a reference voltage of 1Vrms. 0dBV = 1Vrms.
3. 'On Hook mode': GS1 op-amp configured to 0dB gain for Vdd=5V±10%, -4dB (preliminary) for Vdd=3V±10%.
4. 'Off Hook mode': GS2 op-amp configured to 0dB gain for Vdd=5V±10%, -4dB (preliminary) for Vdd=3V±10%.
5. When the signal level difference between the upper and lower tones is within the twist limits.
6. Test condition is both tones have the same amplitude.

AC Electrical Characteristics† - FSK Demodulation

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	Accept Signal Level		-40 -37.78 10.0	-	-6.45 -4.23 476	dBV dBm mVrms	1, 2
2	Bell 202 Format Reject Signal Level		-	-	-50.46 -48.24 3	dBV dBm mVrms	1, 2, 3
3	Transmission Rate		1188	1200	1212	baud	
4	Mark and Space Frequencies Bell 202 1 (Mark) Bell 202 0 (Space) CCITT V.23 1 (Mark) CCITT V.23 0 (Space)		 1188 2178 1280.5 2068.5	 1200 2200 1300 2100	 1212 2222 1319.5 2131.5	 Hz Hz Hz Hz	
5	Twist: 20 log (V_{MARK}/V_{SPACE})		-6	-	+10	dB	2
6	Signal to Noise Ratio	SNR_{FSK}	20	-	-	dB	2, 3, 4
7	Input FSK to $\overline{CD}$ low delay	t_{CP}	-	-	25	ms	See Figures 16, 17
8	Input FSK to $\overline{CD}$ high delay	t_{CA}	10	-	-	ms	See Figures 16, 17
9	$\overline{CD}$ Time Hysteresis		10	-	-	ms	

†AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

*Notes:
1. Tip/Ring input signal level.
   dBm = decibels above or below a reference power of 1mW into 600 ohms. 0dBm = 0.7746Vrms.
   dBV = decibels above or below a reference voltage of 1Vrms. 0dBV = 1Vrms.
2. GS1 op-amp configured to 0dB gain for Vdd=5V±10%, -4dB (preliminary) for Vdd=3V±10%.
3. Both mark and space have the same amplitude.
4. Band limited random noise (300-3400Hz). Present when FSK signal is present.

Electrical Characteristics† - Gain Setting Amplifiers

	Characteristics	Sym	Min	Max	Units	Test Conditions
1	Input Leakage Current	I_{IN}	-	1	µA	$Vss \le V_{IN} \le Vdd$
2	Input Resistance	R_{IN}	10	-	MΩ	
3	Input Offset Voltage	V_{OS}	-	25	mV	
4	Power Supply Rejection Ratio	PSRR	30	-	dB	1kHz ripple on Vdd
5	Common Mode Rejection Ratio	CMRR	40	-	dB	$V_{CMmin} \le V_{IN} \le V_{CMmax}$
6	DC Open Loop Voltage Gain	A_{VOL}	40	-	dB	
7	Unity Gain Bandwidth	f_C	0.3	-	MHz	
8	Output Voltage Swing	V_O	0.5	Vdd-0.7	V	Load ≥ 100kΩ
9	Capacitive Load (GS1,GS2)	C_L	-	50	pF	
10	Resistive Load (GS1,GS2)	R_L	100	-	kΩ	
11	Common Mode Range Voltage	V_{CM}	1.0	Vdd-1.0	V	

†Electrical characteristics are over recommended operating conditions, unless otherwise stated.

AC Electrical Characteristics† - Mode 0 FSK Data Interface Timing

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	$\overline{DR}$	Rise time	t_{RR}	-	-	200	ns	into 50pF load See Figure 11
2		Fall time	t_{RF}	-	-	200	ns	into 50pF load See Figure 11
3		Low time	t_{RL}	415	416	417	µs	1. See Figs. 11, 14, 15
4	DATA	Rate		1188	1200	1212	baud	2
5		Input FSK to DATA delay	t_{IDD}	-	1	5	ms	See Figure 14
6	DATA DCLK	Rise time	t_R	-	-	200	ns	into 50pF load See Figure 10
7		Fall time	t_F	-	-	200	ns	into 50pF load See Figure 10
8		DATA to DCLK delay	t_{DCD}	6	416	-	µs	1, 2, 3 See Figure 10
9		DCLK to DATA delay	t_{CDD}	6	416	-	µs	1, 2, 3 See Figure 10
10	DCLK	Frequency	f_{DCLK0}	1201.6	1202.8	1204	Hz	1. See Figure 14
11		High time	t_{CH}	415	416	417	µs	1. See Figures 10, 14
12		Low time	t_{CL}	415	416	417	µs	1. See Figures 10, 14
13	DCLK $\overline{DR}$	DCLK to $\overline{DR}$ delay	t_{CRD}	415	416	417	µs	1. See Figure 14

†AC Electrical Characteristics are over recommended operating conditions, unless otherwise stated.
‡Typical figures are at 25˚C and are for design aid only: not guaranteed and not subject to production testing.

*Notes:
1. OSC1 at 3.579545 MHz ± 0.1%.
2. FSK input data at 1200 ± 12 baud.
3. Function of signal condition.

AC Electrical Characteristics† - Mode 1 FSK Data Interface Timing

		Characteristics	Sym	Min	Max	Units	Notes
1	DCLK	Frequency	f_{DCLK1}	-	1	MHz	See Figure 15
2		Duty cycle		30	70	%	
3		Rise time	t_{R1}	-	100	ns	See Figure 12
4	DCLK $\overline{DR}$	DCLK low set up to $\overline{DR}$	t_{DDS}	500	-	ns	See Figure 15
5		DCLK low hold time after $\overline{DR}$	t_{DDH}	500	-	ns	See Figure 15

†AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics† - General Timing

		Characteristics	Sym	Min	Max	Units	Notes
1	OSC2	Power-up time	t_{PU}	-	50	ms	See Figures 16, 17
2		Power-down time	t_{PD}	-	10	ms	See Figure 16

†AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

AC Electrical Characteristics - Timing Parameter Measurement Voltage Levels

	Characteristics	Sym	Level	Units	Notes
1	CMOS Threshold Voltage	V_{CT}	0.5*Vdd	V	
2	Rise/Fall Threshold Voltage High	V_{HM}	0.7*Vdd	V	
3	Rise/Fall Threshold Voltage Low	V_{LM}	0.3*Vdd	V	

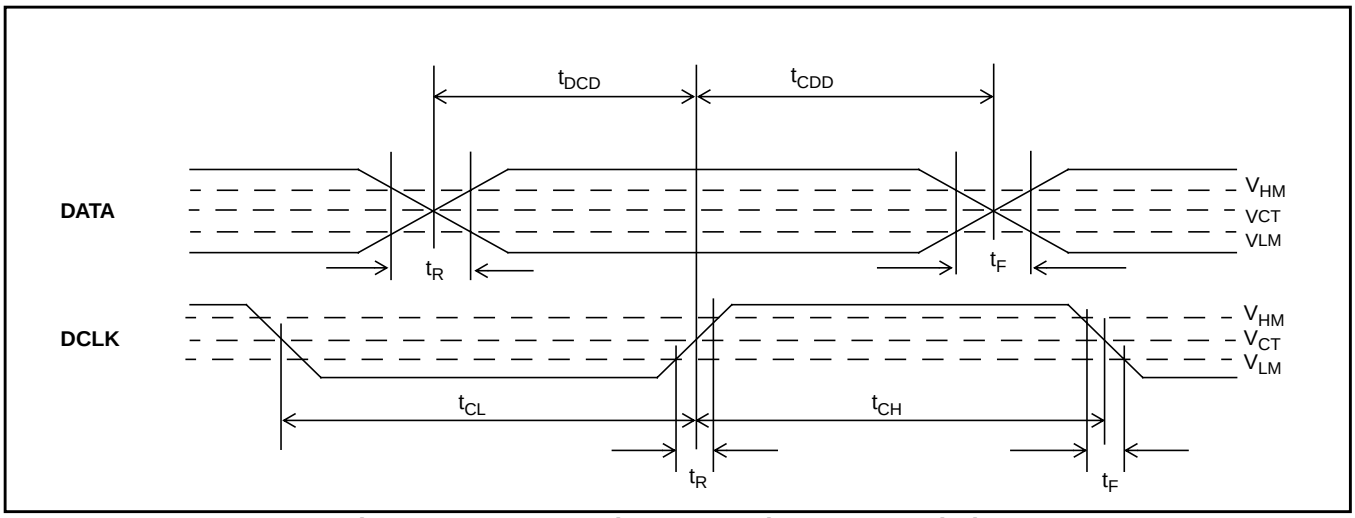


Figure 10 - DATA and DCLK Mode 0 Output Timing

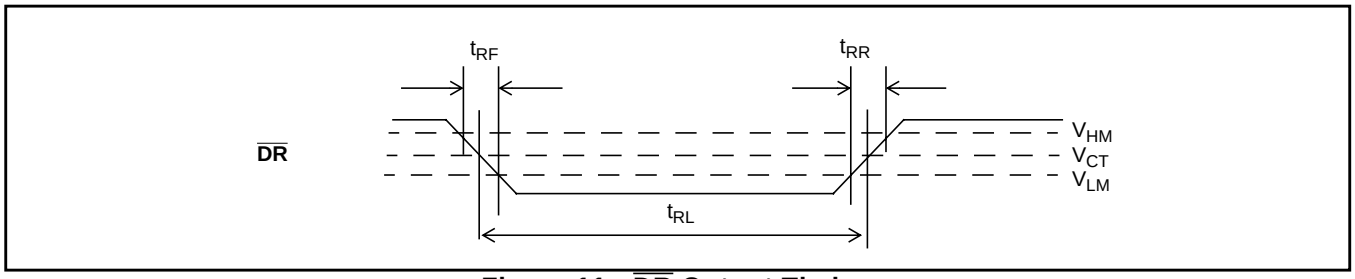


Figure 11 - $\overline{DR}$ Output Timing

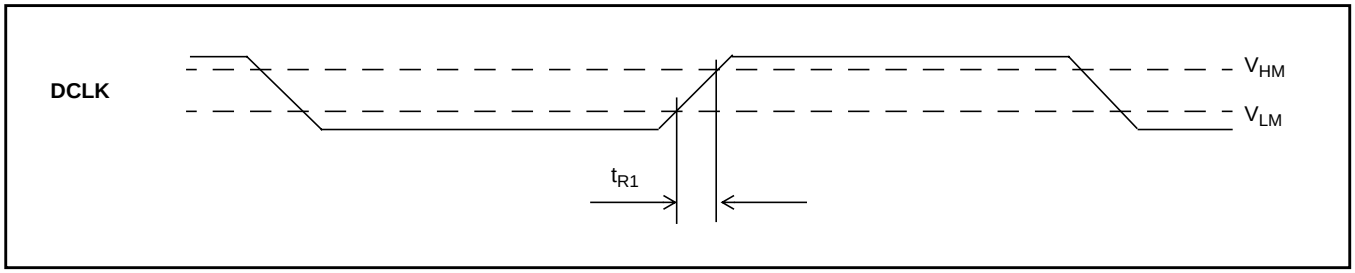


Figure 12 - DCLK Mode 1 Input Timing

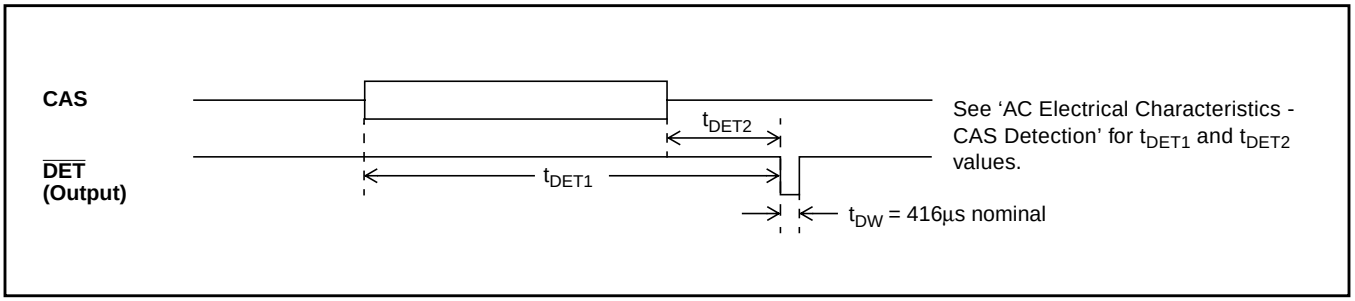
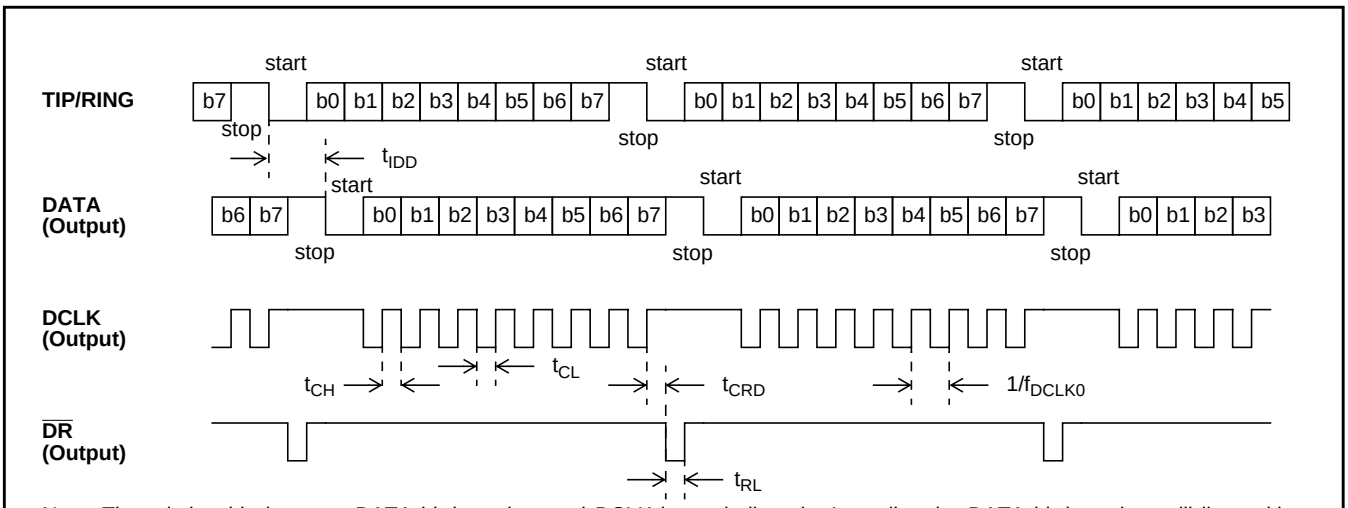
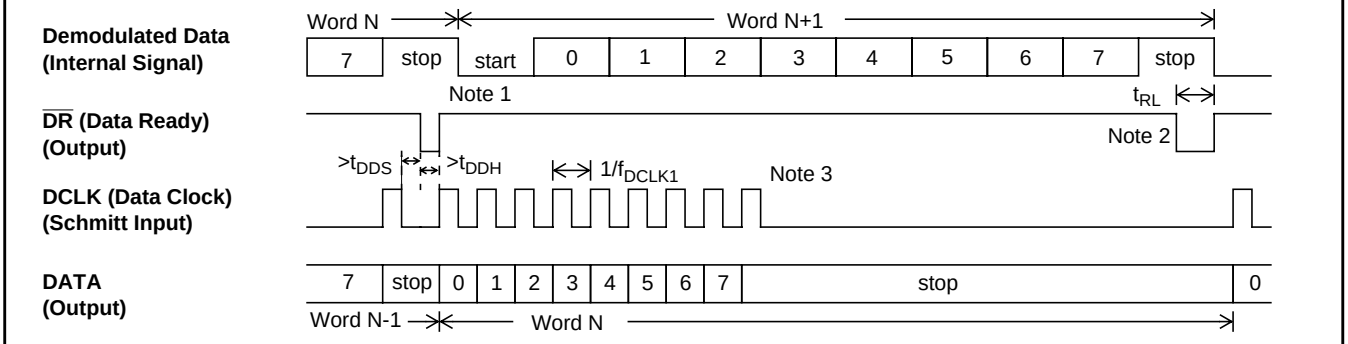


Figure 13 - CAS Detection Timing



Note: The relationship between DATA bit boundary and DCLK is symbolic only. In reality, the DATA bit boundary will jitter with respect to the DCLK falling edges.

Figure 14 - FSK Data Interface Timing - Mode 0



The DCLK input must be low before and after DR falling edge.
Note 1: DCLK occurs during DR low and returns DR to high.
Note 2: DCLK occurs after DR, so DR is low for half a nominal bit time.
Note 3: When framing error (trailing stop bit a 0 instead of a 1) is not checked, the microcontroller only needs to send 8 DCLK pulses to shift the byte out.

Figure 15 - FSK Data Interface Timing - Mode 1

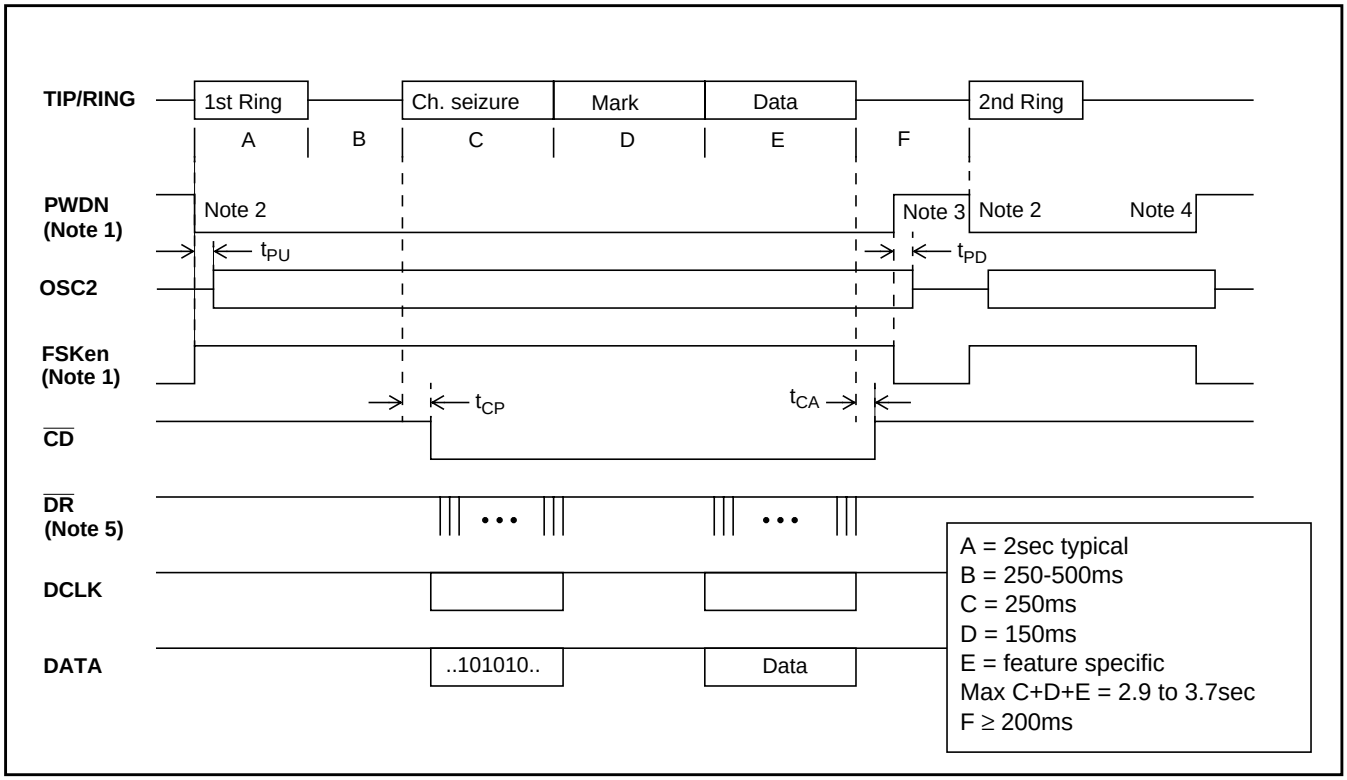


Figure 16 - Application Timing: Bellcore On-Hook Data Transmission Associated with Ringing, e.g. Calling Number Delivery, Calling Name Delivery

Notes:

This on-hook case application is included because a CIDCW CPE must also be capable of receiving on-hook data transmission (with ringing) from the central office.

1) PWDN and FSKen are internal signals decoded from CB0/1/2.
2) The CPE designer may choose to enable the MT88E46 only after the end of ringing to conserve power in a battery operated CPE. $\overline{CD}$ is not activated by ringing.
3) The microcontroller in the CPE powers down the MT88E46 after $\overline{CD}$ has become inactive.
4) The microcontroller times out if $\overline{CD}$ is not activated.
5) The $\overline{DR}$/$\overline{DET}$ output pin is the $\overline{DR}$ signal when FSK is selected.

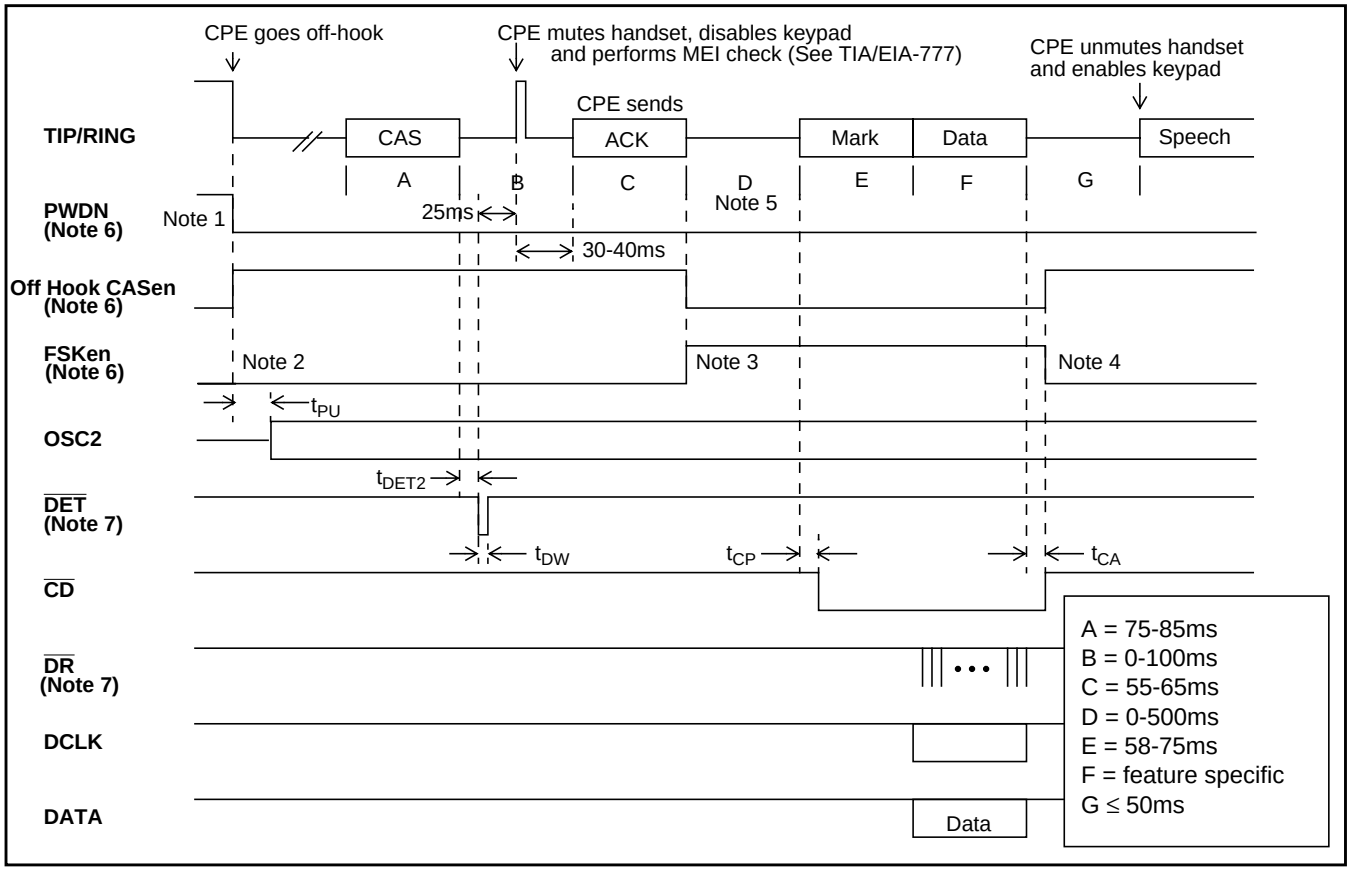
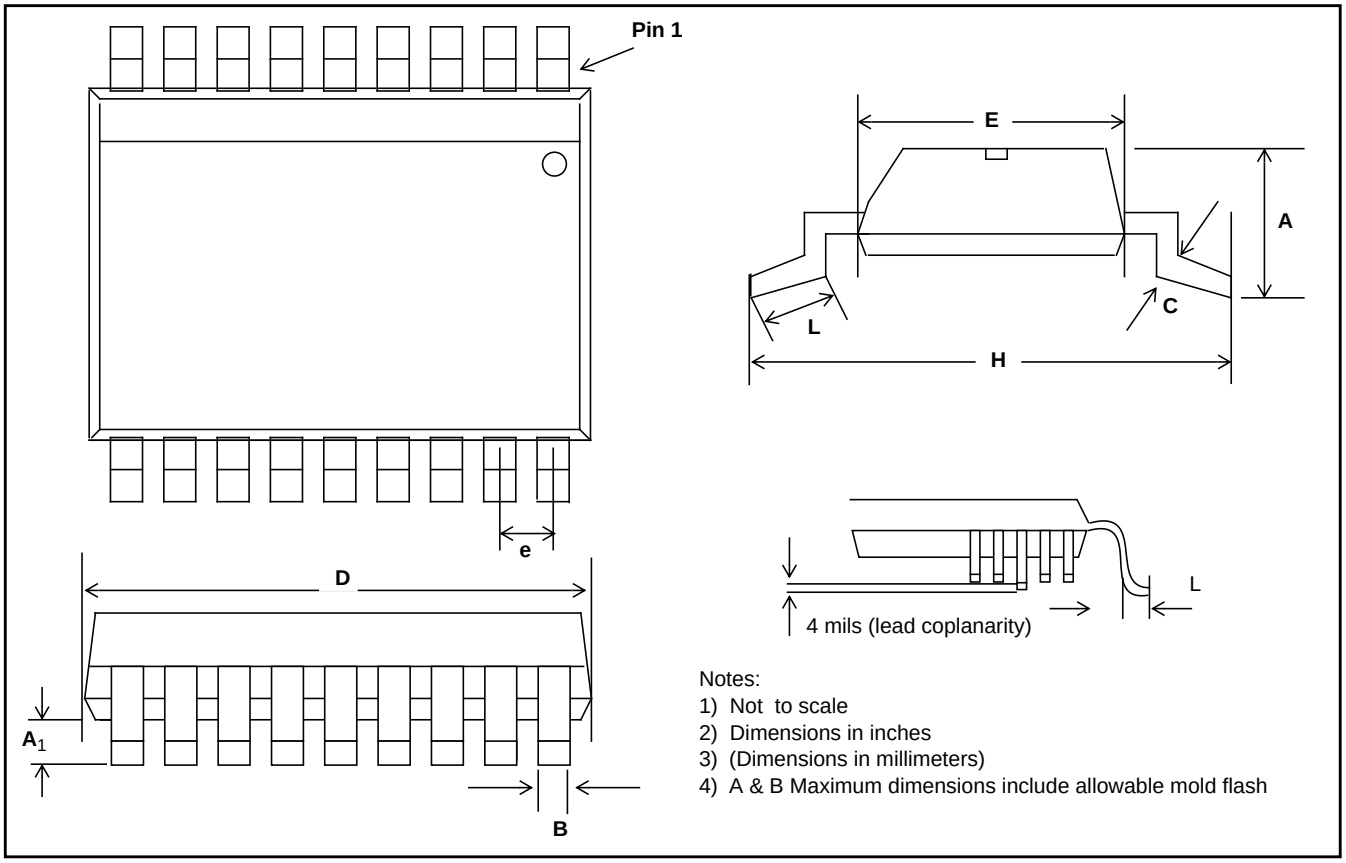


Figure 17 - Application Timing: Bellcore Off-Hook Data Transmission, e.g. CIDCW

Notes:

1) In a CPE where AC power is not available, the designer may choose to switch over to line power when the CPE goes off-hook and use battery power while on-hook. The CPE must also be CID (on-hook) capable because a CIDCW CPE includes CID functionality.
2) Non-FSK signals such as CAS, speech and DTMF tones are in the same frequency band as FSK. They will be demodulated and give false data. Therefore the MT88E46 should be taken out of FSK mode when FSK is not expected.
3) If the CPE is the ACK-Sender, the MT88E46 may be put into FSK mode right after ACK has been sent. If the CPE is not the ACK-Sender, the MT88E46 should be put into FSK mode at 30ms (min ACK delay) + 55ms (min ACK duration) = 85ms after the line HIGH transition. In that case the FSK carrier detector may be activated by the ACK if both the ACK delay and the ACK duration are at maximum. TR-NWT-000575 specifies that ACK = DTMF 'D' for non-ADSI CPE, 'A' for ADSI CPE.
4) The MT88E46 should be taken out of FSK mode when $\overline{CD}$ has become inactive, or when more than 5 framing errors have been detected in the message, or when more than 150ms of continuous Mark or Space has been detected.
5) In an unsuccessful attempt where the central office does not send the FSK signal, the CPE should unmute the handset and enable the keypad after interval D has expired.
6) PWDN, Off Hook CASen and FSKen are internal signals decoded from CB0/1/2.
7) The $\overline{DR}$/$\overline{DET}$ output pin is the $\overline{DET}$ signal when CAS detection is selected, the $\overline{DR}$ signal when FSK is selected.



Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) A & B Maximum dimensions include allowable mold flash

DIM	16-Pin		18-Pin		20-Pin		24-Pin		28-Pin	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A_1	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.013 (0.33)	0.020 (0.51)	0.013 (0.33)	0.030 (0.51)	0.013 (0.33)	0.020 (0.51)	0.013 (0.33)	0.020 (0.51)	0.013 (0.33)	0.020 (0.51)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.398 (10.1)	0.413 (10.5)	0.447 (11.35)	0.4625 (11.75)	0.496 (12.60)	0.512 (13.00)	0.5985 (15.2)	0.614 (15.6)	0.697 (17.7)	0.7125 (18.1)
E	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)	0.291 (7.40)	0.299 (7.40)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)

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NOTES: 1. Controlling dimensions in parenthesis ( ) are in millimeters.
2. Converted inch dimensions are not necessarily exact.

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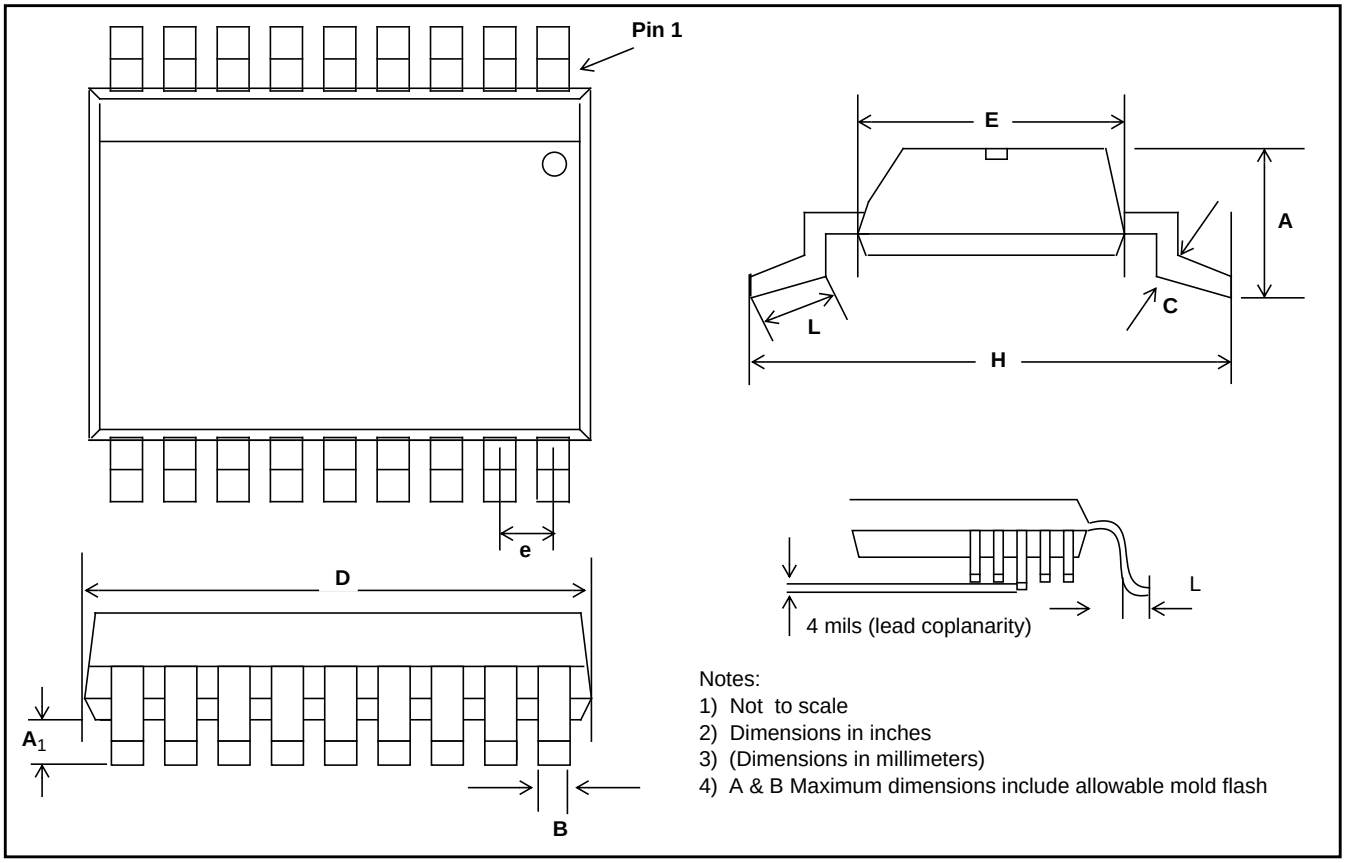

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e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)

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