Preliminary Information

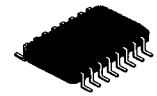
CTCSS ENCODER/DECODER

FEATURES

- **39 CTCSS Tones + Notone**
- **Scanning of any Channel**
- **Improved Sinad**
- **Squelch Tail Elimination**
- **Easy μP Interface**

APPLICATIONS

- **Mobile Radio Channel Sharing**
- **Wireless Intercom**
- **EIA 220B - 37 Tone Plus 97.4Hz & 69.3Hz**



MX265ADW
16 pin SOIC

Description

Voice on shared radio channels is multiplexed with a subaudible CTCSS tone as a means of directing messages among user groups sharing the same RF frequency. Continuous Tone Controlled Sub-audible Squelch (CTCSS) modulates the transmitter with a discrete tone, taken from a field of 39 in the range of 67 to 250 Hz, according to EIA-220-B Standard plus 69.3Hz and 97.4Hz. Groups of radio receivers, segregated by common interest and assigned tone, demodulate the voice/tone mixture for voice messages to be heard.

The MX265A features TX/RX selection and a LOAD/$\overline{\text{LATCH}}$ pin. A Notone program code has been included to permit scanning channels without CTCSS.

The MX265A is available in serial programming mode. It is designed to be used in the new short-range "sport radios," as well as in wireless intercoms.

The MX265A is a CMOS IC requiring a single 3.75-volt supply and a 1MHz clock or crystal.

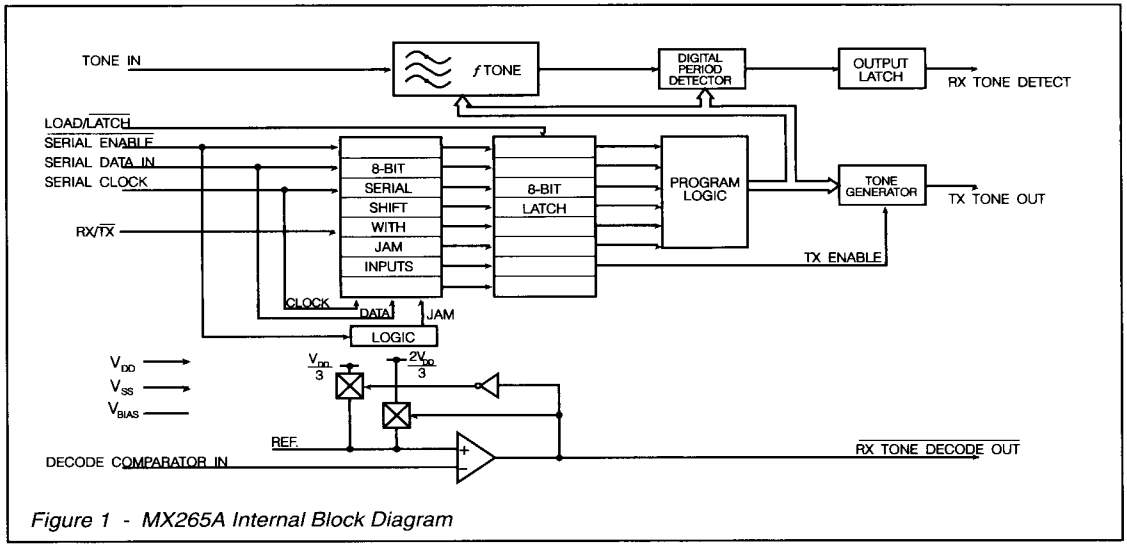
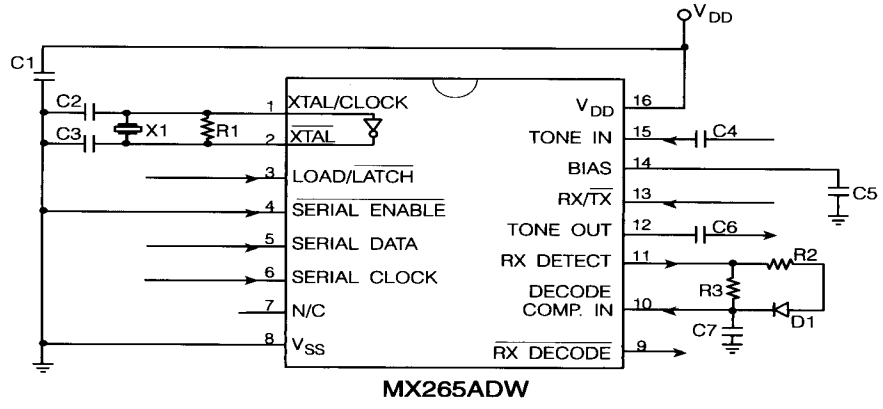


Figure 1 - MX265A Internal Block Diagram

PIN FUNCTION TABLE

Pin	Function
1	**Xtal/Clock:** Input to the on-chip inverter used with a 1 MHz Xtal or external clock source.
2	**$\overline{\text{Xtal}}$:** Output of the on-chip inverter (clock output).
3	**Load/$\overline{\text{Latch}}$:** Controls 8 on-chip latches and is used to latch RX/TX, PTL, and D0-D5 (see Table 2 for D0-D5 programming information). This pin is internally pulled to V_{DD}. A logic "1" applied to this input puts the 8 latches in "transparent" mode. A logic "0" applied to this input puts the 8 latches in the "latched" mode. Data is loaded and latched by a 0-1-0 strobe pulse on this pin (see Fig. 4).
4	**$\overline{\text{Serial Enable}}$:** A logic "0" applied to this input will enable serial programming (see Fig. 4). This pin is internally pulled to V_{DD}.
5	**Serial Data Input:** This is the serial data input. Data is loaded in the following order: D5, D4, D3, D2, D1, D0, RX/TX and PTL (see Fig. 4). This pin is internally pulled to V_{DD}.
6	**Serial Clock Input:** Data is clocked on the positive going edge (see Fig. 4). This pin is internally pulled to V_{DD}.
8	**V_{SS}:** Negative supply.
9	**$\overline{\text{RX Tone Decode Out}}$:** This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input (see Table 1).
10	**Decode Comparator Input:** This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the RX Tone Detect line.
11	**RX Tone Detect:** In RX mode this output will go to logic "1" during a successful decode. It must be externally integrated to control response and deresponse times (see Table 1).
12	**TX Tone Out:** The CTCSS sinewave output appears on this pin under control of the RX/$\overline{\text{TX}}$ pin. This pin, when not transmitting a tone, may be biased to V_{DD}-0.7V or O/C (see Table 1).
13	**RX/$\overline{\text{TX}}$:** This input selects RX or TX mode (see Fig. 2). This function may be selected by this pin, or it may be serially loaded (see Serial Data Input description above). This pin is internally pulled to V_{DD} via a 1MΩ resistor.
14	**Bias:** This pin is the output of an internally generated $V_{DD}/2$ bias level and would normally be externally decoupled to V_{SS} via capacitor C6.
15	**Tone Input:** This is the input to the CTCSS tone detector. It is internally biased to $V_{DD}/2$.
16	**V_{DD}:** Positive Supply.
7	Internal Connection. Do Not Use.



Component Values

R1: 1MΩ	C1: 0.1µF	C5: 0.47µF
R2: 560kΩ	C2: 68pF	C6: 0.1µF
R3: 820kΩ	C3: 33pF	C7: 0.1µF
X1: 1MHz	C4: 0.1µF	D1: Small signal

Tolerances: Resistors ±10%
Capacitors ±20%
Xtal ±0.1%

Figure 2 - External Components

I/O CONDITIONS

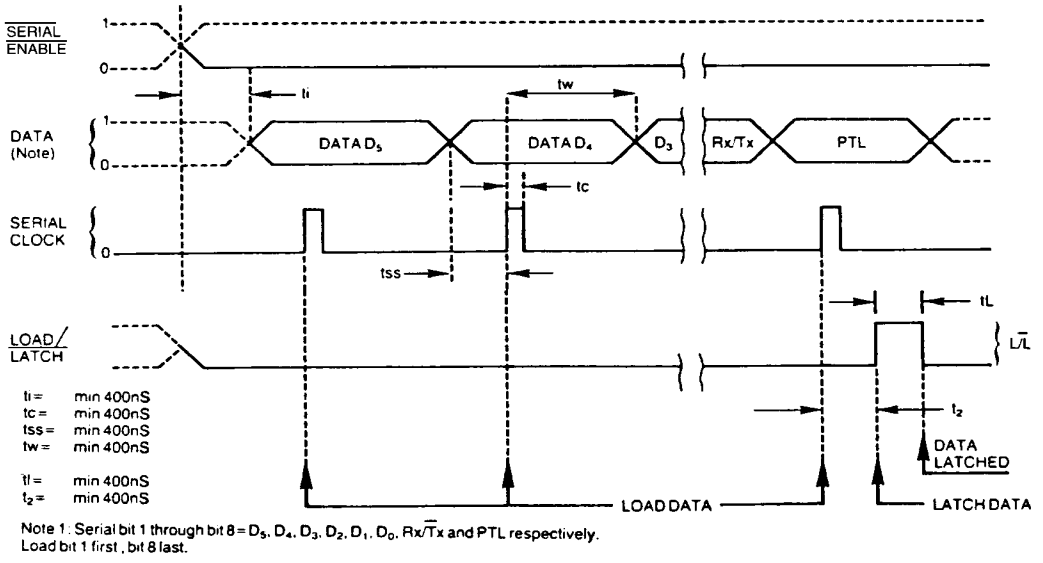
	Input Pin Condition		Output Pin Condition		Result/Function		
D0-D5	RX/$\overline{TX}$	Decode Comp Input	RX Tone Detect	$\overline{Tone}$ Decode	Tone Transmitter Enabled	Tone Decoder Enabled	Notes
Tone	0	x	0	1	Yes	No	
No tone	0	x	0	1	No (bias)	No	1
Tone	1	0	0	1	No (o/c)	Yes	2
Tone	1	1	1	0	No (o/c)	Yes	3
No tone	1	x	x	0	No (o/c)	Yes	4

Table 1 - Combinations of Input/Output Conditions

Notes:

1. NOTONE programmed in TX mode, tone transmit O/P set to $V_{DD}/2$ - 0.7V.
2. Normal decode standby.
3. Normal decode of correct CTCSS tone condition.
4. NOTONE programmed in RX mode, tone transmit O/P (o/c).

TIMING INFORMATION



Note 1: Serial bit 1 through bit 8 = D_5, D_4, D_3, D_2, D_1, D_0, $Rx/\overline{Tx}$ and PTL respectively.
Load bit 1 first, bit 8 last.

Figure 3 - Serial Mode (not to scale)

CTCSS PROGRAMMING TABLE

Tone			Programming for Serial Data Inputs						
Nominal Frequency (Hz)	**MX265A Freq. (Hz)**	**△fo (%)**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Hex**
67.0	67.05	+0.07	1	1	1	1	1	1	3F
69.3	69.32	+.03	1	1	1	0	0	1	39
71.9	71.9	0	0	1	1	1	1	1	1F
74.4	74.35	-0.07	1	1	1	1	1	0	3E
77.0	76.96	-0.5	0	0	1	1	1	1	0F
79.7	79.77	+0.09	1	1	1	1	0	1	3D
82.5	82.59	+0.1	0	1	1	1	1	0	1E
85.4	85.38	-0.2	1	1	1	1	0	0	3C
88.5	88.61	+0.13	0	0	1	1	1	0	0E
91.5	91.58	+0.09	1	1	1	0	1	1	3B
94.8	94.76	-0.04	0	1	1	1	0	1	1D
97.4	97.29	-0.11	1	1	1	0	1	0	3A
100.0	99.96	-0.04	0	0	1	1	0	1	0D
103.5	103.43	-0.07	0	1	1	1	0	0	1C
107.2	107.15	-0.05	0	0	1	1	0	0	0C
110.9	110.77	-0.12	0	1	1	0	1	1	1B
114.8	114.64	-0.14	0	0	1	0	1	1	0B
118.8	118.8	0	0	1	1	0	1	0	1A
123.0	122.8	-0.17	0	0	1	0	1	0	0A
127.3	127.08	-0.17	0	1	1	0	0	1	19
131.8	131.67	-0.10	0	0	1	0	0	1	09
136.5	136.61	+0.08	0	1	1	0	0	0	18
141.3	141.32	+0.02	0	0	1	0	0	0	08
146.2	146.37	+0.12	0	1	0	1	1	1	17
151.4	151.09	-0.2	0	0	0	1	1	1	07
156.7	156.88	+0.11	0	1	0	1	1	0	16
162.2	162.31	+0.07	0	0	0	1	1	0	06
167.9	168.14	+0.14	0	1	0	1	0	1	15
173.8	173.48	-0.19	0	0	0	1	0	1	05
179.9	180.15	+0.14	0	1	0	1	0	0	14
186.2	186.29	+0.05	0	0	0	1	0	0	04
192.8	192.86	+0.03	0	1	0	0	1	1	13
203.5	203.65	+0.07	0	0	0	0	1	1	03
210.7	210.17	-0.25	0	1	0	0	1	0	12
218.1	218.58	+0.22	0	0	0	0	1	0	02
225.7	226.12	+0.18	0	1	0	0	0	1	11
233.6	234.19	+0.25	0	0	0	0	0	1	01
241.8	241.08	-0.30	0	1	0	0	0	0	10
250.3	250.28	-0.01	0	0	0	0	0	0	00
Notone		N/A	1	1	0	0	0	0	30
Serial Input Mode		N/A	1	0	Data	Clock	X	X	2X
Test	4082	N/A	1	1	0	0	1	1	33 or any invalid address

Table 2 - CTCSS Tones

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage	-0.3 to 7.0 V
Input Voltage at any pin (ref V_{SS} = 0V)	-0.3 V to V_{DD} + 0.3 V
Sink/Source Current (Total)	20mA
Maximum Device Dissipation	100mW
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.

V_{DD}=3.75V

T_{AMB}=25°C

0dB ref. = 100mVrms @ 1kHz

Composite signal: 0dB 1kHz test tone, -12dB noise (band limited 6kHz gaussian white noise), -20dB f_0 CTCSS tone.

Characteristics	See Note	Min.	Typ.	Max.	Unit
STATIC VALUES					
Supply Voltage		3.0	3.75	5.5	V
Supply Current					
TX		-	-	3.5	mA
RX		-	-	3.5	mA
RX Monitor		-	-	2.5	mA
Tone Input Impedance		-	1	-	MΩ
Audio Input Impedance		-	1	-	MΩ
Audio Output Impedance		-	1	-	kΩ
Digital Input Impedance	1	-	1	-	MΩ
Input logic"1"	1	70%V_{DD}	-	-	V
Input logic "0"	1	-	-	30%V_{DD}	V
Logic "1" output 1' source = 0.1mA	2	80%V_{DD}	-	-	V
Logic "0" output 1' sink - 0.1mA	2	-	-	20%V_{DD}	V
DYNAMIC VALUES					
Decoder					
Decode Input Signal Level	3	-10	-	+3	dB
Decode Response Time	3,5,6,7	-	-	250	ms
Deresponse Time	3,5,6,7	-	180	250	ms
Decode Selectivity	3	±0.5	-	±3	%f_0
Encoder					
Tone Output Level	9	400	564	800	mV
Tone Frequency Accuracy (f error)		-0.3	-	+0.3	%f_0
Risetime to 90% nominal O/P:					
f_0>100Hz	4,7	-	15	75	ms
f_0<100Hz	4,7	-	45	120	ms
Tone Output Load Current		-	-	5	mA
Total Harmonic Distortion		-	2	5	%
Output Level Variation Between Tones	8	-1	-	+1	dB
TX Output Impedance		-	2.0	-	kΩ

Characteristics	See Note	Min.	Typ.	Max.	Unit
Serial Inputs (See Figure 3)					
Load/Latch Pulse Width t_l		400	-	-	ns
Serial Clock Pulse Width t_c		400	-	-	ns
Serial Set-up Time t_{ss}		400	-	-	ns
Serial Clock Frequency		-	1	-	MHz

NOTES:

1. Refers to RX/TX & Decode Comparator Input.
2. All logic outputs.
3. Composite Signal Test Condition.
4. Any programming tone and RL = 10,000, CL = 15pF. This includes response to a phase reversal instruction.
5. f_0>100Hz (for 100 Hz>f_0>67Hz: t = 100/f_0Hz x 250ms)
6. See Figure 3.
7. Per EIA 220-B.
8. Ref. to 100 Hz.
9. Measured at 3.75V V_{DD}.