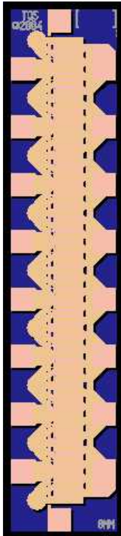
DC - 12 GHz Discrete power pHEMT TGF2021-08



Key Features and Performance

- Frequency Range: DC - 12 GHz
- > 39 dBm Nominal Psat
- 59% Maximum PAE
- 11 dB Nominal Power Gain
- Suitable for high reliability applications
- 8mm x 0.35µm Power pHEMT
- Nominal Bias Vd = 8-12V, Idq = 600-1000mA
  (Under RF Drive, Id rises from 600mA to 1920mA)
- Chip Dimensions: 0.57 x 2.42 x 0.10 mm
  (0.022 x 0.095 x 0.004 in)

Product Description

The TriQuint TGF2021-08 is a discrete 8mm pHEMT which operates from DC-12 GHz. The TGF2021-08 is designed using TriQuint's proven standard 0.35um power pHEMT production process.

The TGF2021-08 typically provides > 39 dBm of saturated output power with power gain of 11 dB. The maximum power added efficiency is 59% which makes the TGF2021-08 appropriate for high efficiency applications.

The TGF2021-08 is also ideally suited for Point-to-point Radio, High-reliability space, and Military applications.

The TGF2021-08 has a protective surface passivation layer providing environmental robustness.

Lead-free and RoHS compliant

Primary Applications

- Point-to-point Radio
- High-reliability space
- Military
- Base Stations
- Broadband Wireless Applications

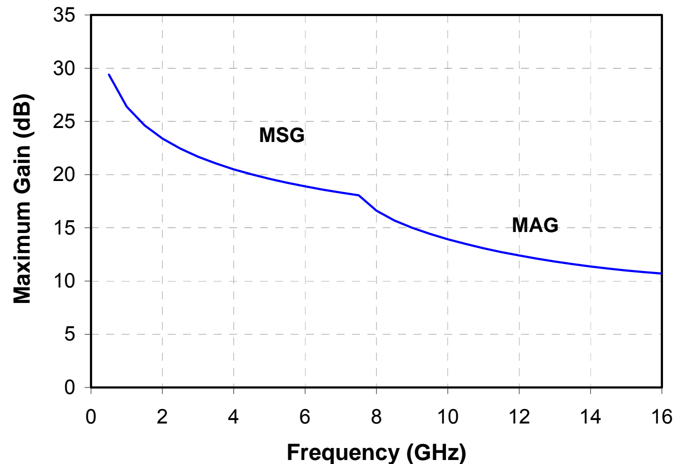


TABLE I
MAXIMUM RATINGS

Symbol	Parameter 1/	Value	Notes
V^+	Positive Supply Voltage	12.5 V	2/
V^-	Negative Supply Voltage Range	-5V to 0V	
I^+	Positive Supply Current	3.8 A	2/
$\| I_G \|$	Gate Supply Current	56 mA	
P_{IN}	Input Continuous Wave Power	34 dBm	2/
P_D	Power Dissipation	See note 3	2/ 3/
T_{CH}	Operating Channel Temperature	150 °C	4/
T_M	Mounting Temperature (30 Seconds)	320 °C	
T_{STG}	Storage Temperature	-65 to 150 °C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ For a median life time of 1E+6 hrs, Power dissipation is limited to:
$P_D(max) = (150\ °C – TBASE\ °C) / 10.8\ (°C/W)$

4/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
DC PROBE CHARACTERISTICS
(T_A = 25 °C, Nominal)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Idss	Saturated Drain Current	-	2400	-	mA
Gm	Transconductance	-	3000	-	mS
V_P	Pinch-off Voltage	-1.35	-1	-0.65	V
V_{BGS}	Breakdown Voltage Gate-Source	-30	-	-8	V
V_{BGD}	Breakdown Voltage Gate-Drain	-35	-	-15	V

Note: For TriQuint's 0.35um power pHEMT devices, RF breakdown >> DC breakdown

TABLE III
RF CHARACTERIZATION TABLE 1/
(T_A = 25 °C, Nominal)

SYMBOL	PARAMETER	Vd = 10V Idq = 600mA	Vd = 12V Idq = 600mA	UNITS
Power Tuned:				
Psat	Saturated Output Power	39.8	40.5	dBm
PAE	Power Added Efficiency	50	48	%
Gain	Power Gain	11	11	dB
Γ_L 2/	Load Reflection coefficient	0.923 ∠ 176.3	0.921 ∠ 175.4	-
Efficiency Tuned:				
Psat	Saturated Output Power	39	39.7	dBm
PAE	Power Added Efficiency	59	55	%
Gain	Power Gain	11.5	11	dB
Γ_L 2/	Load Reflection coefficient	0.937 ∠ 173.7	0.934 ∠ 173.1	-

1/ Values in this table are scaled from measurements taken from a 1mm unit pHEMT cell at 10 GHz

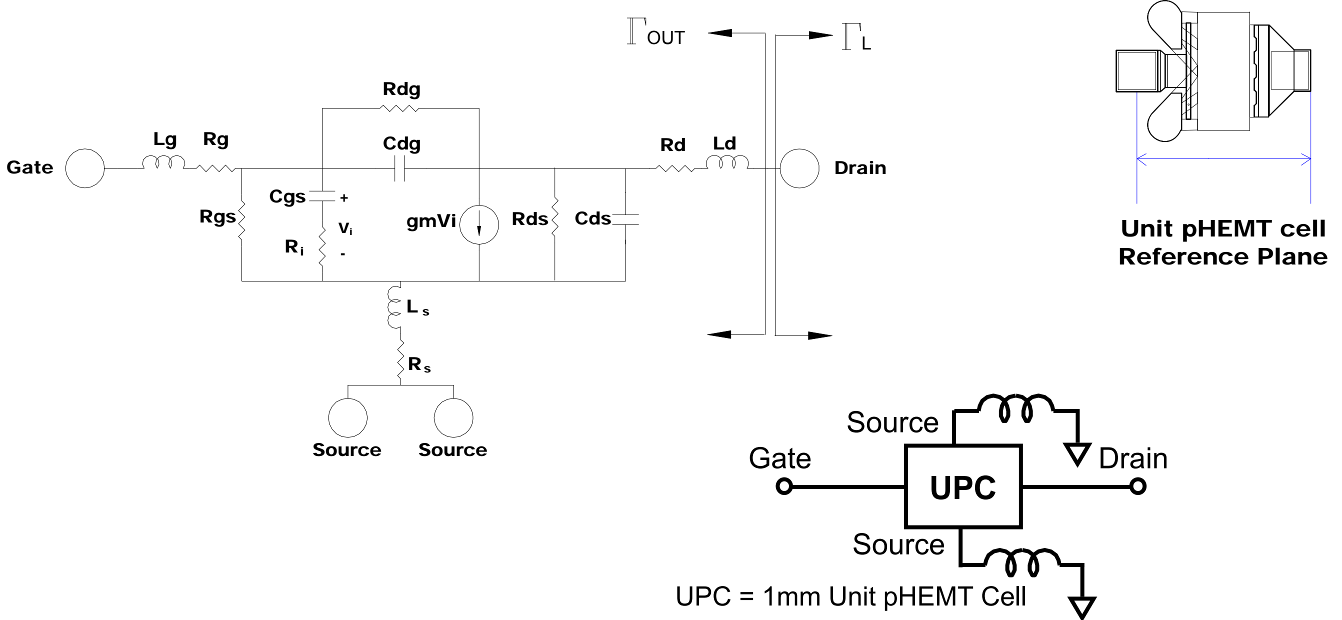
2/ Optimum load impedance for maximum power or maximum PAE at 10 GHz

TABLE IV
THERMAL INFORMATION

Parameter	Test Conditions	T_{CH} (°C)	θ_{JC} (°C/W)	T_M (HRS)
θ_{JC} Thermal Resistance (channel to backside of carrier)	Vd = 12 V Idq = 600 mA Pdiss = 7.2 W	148	10.8	1.2 E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature.

Linear Model for 1mm Unit pHEMT cell



MODEL PARAMETER	Vd = 8V Idq = 75mA	Vd = 8V Idq = 100mA	Vd = 8V Idq = 125mA	Vd = 10V Idq = 75mA	Vd = 10V Idq = 100mA	Vd = 12V Idq = 75mA	UNITS
Rg	0.45	0.45	0.45	0.45	0.450	0.45	Ω
Rs	0.14	0.14	0.14	0.17	0.160	0.19	Ω
Rd	0.41	0.43	0.46	0.41	0.450	0.410	Ω
gm	0.310	0.318	0.314	0.296	0.303	0.286	S
Cgs	2.39	2.58	2.70	2.61	2.74	2.72	pF
Ri	1.22	1.19	1.20	1.24	1.23	1.27	Ω
Cds	0.20	0.201	0.201	0.198	0.199	0.196	pF
Rds	149.1	152.3	158.8	171.8	173.7	187.9	Ω
Cgd	0.115	0.107	0.101	0.101	0.098	0.096	pF
Tau	6.29	6.63	6.99	7.19	7.410	7.79	pS
Ls	0.009	0.009	0.009	0.009	0.010	0.010	nH
Lg	0.089	0.089	0.089	0.089	0.089	0.089	nH
Ld	0.120	0.120	0.120	0.120	0.120	0.120	nH
Rgs	33000	33000	35100	28900	35700	24400	Ω
Rgd	349000	425000	405000	305000	366000	238000	Ω

Linear Model for 8mm pHEMT

L - via = 0.0135 nH (9x)

Gate Pads (8x)

Drain Pads (8x)

UPC UPC UPC UPC UPC UPC UPC UPC

8 7 6 5 4 3 2 1

9 10 11 12 13 14 15 16

Unmatched S-parameter for 8mm pHEMT

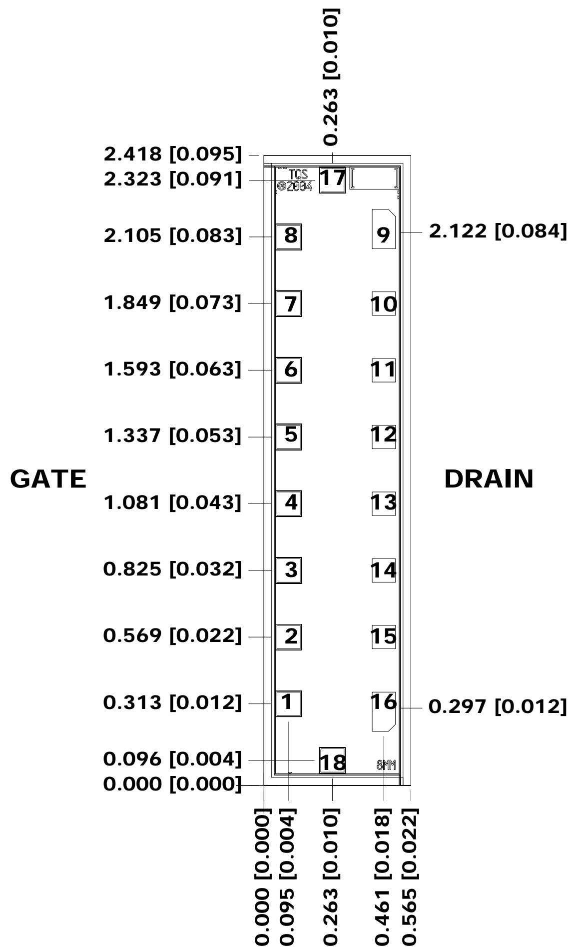
Bias Conditions: Vd=12V, Idq=600mA

Frequency (GHz)	s11 dB	s11 ang deg	s21 dB	s21 ang deg	s12 dB	s12 ang deg	s22 dB	s22 ang deg
0.5	-0.219	-165.41	19.074	93.88	-39.703	6.63	-2.938	-175.24
1	-0.218	-172.72	13.085	86.79	-39.685	2.29	-2.874	-176.34
1.5	-0.216	-175.20	9.538	82.14	-39.733	0.41	-2.829	-176.18
2	-0.215	-176.46	6.995	78.13	-39.810	-0.81	-2.776	-175.74
2.5	-0.213	-177.22	4.997	74.41	-39.911	-1.72	-2.713	-175.22
3	-0.210	-177.75	3.340	70.85	-40.033	-2.43	-2.641	-174.70
3.5	-0.207	-178.14	1.917	67.41	-40.175	-2.98	-2.561	-174.21
4	-0.204	-178.44	0.662	64.08	-40.335	-3.39	-2.475	-173.77
4.5	-0.201	-178.69	-0.466	60.84	-40.512	-3.65	-2.384	-173.39
5	-0.197	-178.90	-1.494	57.69	-40.703	-3.77	-2.290	-173.06
5.5	-0.194	-179.08	-2.443	54.62	-40.907	-3.73	-2.196	-172.80
6	-0.190	-179.25	-3.326	51.64	-41.121	-3.54	-2.101	-172.60
6.5	-0.187	-179.39	-4.154	48.74	-41.344	-3.19	-2.007	-172.45
7	-0.183	-179.53	-4.935	45.92	-41.574	-2.67	-1.914	-172.36
7.5	-0.179	-179.66	-5.676	43.18	-41.807	-1.99	-1.824	-172.31
8	-0.175	-179.78	-6.382	40.52	-42.041	-1.13	-1.737	-172.31
8.5	-0.172	-179.89	-7.055	37.94	-42.275	-0.11	-1.653	-172.34
9	-0.168	180.00	-7.701	35.44	-42.504	1.08	-1.573	-172.40
9.5	-0.165	179.89	-8.321	33.01	-42.727	2.43	-1.497	-172.50
10	-0.162	179.79	-8.917	30.65	-42.943	3.95	-1.424	-172.62
10.5	-0.159	179.68	-9.492	28.36	-43.148	5.62	-1.354	-172.76
11	-0.155	179.58	-10.047	26.14	-43.342	7.45	-1.289	-172.92
11.5	-0.153	179.49	-10.583	23.98	-43.522	9.43	-1.226	-173.09
12	-0.150	179.39	-11.103	21.88	-43.683	11.58	-1.168	-173.28
12.5	-0.147	179.30	-11.606	19.85	-43.822	13.87	-1.112	-173.47
13	-0.144	179.20	-12.094	17.87	-43.933	16.28	-1.060	-173.68
13.5	-0.142	179.11	-12.569	15.94	-44.015	18.79	-1.010	-173.90
14	-0.139	179.02	-13.029	14.07	-44.066	21.36	-0.964	-174.12
14.5	-0.137	178.93	-13.477	12.25	-44.085	23.96	-0.920	-174.34
15	-0.135	178.84	-13.913	10.48	-44.074	26.55	-0.878	-174.57
15.5	-0.133	178.75	-14.338	8.75	-44.033	29.12	-0.839	-174.80
16	-0.131	178.66	-14.752	7.06	-43.965	31.64	-0.803	-175.03
16.5	-0.129	178.58	-15.156	5.42	-43.871	34.10	-0.768	-175.26
17	-0.128	178.49	-15.551	3.81	-43.755	36.47	-0.735	-175.49
17.5	-0.126	178.40	-15.936	2.25	-43.619	38.75	-0.704	-175.73
18	-0.124	178.32	-16.314	0.72	-43.465	40.93	-0.674	-175.96
18.5	-0.123	178.23	-16.683	-0.78	-43.296	43.00	-0.647	-176.19
19	-0.122	178.15	-17.044	-2.24	-43.114	44.96	-0.620	-176.42
19.5	-0.120	178.06	-17.398	-3.67	-42.922	46.81	-0.595	-176.65
20	-0.119	177.98	-17.746	-5.08	-42.721	48.56	-0.572	-176.88
20.5	-0.118	177.90	-18.087	-6.45	-42.512	50.19	-0.549	-177.10
21	-0.117	177.82	-18.422	-7.80	-42.299	51.72	-0.528	-177.33
21.5	-0.116	177.73	-18.751	-9.12	-42.082	53.15	-0.508	-177.55
22	-0.115	177.65	-19.076	-10.41	-41.862	54.48	-0.489	-177.77
22.5	-0.114	177.57	-19.395	-11.69	-41.640	55.71	-0.470	-177.99
23	-0.113	177.49	-19.709	-12.94	-41.418	56.86	-0.453	-178.20
23.5	-0.112	177.41	-20.020	-14.17	-41.196	57.91	-0.436	-178.42
24	-0.111	177.33	-20.326	-15.38	-40.975	58.88	-0.421	-178.63
24.5	-0.110	177.25	-20.628	-16.57	-40.755	59.77	-0.406	-178.84
25	-0.110	177.17	-20.927	-17.74	-40.539	60.58	-0.391	-179.05
25.5	-0.109	177.09	-21.222	-18.90	-40.327	61.31	-0.377	-179.25
26	-0.109	177.01	-21.515	-20.04	-40.121	61.98	-0.364	-179.46

Note: The s-parameters are calculated by connecting nodes 1-8 together, and nodes 9-16 together to form a 2-port network.

TriQuint Semiconductor: Phone (972)994-8465 Fax (972)994-8504 Info-mmw@tqs.com www.triquint.com Rev -

Mechanical Drawing



Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)

GND IS BACKSIDE OF MMIC

Bond pads #1-8:	**(Gate)**	**0.090 x 0.090 (0.004 x 0.004)**
Bond pads #9-16:	**(Drain)**	**0.090 x 0.090 (0.004 x 0.004)**
Bond pad #17:	**(Vg*)**	**0.090 x 0.090 (0.004 x 0.004)**
Bond pad #18:	**(Vg*)**	**0.090 x 0.090 (0.004 x 0.004)**

***Note: Bond pads #17 & 18 are alternate gate pads that can be used for paralleling FETs.**

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handing, assembly and test.

Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300 °C for 30 sec
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use flux
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200 °C.