

Description

The μPB100422 is a very high-speed 100K interface ECL RAM organized as 256 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 7 or 10 ns maximum are available in 24-pin ceramic DIP or ceramic flatpack packaging.

Features

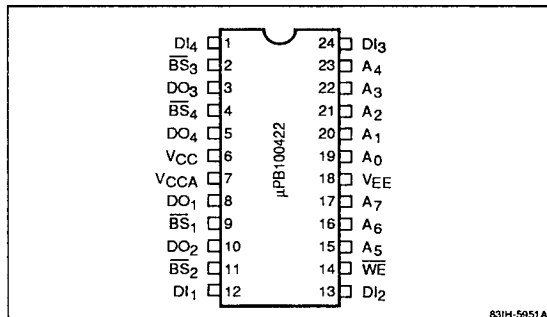
- 256-word x 4-bit organization
- 100K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin ceramic DIP or 24-pin ceramic flatpack packaging

Ordering Information

Part Number	Access Time (max)	Supply Current (min)	Package
μPB100422D-7	7 ns	-220 mA	24-pin ceramic DIP
D-10	10 ns		
μPB100422B-7	7 ns	-220 mA	24-pin ceramic flatpack
B-10	10 ns		

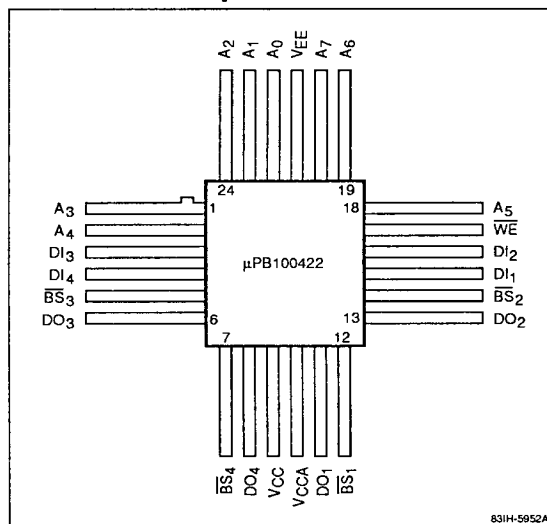
Pin Configurations

24-Pin Ceramic DIP



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24-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A ₀ - A ₇	Addresses
BS ₁ - BS ₄	Block select inputs
DI ₁ - DI ₄	Data inputs
DO ₁ - DO ₄	Data outputs
WE	Write enable
V _{CC}	Power supply (current switches and bias driver)
V _{CCA}	Power supply (output devices)
V _{EE}	Power supply

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C _{IN}		4		pF
Output capacitance	C _{OUT}		5		pF

Absolute Maximum Ratings

Supply voltage, V _{EE} to V _{CC}	-7.0 to +0.5 V
Input voltage, V _{IN}	V _{EE} to +0.5 V
Output current, I _{OUT}	-30 to +0.1 mA
Storage temperature, T _{STG}	-65 to +150°C
Storage temperature, under bias, T _{STG} (bias)	-55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

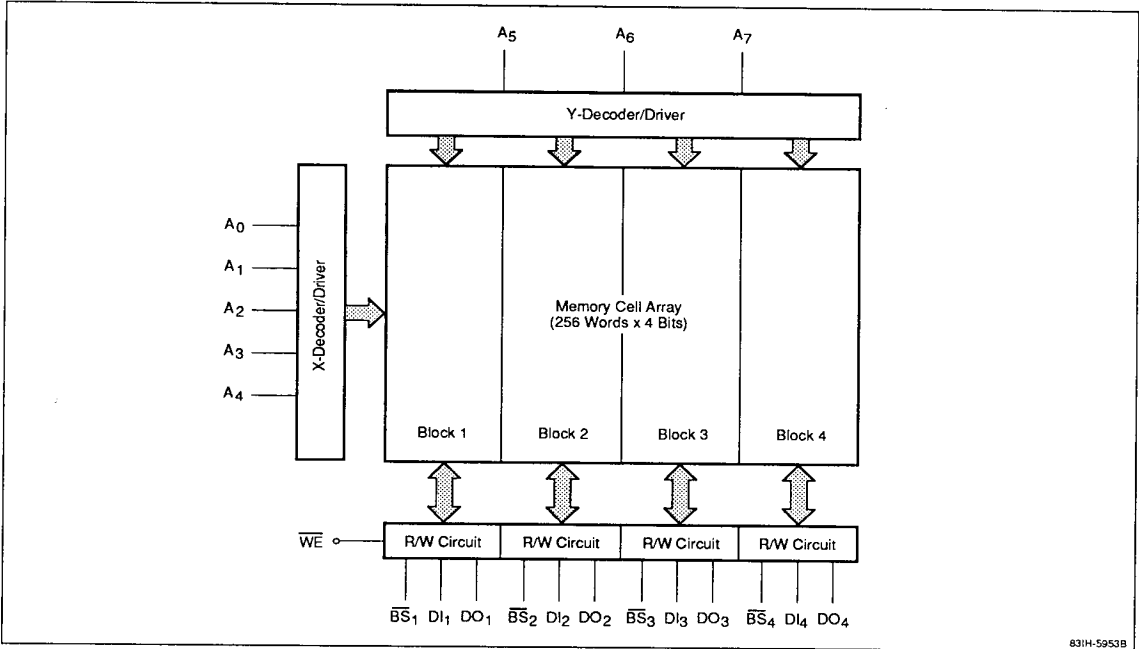
Truth Table

BS	WE	DI	DO	Function
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data Valid	Read

Notes:

- (1) The Block Select Input for each of the four memory blocks is used independently as shown in the block diagram.

Block Diagram



831H-5953B

DC Characteristics

$T_A = 0$ to $+85^\circ\text{C}$; $V_{EE} = -4.5\text{ V}$; output load = $50\ \Omega$ to -2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	-1025		-880	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output voltage, low	V_{OL}	-1810		-1620	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output threshold voltage, high	V_{OHC}	-1035			mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Output threshold voltage, low	V_{OLC}			-1610	mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Input voltage, high	V_{IH}	-1165		-880	mV	For all inputs
Input voltage, low	V_{IL}	-1810		-1475	mV	For all inputs
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{BS}_1$ - $\overline{BS}_4$: $V_{IN} = V_{IL}$ min
		-50			μA	For all others: $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	-220			mA	All inputs and outputs open

Notes:

- (1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

$T_A = 0$ to $+85^\circ\text{C}$; $V_{EE} = -4.5\text{ V} \pm 5\%$

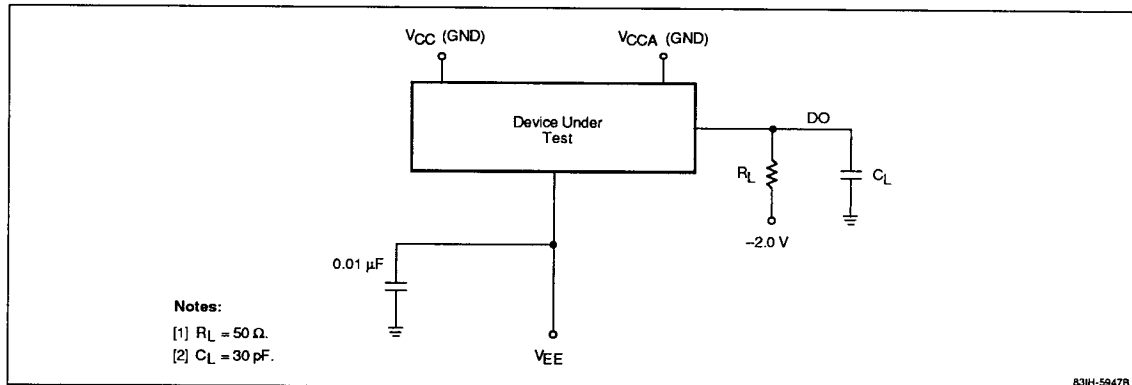
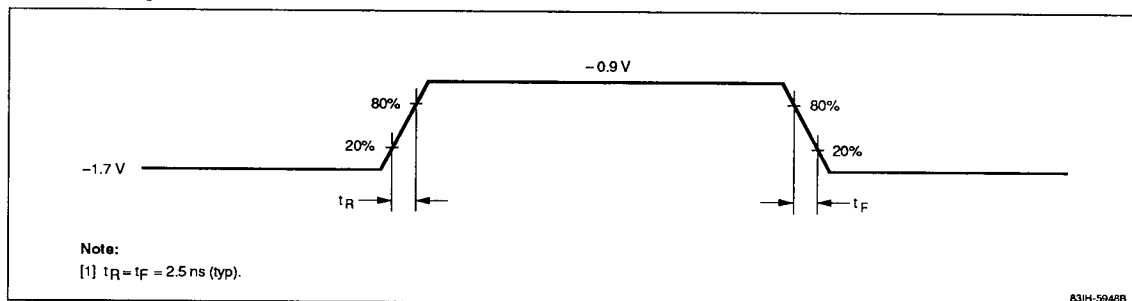
Parameter	Symbol	μPB100422-7			μPB100422-10			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Read Operation									
Block select access time	t _{ABS}			5			5	ns	
Block select recovery time	t _{RBS}			5			5	ns	
Address access time	t _{AA}			7			10	ns	
Write Operation									
Write pulse width	t _W	5			6			ns	
Data setup time	t _{WSD}	1			2			ns	
Data hold time	t _{WHD}	1			2			ns	
Address setup time	t _{WSA}	1			2			ns	
Address hold time	t _{WHA}	1			2			ns	
Block select setup time	t _{WSBS}	1			2			ns	
Block select hold time	t _{WHBS}	1			2			ns	
Write disable time	t _{WS}			5			5	ns	
Write recovery time	t _{WR}			6			9	ns	
Output Rise and Fall Times									
Output rise time	t _R		2			2		ns	
Output fall time	t _F		2			2		ns	

Notes:

- (1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.
- (2) All timing measurements are referenced to 50% input levels.
- (3) The output load is shown in figure 1.
- (4) Input transition times are shown in figure 2.

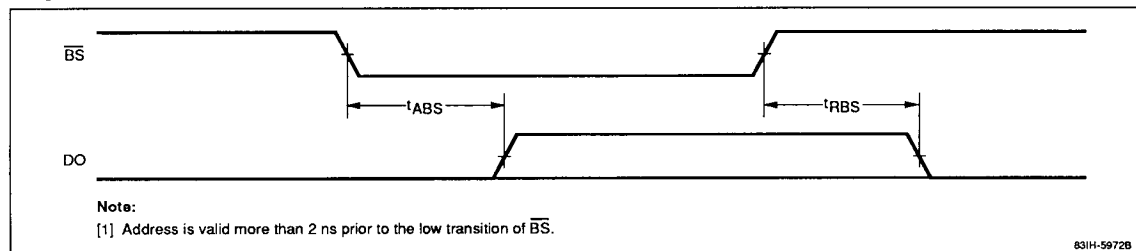
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Figure 1. Loading Conditions Test Circuit**Figure 2. Input Pulse**

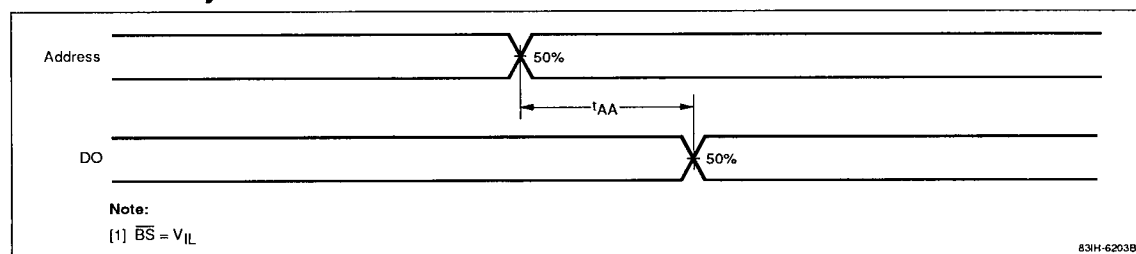
Timing Waveforms

Chip Select Access

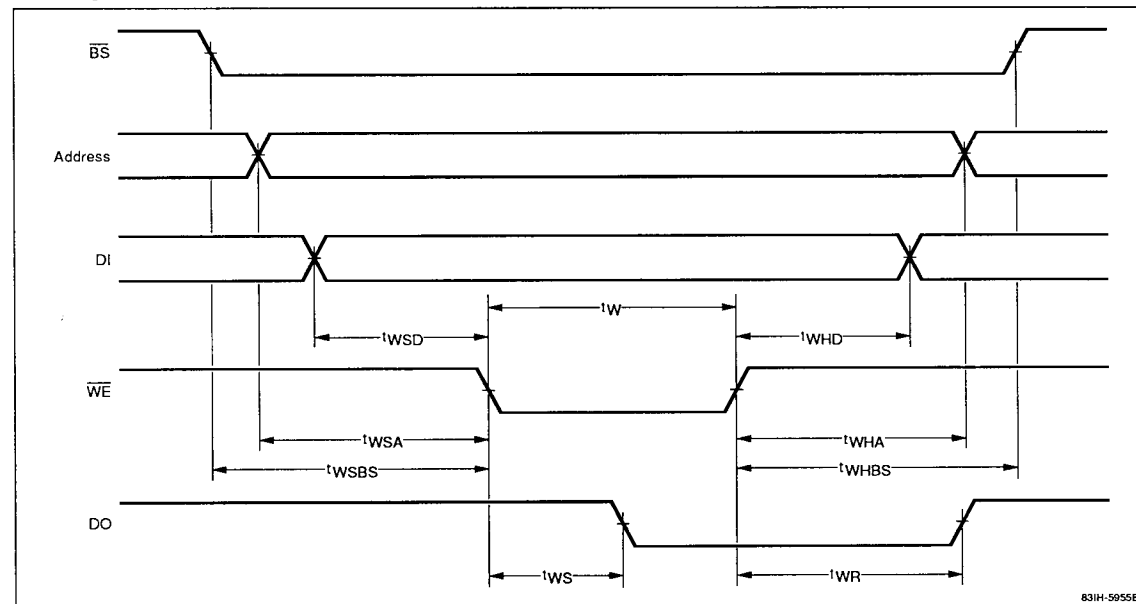


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Address Access Cycle



Write Cycle



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