128Kx72 Synchronous Flow Through SRAM MODULE *ADVANCED**

FEATURES

- Fast Access Times of 10 and 11ns
- Fast $\overline{OE}$ Access Time of 5ns
- Packaging:
  - 164 lead, 27.8mm (1.09 inch) square CQFP, 4.57mm (0.180 inch) high
- Single +3.3V - 5% +10% Power Supply
- 5V-Tolerant Common Data I/O
- Individual Byte Write Control and Global Write
- Flow through Data Bus
- Commercial, Industrial and Military Temperature Ranges
- Write Pass-through Capability
- Clock Controlled, Registered, Address, Data and Control
- Internally Self-timed Write Cycle
- Burst Control Pin (Interleaved or Linear Burst)

** This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG. 1 PIN CONFIGURATION FOR WY128K72V-XG5X

TOP VIEW

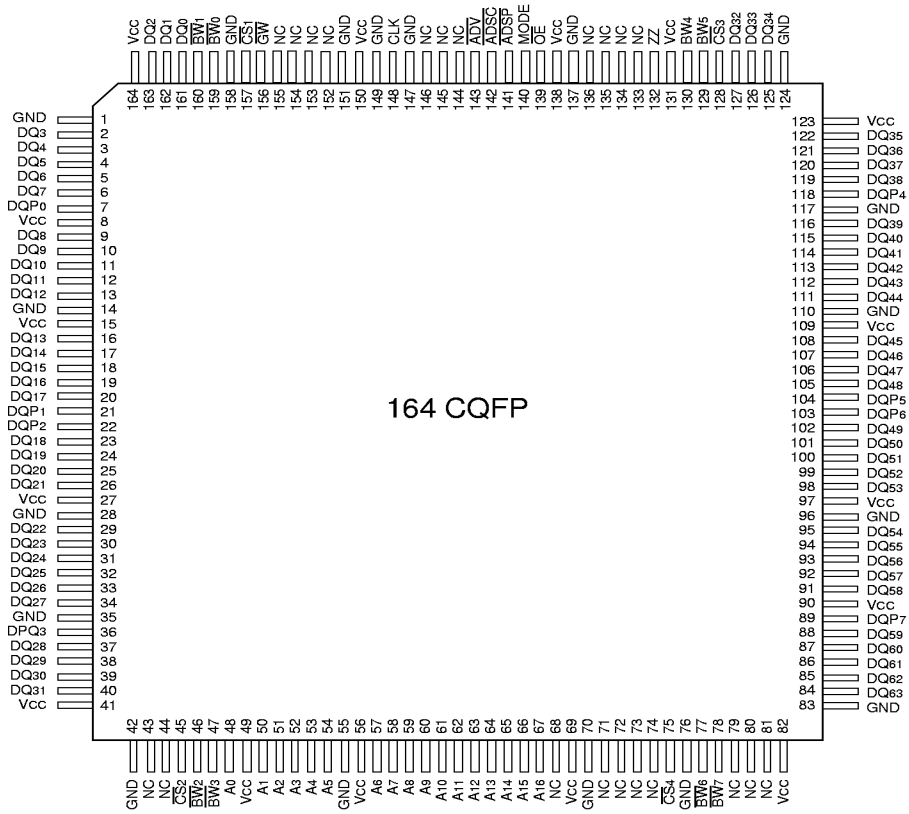
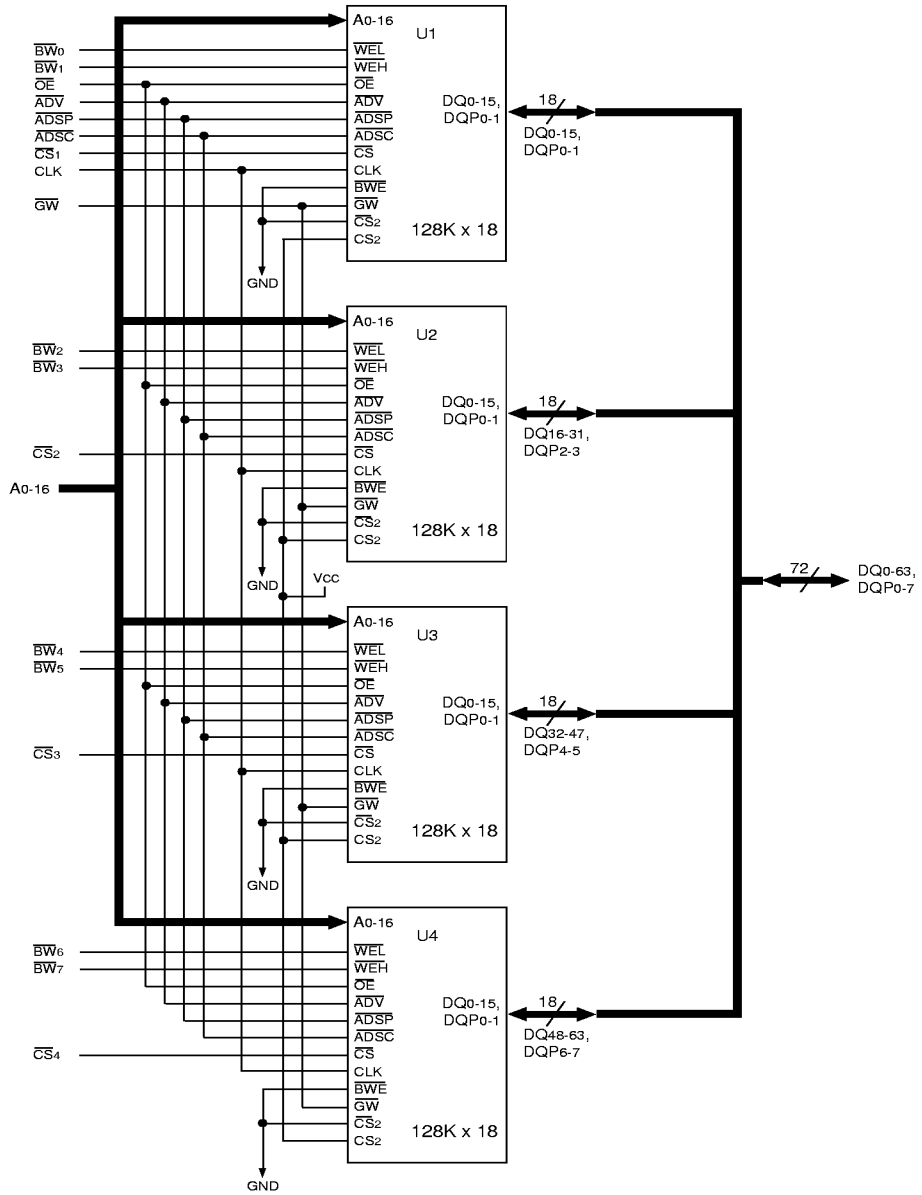


FIG. 2 BLOCK DIAGRAM FOR WY128K72V-XG5X



PIN CONFIGURATION DESCRIPTION

Pin	Type	Description
A_{0-16}	Input	Synchronous Address: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
$\overline{BW}_{0-7}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle
$\overline{GW}$	Input	Global Write: This active LOW input allows a full 72-bit WRITE to occur independent of the $\overline{BW}_{0-7}$ lines and must meet the setup and hold times around the rising edge of CLK.
CLK	Input	Clock: This signal registers the address, data, chip select, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet the setup and hold times around the clock's rising edge.
$\overline{CS}_{1-4}$	Input	Synchronous Chip Select Inputs: These active LOW inputs are used to enable each device and condition the internal use of $\overline{ADSP}$. $\overline{CS}x$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input	Output Enable: This active LOW, asynchronous input enables the Data I/O output drivers.
$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal bus counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, $\overline{ADV}$ must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated.
$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of byte write enables and $\overline{ADSC}$, but dependent upon $\overline{CS}x$. $\overline{ADSP}$ is ignored if $\overline{CS}x$ is HIGH.
$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CS}x$ is LOW. $\overline{ADSC}$ is also used to place the chip into power-down state when $\overline{CS}x$ is HIGH.
MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects a linear burst. NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.
ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
DQ_{0-63}	Input/Output	Data Inputs/Outputs: Input data must meet setup and hold times around the rising edge of CLK.
DQP_{0-7}	Input/Output	Parity Data I/Os
Vcc	Supply	Power Supply (3.3V)
GND	Supply	Ground
NC	–	Not Connected

INTERLEAVED BURST ADDRESS TABLE
(Mode = NC/High)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE
(Mode = Low)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS

Function	$\overline{GW}$	$\overline{BW_0}$	$\overline{BW_1}$
READ	H	H	H
WRITE byte "0"	H	L	H
WRITE byte "1"	H	H	L
WRITE all bytes	H	L	L
WRITE all bytes	L	X	X

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Voltage on Vccq Supply Relative to Vss	-0.5	+4.6	V
Voltage on Vcc Supply Relative to Vss	-0.5	+4.6	V
V_{IN}	-0.5	Vcc +0.5	V
Short Circuit Output Current		100	mA
Operating Temperature	-55	+125	°C
Storage Temperature	-65	+150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a Stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

Function	Address Used	$\overline{CSx}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	L	X	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power Down	None	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	L	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic Low.
2. For $\overline{WRITE}$ = L means any one or more byte enable signals ($\overline{BW}$x) are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$ = H for all $\overline{BW}$x, $\overline{GW}$ HIGH.
3. All inputs except $\overline{OE}$ and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Suspending burst generates wait cycle.
5. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ cycle at the L-H edge of CLK. A WRITE cycle is performed by setting one or more byte write enables and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Max	Units
Input High (Logic 1) Voltage (1, 2)	V_{IH}		2.0	V_{CC} + 0.3	V
Input Low (Logic 0) Voltage (1, 2)	V_{IL}		-0.3	0.8	V
Input Leakage Current (3)	I_{LI}	$0V \le V_{IN} \le V_{CC}$ (Data In)	-4	4	µA
Output Leakage Current	I_{LO}	Output(s) disabled, $0V \le V_{IN} \le V_{CC}$	-1	1	µA
Output High Voltage (1, 3)	V_{OH}	I_{OH} = -4.0mA	2.4		V
Output Low Voltage (1, 3)	V_{OL}	I_{OL} = 8mA		0.4	V
Supply Voltage (1)	V_{CC}		3.135	3.6	V

NOTES:

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +4.6V$ for $t \le t_{KC}/2$ for $I \le 20mA$
   Undershoot: $V_{IL} \le -0.7V$ for $t \le t_{KC}/2$ for $I \le 20mA$
   Power-up: $V_{IH} \le +3.6V$ and $V_{DD} \le 3.135V$ for $t \le 200ms$
3. MODE pin has an internal pull-up. This pin exhibits an input leakage current of ±40µA.
4. The load used for V_{OH}, V_{OL} testing is shown in the DC Output Load Equivalent.

DC CHARACTERISTICS

(V_{CC} = 3.3V -5% +10%)

Parameter	Conditions	Symbol	Max	Unit
Power Supply Current: Operating (1,2)	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ t_{KC} min; Vcc = Max; outputs open	I_{CC}	800	mA
Power Supply Current: Idle (1,2)	Device selected; Vcc = Max; ADSC, ADSP, ADV, GW, BWx ≥ V_{IH}; all inputs ≤ Vss + 0.2 or ≥ Vcc - 0.2; cycle time ≥ t_{KC} min; outputs open	I_{CC1}	240	mA
CMOS Standby (2)	Device deselected; Vcc = Max; all inputs ≤ Vss + 0.2 or ≥ Vcc - 0.2; all inputs static; CLK frequency = 0	I_{SB2}	40	mA
TTL Standby (2)	Device deselected; Vcc = Max; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; Vcc = Max; CLK frequency = 0	I_{SB3}	100	mA
Clock Running (2)	Device deselected; Vcc = Max; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; CLK cycle time ≥ t_{KC} min	I_{SB4}	240	mA

NOTES:

1. Icc is specified with no output current and increases with greater output loading and faster cycle times.
2. "Device Deselected" means the device is in Power-Down mode as defined in the truth table. "Device Selected" means the device is active.

CAPACITANCE

Description	Conditions	Symbol	Max	Units
Input Capacitance ($\overline{CS}$x, $\overline{BW}$x)	T_A = 25°C; f = 1MHz	C_I	15	pF
Input Capacitance ($\overline{OE}$, $\overline{ADSP}$, $\overline{ADSC}$, $\overline{GW}$)		C_I	40	pF
Input/Output Capacitance (DQ)		C_O	15	pF
Address Capacitance		C_A	40	pF
Clock Capacitance		C_{CK}	40	pF

NOTE: These parameters are guaranteed by design but not tested.

AC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 3.3V -5% +10%)

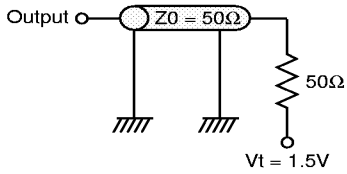
Parameter	Symbol	-10		-11		Unit
		Min	Max	Min	Max	
Clock						
Clock Cycle Time	t_{KC}	15		15		ns
Clock Frequency	t_{KF}		66		66	MHz
Clock HIGH Time	t_{KH}	5		5		ns
Clock LOW Time	t_{KL}	5		5		ns
Output Times						
Clock to Output Valid	t_{KQ}		10		11	ns
Clock to Output Invalid (2)	t_{KQX}	3		3		ns
Clock to Output in Low-Z (2, 3, 4)	t_{KQLZ}	4		4		ns
$\overline{\text{Clock}}$ to Output in High-Z (2, 3, 4)	t_{KQHZ}		5.0		5.0	ns
$\overline{\text{OE}}$ to Output Valid (5)	t_{OEQ}		5.0		5.0	ns
$\overline{\text{OE}}$ to Output in Low-Z (2, 3, 4)	t_{OELZ}	0		0		ns
OE to Output in High-Z (2, 3, 4)	t_{OEHZ}		5.0		5.0	ns
Setup Times						
Address (6, 7)	t_{AS}	2.5		2.5		ns
Address Status ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$) (6, 7)	t_{ADSS}	2.5		2.5		ns
Address Advance ($\overline{\text{ADV}}$) (6, 7)	t_{AAS}	2.5		2.5		ns
Byte Write Enables ($\overline{\text{BW}}$x, $\overline{\text{GW}}$) (6, 7)	t_{WS}	2.5		2.5		ns
Data-In (6, 7)	t_{DS}	2.5		2.5		ns
Chip Select ($\overline{\text{CS}}$) (6, 7)	t_{CSS}	2.5		2.5		ns
Hold Times						
Address (6, 7)	t_{AH}	0.5		0.5		ns
Address Status ($\overline{\text{ADSC}}$, $\overline{\text{ADSP}}$) (6, 7)	t_{ADSH}	0.5		0.5		ns
Address Advance ($\overline{\text{ADV}}$) (6, 7)	t_{AAH}	0.5		0.5		ns
Byte Write Enables ($\overline{\text{BW}}$x, $\overline{\text{GW}}$) (6, 7)	t_{WH}	0.5		0.5		ns
Data-In (6, 7)	t_{DH}	0.5		0.5		ns
Chip Select ($\overline{\text{CS}}$) (6, 7)	t_{CSH}	0.5		0.5		ns

NOTES:

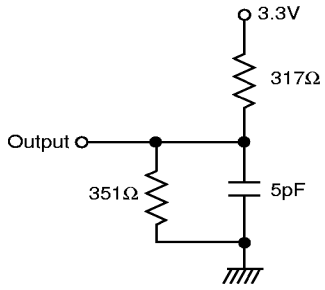
1. Test conditions as specified with the output loading as shown in the "Output Load Equivalent" unless otherwise noted.
2. This parameter is measured with output load as shown in "Output Load Equivalent".
3. This parameter is sampled.
4. Transition is measured ±500mV from steady state voltage.
5. $\overline{\text{OE}}$ is a "don't care" when a byte write enable is sampled LOW.
6. A READ cycle is defined by byte write enables all HIGH or $\overline{\text{ADSP}}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{\text{ADSP}}$ HIGH for the required setup and hold times.
7. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is LOW and chip enabled. All other synchronous inputs must meet specified setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip select must be valid at each rising edge of CLK when either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$ is LOW to remain enabled.

FIG. 3 OUTPUT LOADS

AC Output Load Equivalent



DC Output Load Equivalent



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IH} = (Vcc/2.2) +1.5	V
	V_{IL} = (Vcc/2.2) -1.5	
Input Rise and Fall Times	1	ns
Input Timing Reference Level	Vcc/2.2	V
Output Timing Reference Level	Vcc/2.2	V
Output Load	See figures at left	

SNOOZE MODE

SNOOZE MODE is a low current "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

The ZZ pin is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any access pending when the device enters SNOOZE MODE is not guaranteed to complete sucessfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are complete.

SNOOZE MODE ELECTRICAL CHARACTERISTICS

Description	Conditions	Symbol	Min	Max	Units
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2Z}		40	mA
ZZ active to input ignored (1)		t_{ZZ}		t_{KC}	ns
ZZ inactive to input sampled (1)		t_{RZZ}	t_{KC}		ns
ZZ active to snooze current (1)		t_{ZZI}		t_{KC}	ns
ZZ inactive to exit snooze current (1)		t_{RZZI}	0		ns

NOTE:
1. These parameters are guaranteed by design but not tested.

FIG. 4 SNOOZE MODE WAVEFORM

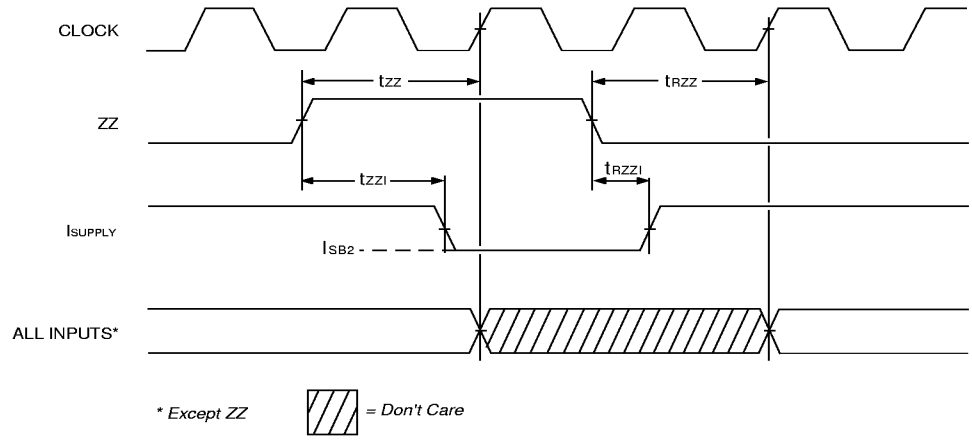
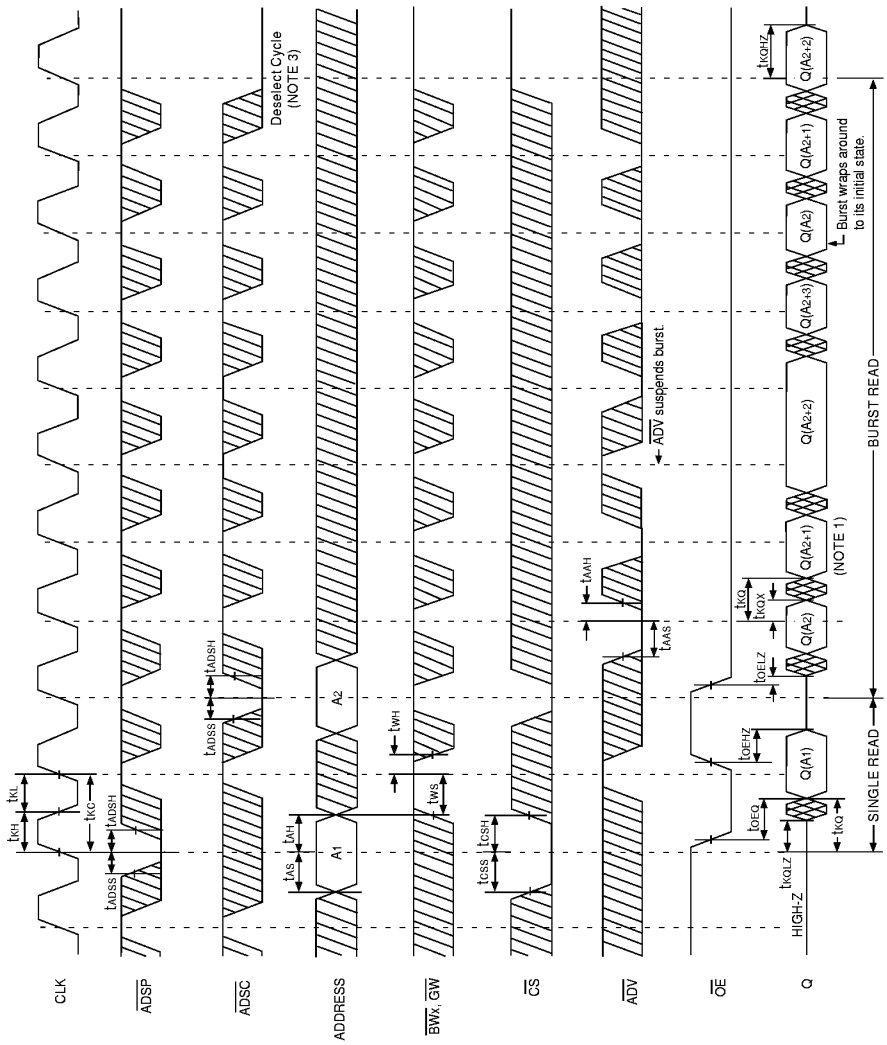
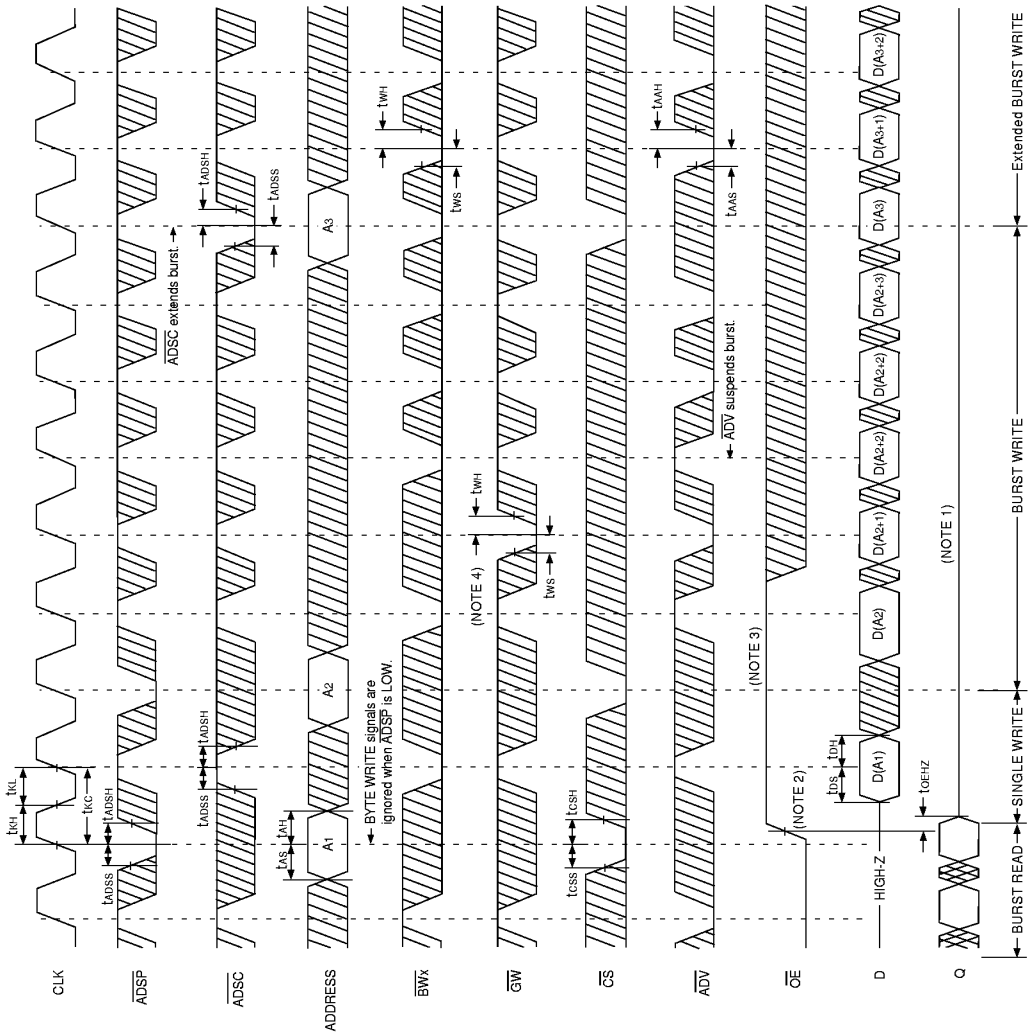


FIG. 5 TIMING WAVEFORM OF READ CYCLE



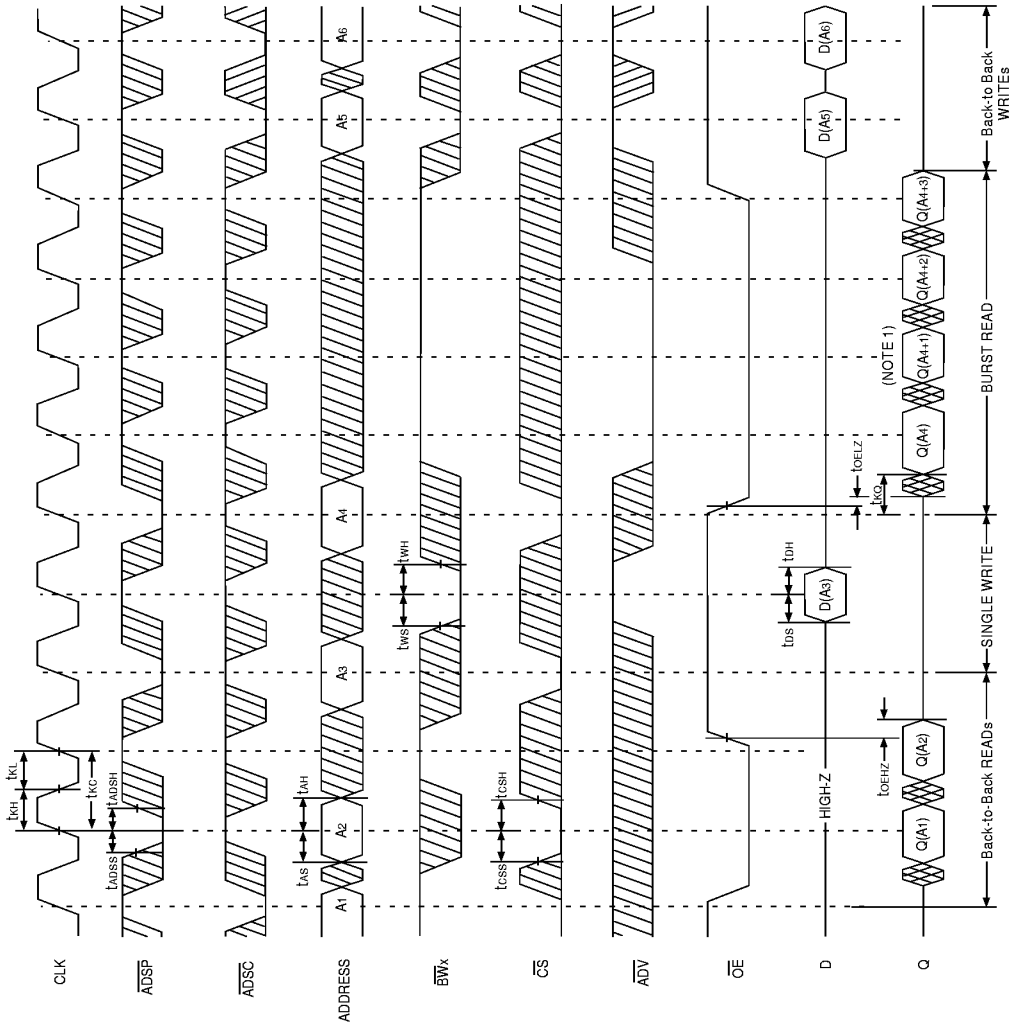
NOTES:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. Timing is shown assuming that the device was not enabled before entering into this sequence.
3. Outputs are disabled tKQHZ after deselect.

FIG. 6 TIMING WAVEFORM OF WRITE CYCLE



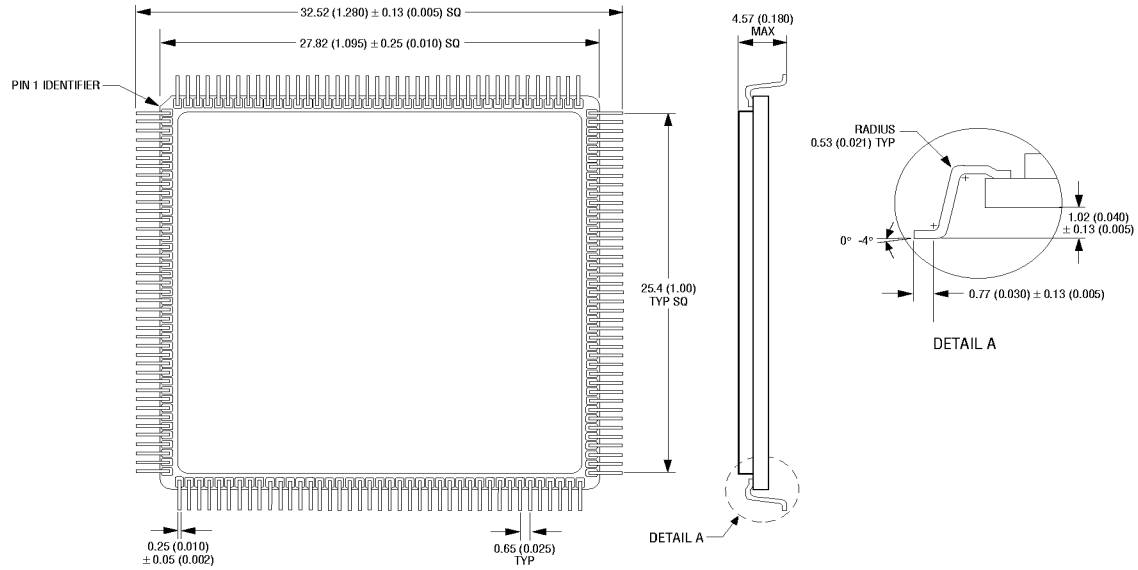
NOTES:
1. D(A2) refers to input for address A2. D(A2+1) refers to output for the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to loaded address.
4. Full-width WRITE can be initiated by $\overline{GW}$ LOW; or $\overline{GW}$ HIGH and $\overline{BW}_{0-7}$ LOW.

FIG. 7 TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE



NOTES:
1. Q(A4) refers to input for address A4. D(A4+1) refers to output for the next internal burst address following A4.
2. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP, ADSC or ADV cycle is performed.
3. GW is HIGH.
4. Back-to-back READs may be controlled by either ADSP or ADSC.

PACKAGE DIMENSION 164 LEAD CQFP



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W Y 128K 72 V - XX G5 X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:
G5 = 27.8 mm Ceramic Quad Flatpack, CQFP

ACCESS TIME (ns)

Voltage Supply 3.3V -5% +10%

ORGANIZATION, 128Kx72

Synchronous Flow Through SRAM

WHITE MICROELECTRONICS