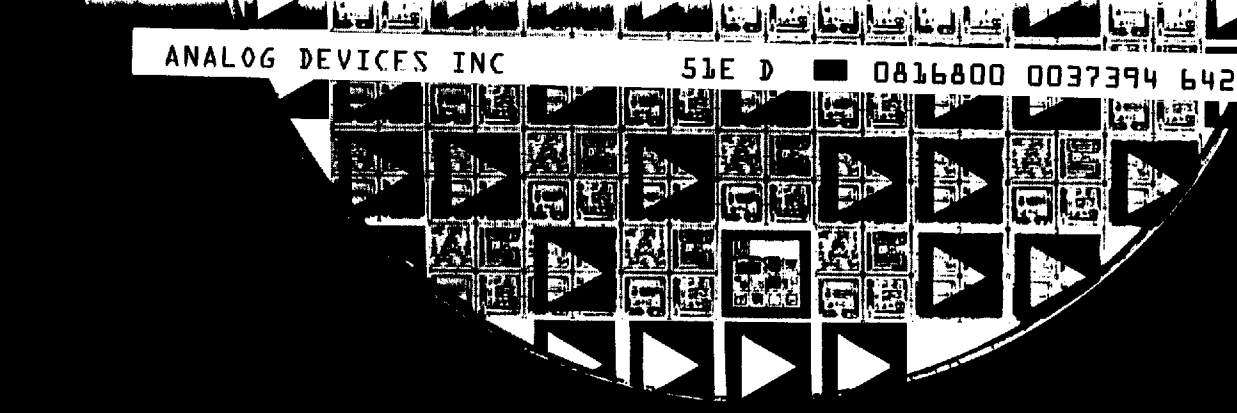


MIXED SIGNAL ASIC

DESIGNERS' GUIDE

MIXED SIGNAL BIPOLAR PROCESSES

ANALOG DEVICES

ANALOG DEVICES

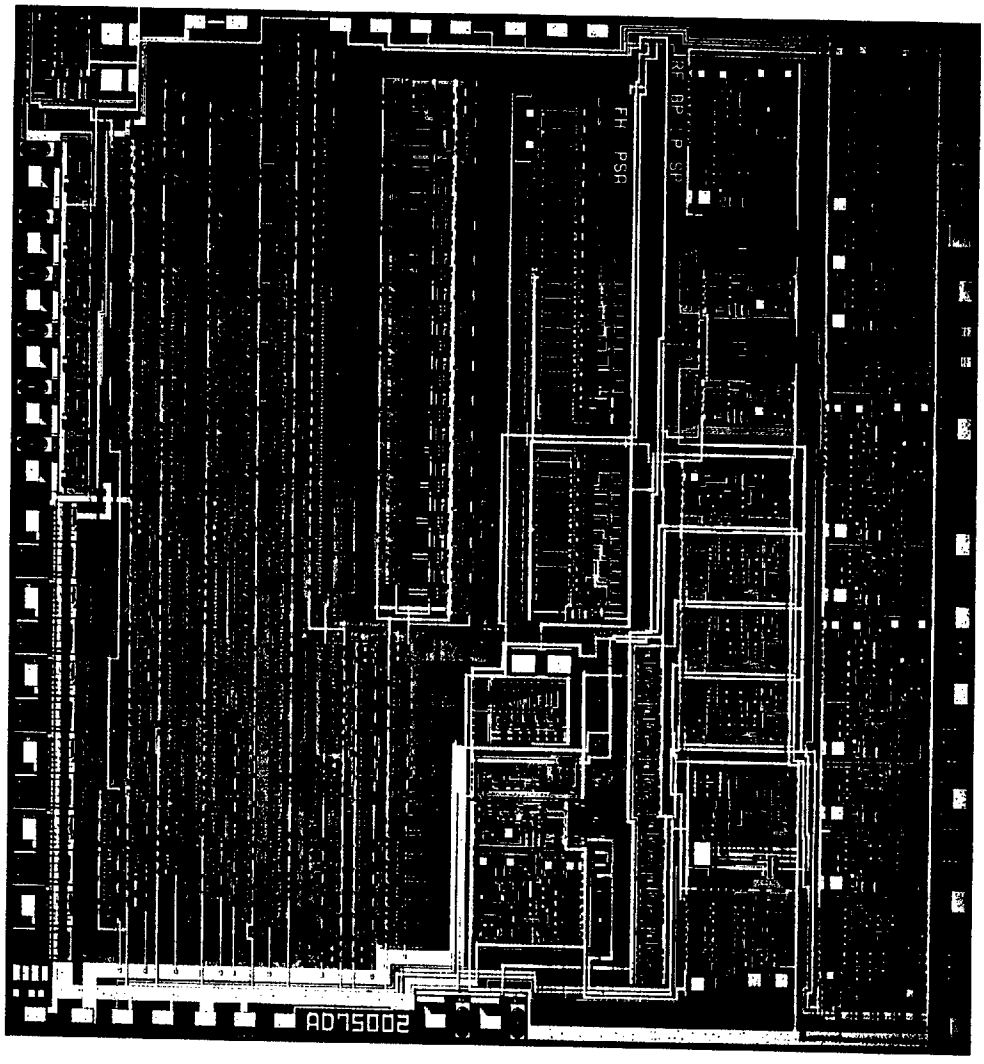


Table of Contents

B

Analog/ Digital ASICs and USICs

Introduction

Analog Devices has long been a leader in standard integrated circuits for precision analog and data acquisition applications. Now we offer a full spectrum of capabilities in precision Application-Specific and User-Specific ICs (ASICs and USICs). These chip-level systems can implement multi-channel designs with 12-bit accuracy and 16-bit precision that formerly required board-level solutions.

ASICs and USICs offer many benefits to the systems designer. Because they integrate many functions on a chip, they reduce system size, weight, and assembly time, and increase system reliability. High integration also improves matching among channels, simplifies interfaces, increases performance, and reduces power consumption. Also, USICs are tailor-made for only one customer, assuring design exclusivity and security. Together, these benefits make possible whole new classes of systems, and improve the performance/price ratio of existing designs.

Full-custom parts optimize performance and space requirements, while cell-based semi-custom parts reduce development time and engineering expense. Development costs often can be reduced further by tailoring a Linear System Macro, a pre-defined system-on-a-chip, to your application.

Analog Devices fabricates chips in 3 BiCMOS processes, offering a range of supply voltages from +5 volts to ±15 volts. Our comprehensive cell libraries contain most of the functions in our standard product catalogs. These include such industry standards as the AD7572 12-bit analog-to-digital converter, AD667 12-bit digital-to-analog converter, AD-OP27 operational amplifier, AD584 voltage reference, and AD585 sample-and-hold.

Using powerful industry-standard as well as proprietary CAD systems, Analog's experienced design engineers design, simulate, and lay out your circuit. Our design centers are located in Massachusetts, England, and Ireland. We fabricate, assemble, and test chips in our MIL-38510 certified facilities in the USA and Europe, and assemble and test chips in our facility in Asia.

Features

Range of bipolar/CMOS processes

- Precision bipolar & FET linear devices
- Dense high-speed CMOS logic
- Laser-trimmable thin-film resistors
- Power supplies from +5 V to ±15 V

Extensive standard-cell libraries

- Cells based on ADI catalog parts
- 8-bit, 12-bit, and 16-bit data converters
- Amplifiers, switches, and references
- Switched-capacitor and active filters
- Logic including PLAs and UART

Benefits

- High-accuracy data converters and signal processing
- Combined analog and digital functions on one chip
- High levels of functional integration
- Wide dynamic range
- Short turn times for complex circuits

Analog/ Digital BiCMOS Processes

Analog Devices' ASICs and USICs are fabricated in our three bipolar-CMOS processes, which are also used for volume production of standard ICs. These processes are ideally suited for applications in data acquisition, instrumentation, avionics, industrial automation, telecommunications and other control and signal-processing systems.

The BiMOS II and Linear-Compatible CMOS (LC^2MOS) processes combine bipolar and CMOS transistors on one chip. These processes provide functional density an order of magnitude greater than earlier mixed-signal processes, and make it possible to integrate over 20,000 devices on one chip.

The bipolar transistors provide precision, low-noise, low-offset input stages and moderate-power output stages. The CMOS devices make dense, low-power logic; switches for analog multiplexers, data converters, and switched-capacitor filters; and high-impedance input stages and current sources for linear circuitry. The thin-film resistors are very stable over time and temperature, and may be laser trimmed for precise matching and absolute values.

The major difference among the processes is their recommended supply voltages. BiMOS II is designed to run on ±12 V supplies. Most BiMOS II cells are designed to accommodate ±5 V signals, although some cells can handle ±8 or ±10 V swings. LC^2MOS has two variants: one runs on ±5 V supplies, with ±3 V signal swings; the other runs on ±15 V, with ±10 V swings.

BiMOS and LC^2MOS also differ in the devices they offer and hence the applications for which they are best suited. BiMOS, an n-well process, has a high-quality NPN transistor and thin-film resistors which have lower temperature coefficients than those in LC^2MOS. These features make BiMOS a particularly good match for low-frequency and instrumentation applications.

LC^2MOS is a p-well process, and has a higher-frequency PNP transistor. LC^2MOS also includes a JFET for very low input noise at high input impedance, and a Zener diode with better noise and drift than those of a band-gap reference. These characteristics make it well suited for AC signal-processing applications. LC^2MOS also has higher logic density and higher-speed logic than BiMOS II.

Analog's BiCMOS processes are inherently safe against latch-up. Furthermore, protection circuitry can yield parts that exceed industry and MIL standards on ESD and latch-up. (However, the lowest input currents are obtained with minimal protection circuitry.)

Analog Devices will review your application and recommend the appropriate bipolar-CMOS process for your needs.

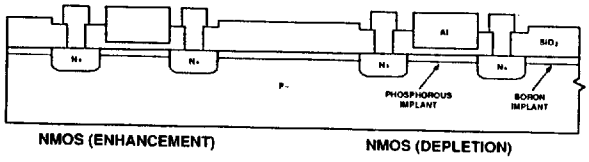
The BiMOS Process

BiMOS II features high-quality NPN transistors that have very low noise, tight matching, and high Early voltage. These characteristics make it possible to build high-performance amplifiers and comparators with low-offset input stages and excellent linearity, as well as stable band-gap references.

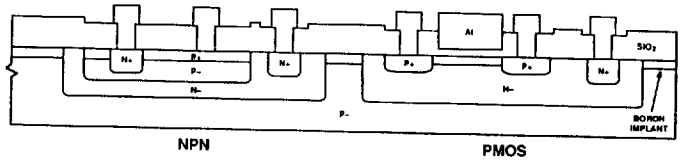
The exceptionally stable thin-film resistors are used in precision data converters, programmable-gain amplifiers, and other linear circuits.

BiMOS II uses two levels of metal interconnect as well as self-aligned polysilicon to reduce chip area and layout time.

CROSS SECTIONAL VIEW OF BIMOS II PROCESS



NMOS (ENHANCEMENT) NMOS (DEPLETION)



NPN PMOS

Typical Device Characteristics

BJTs	NPN	L PNP
BV_{CEO}	20 V	35 V
Beta	100–250	50
V_A	100 V	
V_{BE} match	100 μV	
f_T	300 MHz	6 MHz
Vertical PNP (not shown)		
BV_{CEO}	75 V	
Beta	100	
f_T	15 MHz	
MOSFETs	**NMOS**	**PMOS**
BV_{DSS}	26 V	26 V
V_{TO}	1.0 V	0.7 V
Thin-film Resistors		
Sheet ρ	100 or 1 kΩ/sq.	
TC*	< 50 ppm/°C	
Tolerance*	< 0.1%	
Matching*	< 0.01%	
Range*	50 to 20 kΩ best; to 5 MΩ possible	

*Specifications given are for 1 kΩ/square material.

The LC²MOS Processes

Typical Device Characteristics for ±5 V Process

MOSFETs	NMOS	PMOS
B_{VDSS}	> 10 V	> 10 V
V_{TO}	+0.75 V	−1.0 V
BJTs	**V PNP**	**Substr. NPN**
BV_{CEO}	> 10 V	35 V
Beta	> 100	> 100
f_T	1 GHz	6 MHz
N-channel JFET		
BV	> 8 V	
V_P	−2 V	
Noise*	12 nV/√Hz	
Leakage	< 1 nA @ 125°C	
Buried Zener Diode		
V_Z	6.1 V	
TC	+2.5 mV/°C	
Noise	60 nV/√Hz	
Thin-film Resistors		
Sheet ρ	2 kΩ/square	
TC	−350 ppm/°C max	
Matching	< ±0.1%, typical; < ±0.02%, trimmed	
Range	1 kΩ to 1 MΩ	

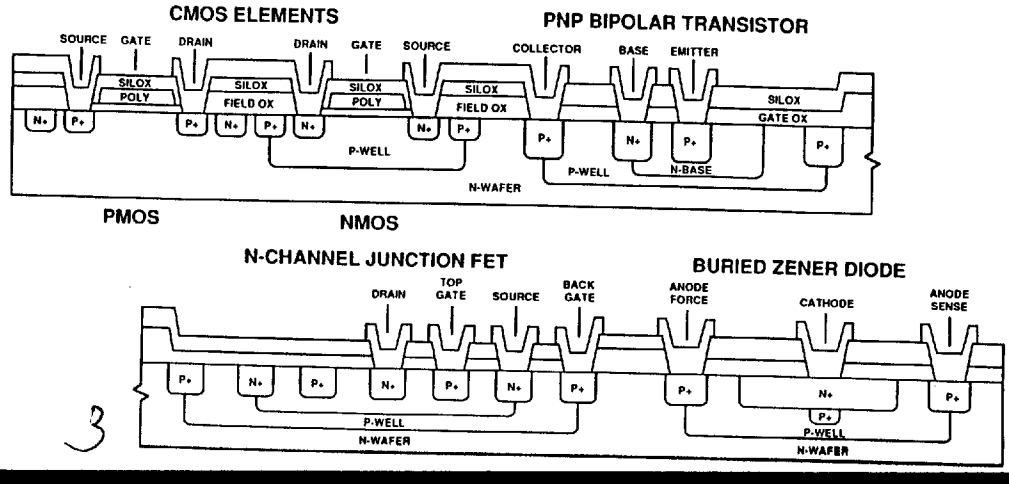
*@ 10 Hz for 1500 square micron active gate area and 100 μA drain current

LC²MOS has two variants: one with 2- to 3-μ design rules and 500-Å gate oxide for ±5-volt supplies, and one with 5-μ design rules and 1000-Å gate oxide for ±15-volt supply circuits.

For highly complex system-on-a-chip products, the ±5-V cell library offers the best combination of circuit density and power dissipation. This library is designed for ±3-volt signal swings (2.12 V RMS). It can implement systems of better than 12-bit quality, with noise + distortion levels below −75 dB. Gate delays, as measured in a ring oscillator, are typically 1.5 ns.

The ±15-volt process can accommodate signal swings of up to ±10 V (7.07 V RMS). However, the higher power dissipation and larger geometries result in lower levels of integration than can be achieved with the finer geometry processes.

LC²MOS PROCESS



3

Estimating Circuit Feasibility

The following pages contain listings of the cell libraries for the ±5-V LC²MOS and the ±12-V BiMOS II processes. These processes are independent, and cells from the two processes cannot be combined on one chip.

The specifications shown represent typical performance at 25°C. The equivalent standard products listed indicate the general function and performance of the cell; the cell may not match all performance parameters of the standard part.

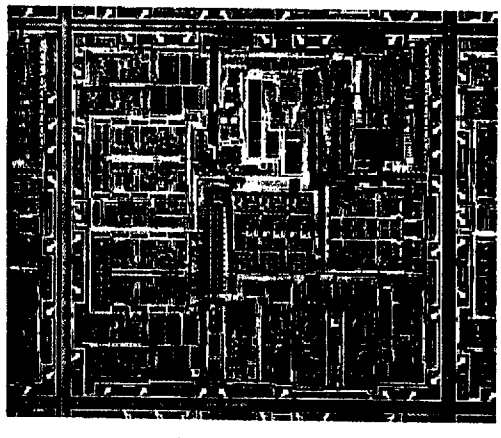
The listings indicate for each cell its approximate power consumption and die area. These will help to determine whether a given circuit concept will fit within constraints of power dissipation and die size.

Excessive power dissipation can affect the linearity, offset, and drift of precision analog circuits. Power dissipation per chip should be limited to about 250 mW in LC²MOS and 750 mW in BiMOS II.

The total die area can be estimated by adding the total cell area, including input/output pads. The figures in the tables include area for interconnecting the cells. As a rule of thumb, circuits up to 12 units in LC²MOS, and 20 units in BiMOS II are common.

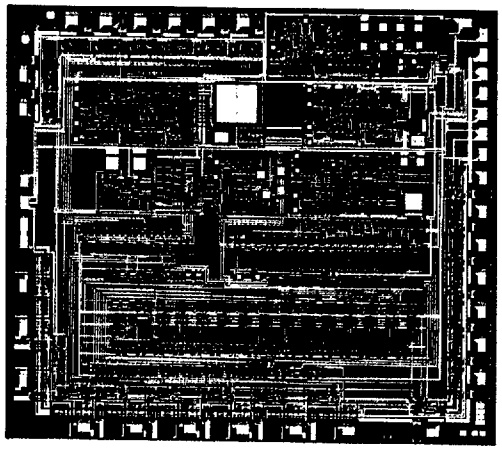
Size estimates larger than these should be reviewed by ADI engineers. Often, they can develop novel architectural approaches that exploit the combination of devices on the same chip to reduce the die size.

Two examples of these calculations follow.



LC²MOS Custom Data Acquisition System

#	Cell Name	Cell Function	Unit Area	Total Area
7	AMPJH10	Opamp	0.50	3.5
4	AMPBL10	Opamp	0.45	1.8
6	AMPMH60	Opamp	0.10	0.6
1	REFB20	Reference	0.35	0.35
1	ADC1010	Converter	3.15	3.15
900		Gates	0.0018	1.62
28		Pads	0.034	0.95
TOTAL				12.0



BiMOS II LSM Data Acquisition System

#	Cell Name	Cell Function	Unit Area	Total Area
1	MUX4210	Multiplexer	0.6	0.6
1	SHATI10	Sample/hold	1.3	1.3
1	RPGA10	Gain network	0.5	0.5
1	REFV05	Reference	0.6	0.6
1	ADC1210	Converter	5.2	5.2
1	CLK11	Oscillator	0.6	0.6
200		Gates	0.008	1.6
28		Pads	0.06	1.7
TOTAL				12.1

LC²MOS Analog Cell Library

The LC²MOS cell library is designed for a variety of applications in data acquisition, control, and instrumentation. Many of the cells were derived from Analog Devices' standard products.

The following cells are designed to operate from ±5-volt supplies and handle ±3-volt signals. Input signals outside this range can be attenuated by on-chip thin-film resistors.

All DAC and ADC cells have ±1-LSB differential and integral nonlinearity over the −55 to +125°C temperature range.

The opamps and filters are described further on the following page.

LC²MOS Analog Cells for ±5-Volt Supplies

Name	Function	Power	Size	Equivalent	Comments
L10/AMPBL10	Opamp w/ PNP inputs	15	0.45	ADOP27	General-purpose bipolar; $Z_{OUT} \leq 2\ k\Omega + 100\ pF$
L10/AMPBH20	Opamp w/ PNP inputs	12	0.40	ADOP27	General-purpose bipolar; $Z_{OUT} \leq 50\ k\Omega + 10\ pF$
L10/AMPBH30	Opamp w/ PNP Darlington inputs	15	0.45	ADOP27	Low-bias-current bipolar; $Z_{OUT} \leq 2\ k\Omega + 100\ pF$
L10/AMPBH40	Opamp w/ PNP Darlington inputs	12	0.40	ADOP27	Low-bias-current bipolar; $Z_{OUT} \leq 50\ k\Omega + 10\ pF$
L10/AMPJH10	Opamp w/ JFET inputs	20	0.50	AD711	General-purpose JFET; $Z_{OUT} \leq 2\ k\Omega + 100\ pF$
L10/AMPJH20	Opamp w/ JFET inputs	17	0.45	AD711	General-purpose JFET; $Z_{OUT} \leq 50\ k\Omega + 10\ pF$
L10/AMPMH50	Opamp w/ PMOS inputs	7	0.15	—	AC & audio applications; $Z_{OUT} \leq 2\ k\Omega + 100\ pF$
L10/AMPMH60	Opamp w/ PMOS inputs	4	0.10	—	AC & audio applications; $Z_{OUT} \leq 50\ k\Omega + 10\ pF$
L10/REFZ10	Buried-Zener reference	13	1.95	AD580	Fast 12-bit ADC applications
L10/REFB10	+3-volt bandgap w/ JFET amp	7	0.35	AD580	Audio- and sub-audio-band applications
L10/REFB20	+3-volt bandgap w/ NMOS amp	7	0.35	AD580	Audio-band applications
L10/SHATF10	Classical track-and-hold	10	1.75	AD585	12-bit DC precision
L10/SHASF10	Switched-capacitor sample-and-hold	7	0.20	—	S/(N+THD) > 80 dB, 200 Hz to 20 kHz
L10/ADC0810	8-bit ADC w/ track-and-hold & ref	30	1.15	AD7569 ADC	Conversion time ≤ 2 µs; $V_{IN} \leq 2.5$ V
L10/ADC1010	10-bit ADC w/ SHA	30	3.15	AD7579	Conversion time ≤ 10 µs
L10/ADC1210	12-bit ADC	40	2.95	AD7878/70	Conversion time ≤ 10 µs
L10/ADC04	14-bit ADC	40	3.00	AD7871	Conversion time ≤ 10 µs
L10/DAC0810	8-bit DAC w/ ref; voltage output	30	0.85	AD7569 DAC	$V_{OUT} = \pm 2.5$ V
L10/DAC02	8-bit DAC; current output	10	0.45	AD7524	$I_{OUT} = V_{IN}/10\ k\Omega$
L10/DAC03	8-bit DAC; voltage output;	28	0.45	AD7569 DAC	Use w/ +3-volt reference and buffer amp
L10/DAC1010	10-bit DAC; voltage output;	50	1.15	AD7579	Use w/ +3-volt reference and buffer amp
L10/DAC1210	12-bit DAC; voltage output;	40	1.65	AD7848	Use w/ +3-volt reference and buffer amp
L10/DAC1410	14-bit DAC; voltage output;	40	2.00	AD7840	Use w/ +3-volt reference and buffer amp
(Compiled)	Switched-cap filter section	5	0.60	—	Up to 10 orders; Chebyshev or elliptic
(Compiled)	Active RC filter	5	0.25	—	Up to 3 orders; Rausch or Sallen & Key
	Bonding pad	0	0.034	—	Includes ESD protection

Notes:
Power is typical consumption in mW. The recommended maximum total power dissipation is 250 mW.
Size is shown in arbitrary units of area. The recommended maximum total die area is 12 units.
Equivalents illustrate the function of the cell and are not exact replacements for the standard products listed.

Operational Amplifiers

The broad range of transistor types in LC²MOS — bipolar, JFET, and MOS — allows a variety of opamps, optimizing various performance parameters. Bipolar opamps give very high gain, low offset voltage, low noise, and good rejection of common-mode signals and power-supply noise. JFET opamps offer high slew rate, low input current, and low noise. MOS amps are very compact and are used typically in switched-capacitor filters.

The following table compares the performance of eight of the opamp cells in the ±5-volt LC²MOS library. All are designed to operate with ±3-volt signals.

LC²MOS Operational Amplifier Cells for ±5-Volt Supplies

Cell Name	Input	Gain dB	GBW MHz	Slew Rate V/μs	V_{os} mV	I_B nA	I_{os} nA	Noise nV/√Hz @ 10 Hz	CMRR dB @ DC	PSRR dB @ 100 kHz	Load kΩ‖pF
L10/AMPBL1O	PNP	118	2.5	2.5	±0.5	350	15	22	110	65	2‖100
L10/AMPBH20	PNP	118	2.5	2.5	±0.5	350	15	22	110	65	50‖10
L10/AMPBH30	PNP	118	1.5	1.2	±1.0	3.0	0.2	120	110	65	2‖100
L10/AMPBH40	PNP	118	1.5	1.2	±1.0	3.0	0.2	120	110	65	50‖10
L10/AMPJH10	JFET	110	5.0	13	±1.0	0.005	0.001	80	100	55	2‖100
L10/AMPJH20	JFET	110	5.0	13	±1.0	0.005	0.001	80	100	55	50‖10
L10/AMPMH50	PMOS	110	1.5	6.0	±10	—	—	3,000	100	60	2‖100
L10/AMPMH60	PMOS	110	1.5	6.0	±10	—	—	3,000	100	60	50‖10

Compiled Filters

Filter compilers can generate both switched-capacitor filters and active RC filters.

Switched-cap filters (SCFs) can be made in Chebyshev or elliptic topologies up to 10th-order. Noise and distortion levels are compatible with 12-bit systems, with S/(N+THD)≥75 dB. SCFs provide the most accurate corner frequencies, and low noise and distortion. In the audio band, SCFs can provide passband ripple ≤0.1 dB and frequency accuracy of better than 1%.

Below 100 Hz, SCF accuracy and noise performance degrade, and above 50 kHz, distortion increases. Active RC filters provide better solutions at these frequencies.

Active RC filters can go up to 3 orders, in Sallen & Key or Rausch topologies. They can use laser-trimmed resistors and on- or off-chip capacitors. Corner frequencies can range from 1 kHz to 1 MHz with on-chip capacitors. These filters offer even lower noise and distortion than SCFs, and do not suffer from aliasing. However, they are larger and less accurate in corner frequency, limited to ±15% accuracy.

±15-Volt Availability

A cell library is also available in the version of LC²MOS optimized for operation from ±15 V supplies. This library is aimed at the integration of primarily analog systems, typically comprising op-amps with bipolar or JFET inputs, comparators, inverters, muxes, and precision gain switching. The range of functions available is similar to the ±5 V library.

In estimating the maximum level of integration, allow for the following scaling factors relative to the ±5 V process:

Analog cell area:	1.5 ×
Digital cell area:	4 ×
Power:	3 ×

LC²MOS Digital Cell Library

The digital CMOS cell library for the ±5-volt LC²MOS process operates from a single 5-V supply and interfaces directly to TTL or CMOS signals. It contains both static gates and synchronous dynamic logic using 2-phase clocking. The dynamic logic is comparable in density to the static logic used in gate arrays. The maximum toggle rate is 8 MHz and bus access times are less than 50 ns at T_{amb} = −40 to +85°C. At T_{amb} = −55 to +125°C, the maximum toggle rate is 5 MHz.

Compiled Logic Blocks

Compilers make several types of complex macro blocks for logic and memory.

Function	Features	Capability
RAM	Dynamic 4-transistor cell	Up to 1,024 bits
ROM	Dynamic	Up to 10,000 bits
Adder	With carry-look-ahead	Up to 16 bits; < 125 ns cycle
Counter	With enable and preset	Up to 16 bits

Primitive Logic Cells

Name	Function	Drive	Size	Comments
		pF	units	
L10/DIL1	D-type flip-flop	0.3	0.0039	Requires 2-phase non-overlapping clocks
L10/DIL2	D-type flip-flop	0.7	0.0039	Requires 2-phase non-overlapping clocks
L10/CG1	–(A·(B+C))	—	0.003	CG1–CG3 generate
L10/CG2	–(A+B+C)	—	0.003	2-phase non-overlapping
L10/CG3	Buffer Q/Qbar	6.0	0.0055	clocks
L10/ND2	2-input NAND	0.6	0.0018	Asynchronous static gate
L10/ND3	3-input NAND	0.6	0.0018	Asynchronous static gate
L10/ND4	4-input NAND	0.6	0.0018	Asynchronous static gate
L10/NR2	2-input NOR	0.6	0.0018	Asynchronous static gate
L10/NR3	3-input NOR	0.6	0.0023	Asynchronous static gate
L10/INV1	Inverter	0.6	0.0013	Asynchronous static gate
L10/INV2	Inverter	1.2	0.0018	Asynchronous static gate
L10/XNR1	2-input XNOR	0.6	0.0043	Asynchronous static gate
L10/DMX1	(C1·D1 + C2·D2)	1.2	0.0046	Multiplexer with buffer
L10/PB1	Prebuffer for OB1	—	0.0086	For 2-state TTL-compatible output
L10/PB2	Prebuffer for OB1	—	0.0146	For 3-state TTL-compatible output
L10/OB1	TTL output buffer	50	0.042	Includes static protection and pad
L10/IB3	TTL input buffer	0.6	0.0095	Gated input (synchronous; use with pad)
L10/IB4	TTL input buffer	0.6	0.0055	Direct input (asynchronous; use with pad)

BiMOS II Cell Library

The BiMOS II cell library is designed for a variety of applications in data acquisition, control, and instrumentation. Many of the cells were derived from Analog Devices' standard products.

All analog cells are designed to operate from ±12 V supplies and to handle ±5 V signals. Some cells handle ±10 V signals, and input signals outside this range can be attenuated by on-chip thin-film resistors. Logic cells operate from a +5 V supply.

The CMOS devices in the BiMOS II process implement far denser logic than previous linear processes. However, BiMOS II is not as efficient in realizing large-scale logic functions as digital-only processes. The logic can effectively control the analog functions on the chip, interface to digital circuitry on other chips, and perform a limited amount of digital signal processing, especially bit-serial DSP. Configurable macros include PLAs, filtering, and RMS-to-digital conversion.

The basic gate delay (fanout = 2) is typically 6 ns. The recommended gate count limit is 2,000.

BiMOS II Analog Cells for ±12-Volt Supplies

Name	Function	Power	Size	Equivalent	Comments
B24/TS590	Temperature sensor	7	0.6	AD590	Current output; 1 μA/°K ±0.25%
B24/AMPDA1	Opamp	75	0.9	–	SR >10 V/μs, V_{OS}< 0.1 mV, CMV = ±9 V
B24/AMPLC2	Opamp	25	0.3	–	Bipolar input; I_B < 1 nA
B24/AMPLN1	Opamp	25	0.7	–	Low-noise bipolar; noise < 8 nV/√Hz, V_{OS}< 0.1 mV
B24/AMPPR1	Opamp	25	0.4	–	Protected bipolar input; GBW = 2 MHz
B24/AMPM1	Opamp	25	0.4	–	MOS input; I_B < 5 pA, GBW = 2 MHz
B24/AMPBF1	Buffer amplifier	25	0.6	–	±10 V input swing, gain = 1
B24/AMPBF2	Opamp	30	0.7	–	±10 V output swing
B24/AMPMH10	Opamp	20	0.8	AD711	MOS input; V_{OS}=1 mV, load=2 kΩ‖500 pF
B24/AMPBH10	Opamp	20	0.6	–	GBW=2 MHz, V_{OS} < 0.2 mV, noise < 10 nV/√Hz
B24/IN524	Instrumentation amplifier	48	1.3	AD524	Nonlinearity < 0.01%; CMRR > 100 dB
B24/AMPPG32	Programmable-gain amplifier	140	3.4	–	Constant 1.5 MHz BW at gains 1–128, I_B < 10 pA
B24/RPGA10	Programmable-gain network	3	0.5	–	Use with an op amp for gains of 1–16
B24/CMPBH10	Latching comparator	18	0.5	–	Response time < 100 ns @ 100 μV; I_B < 50 nA
B24/MUX3210	Analog multiplexer	0	0.4	–	8 channels; R_{ON} = 3 kΩ
B24/MUX4210	Analog multiplexer	0	0.6	AD7501	8 channels; R_{ON} = 300 Ω
B24/MUX1616	Crosspoint switch array	0	10.7	–	Latched 16 x 16 analog switch array; R_{ON} = 200 Ω
B24/SCF1	Switched-capacitor filter	51	1.7	1059	2-pole filter; configurable HP/LP/BP/AP/notch
B24/FNOTCH1	Switched-capacitor filter	51	1.7	1059	Notch filter; programmable Q, 50/60 Hz
B24/VCO1	Voltage-controlled oscillator	6	0.6	AD654	To 500 kHz, 0.03% linearity, 80 dB range
B24/CLK11	Fixed-frequency oscillator	6	0.6	–	Gated; factory trimmed; 1 to 12 MHz range
B24/XCO1	Crystal-controlled oscillator	11	0.3	–	Gated; 1 to 12 MHz
B24/MLT1	Analog multiplier	96	6.5	AD534	1 MHz bandwidth; 2% nonlinearity

Notes:
Equivalents illustrate the function of the cell and are not exact replacements for the standard products listed.
Size is shown in arbitrary units. The recommended maximum total die area is 20 units.
Power is typical consumption in mW. The recommended maximum total power dissipation is 750 mW.

BiMOS II Converter and Support Cells for ±12-Volt Supplies

Name	Function	Power	Size	Equivalent	Comments
B24/REFV02	Voltage reference	22	0.6	AD584	2.5-volt bandgap; ±25 ppm/°C, noise < 10 μV p-p
B24/REFV05	Voltage reference	22	0.6	AD584	5.0-volt bandgap; ±25 ppm/°C, noise < 15 μV p-p
B24/REFV10	Voltage reference	22	0.6	AD584	10-volt bandgap; ±25 ppm/°C, noise < 25 μV p-p
B24/SHATI10	Sample-and-hold amplifier	80	1.3	AD585	Acquisition time < 5 μs, Z_{IN} >100 MΩ
B24/SHATI20	Sample-and-hold amplifier	24	1.0	AD389	Acquisition time < 5 μs, pedestal < 2 mV
B24/ADC1210	12-bit A/D converter	99	5.2	AD674	Linear to ±3/4 LSB, $t_{convert}$ = 15 μs
B24/DSSSE1	Sigma-delta modulator ADC	31	0.3	AD652	Linear to 12 bits, clock rates to 5 MHz
B24/DSSD2	Sigma-delta modulator ADC	31	0.4	–	Differential-input version of B12/DSSSE1
B24/DSD1	Sigma-delta modulator ADC	34	2.6	–	16-bit version of B12/DSSD2; auto-zero
B24/DAC1410	14-bit D/A converter	96	3.5	–	Bipolar, current output; t_{settle} = 2 μs
B24/DAC1220	12-bit D/A converter	80	1.3	AD6012	Bipolar, voltage output; t_{settle} = 3 μs
B24/DAC1210	12-bit D/A converter	60	1.2	AD565	Bipolar, I output; t_{settle} = 250 ns
B24/DAC664	12-bit D/A converter	85	2.4	AD664	MOS, 2-quadrant multiplying; V out; t_{settle} = 10 μs
B24/DAC0820	8-bit D/A converter	30	0.8	DAC-08	MOS, I output; t_{settle} = 100 ns
B24/PAD1	Bonding pad	0	0.03	–	Unprotected bonding pad
B24/PADP1	Bonding pad	0	0.06	–	Protected bonding pad

BiMOS II Logic Cells for ±12-Volt Supplies

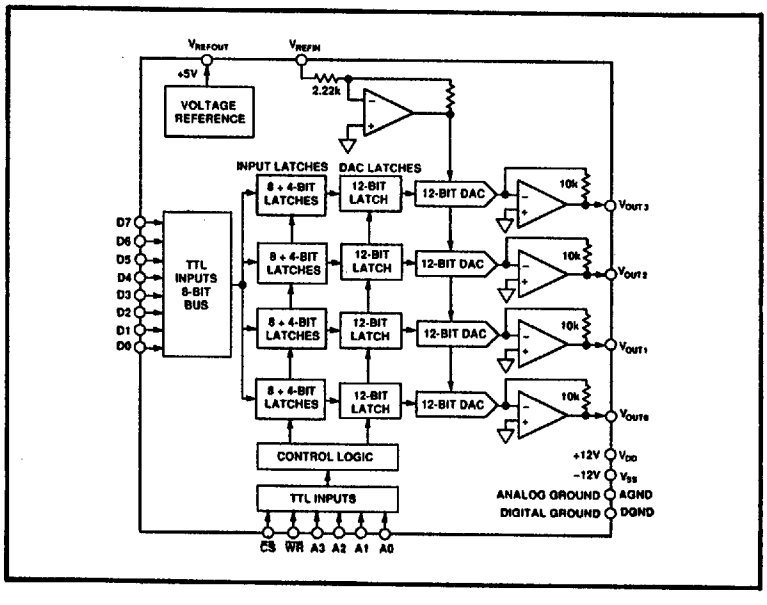
Name	Function	Size	Comments
B24/INVX1	Inverter	0.004	1x drive
B24/INVX4	Inverter	0.019	4x drive
B24/BF1	Buffer	0.004	1x drive
B24/BF4	Buffer	0.019	4x drive
B24/BFC4	Complementary buffer	0.019	4x drive; differential outputs
B24/ND2X1	2-input NAND	0.008	
B24/ND4X1	4-input NAND	0.014	
B24/NR2X1	2-input NOR	0.010	
B24/XOR2	2-input XOR	0.021	
B24/BLPR1	Set/reset latch	0.023	
B24/DFF4	D flip-flop with preset	0.041	
B24/PRTSS21	Synchronous serial port	2.4	Compatible with ADSP-2101; DC – 6 Mbps
B24/PRTAS64	Asynchronous serial port	4.2	Compatible with 6402; DC – 250 kbps, 8 bits
B24/MLT88	Digital multiplier	3.0	Parallel; 8 × 8, 1 μs multiply
B24/RAM88	Dual-port RAM	0.68	8-byte block

Linear System Macros

ADI has designed several chip architectures that may be quickly customized to a specific application. Each Linear System Macro (LSM) is a system-on-a-chip that satisfies a broad range of applications. All of the LSMs shown here all operate with ±12 V supplies and ±5 V signals, except for the AD79015, which operates from ±5 V and handles ±3 V signals.

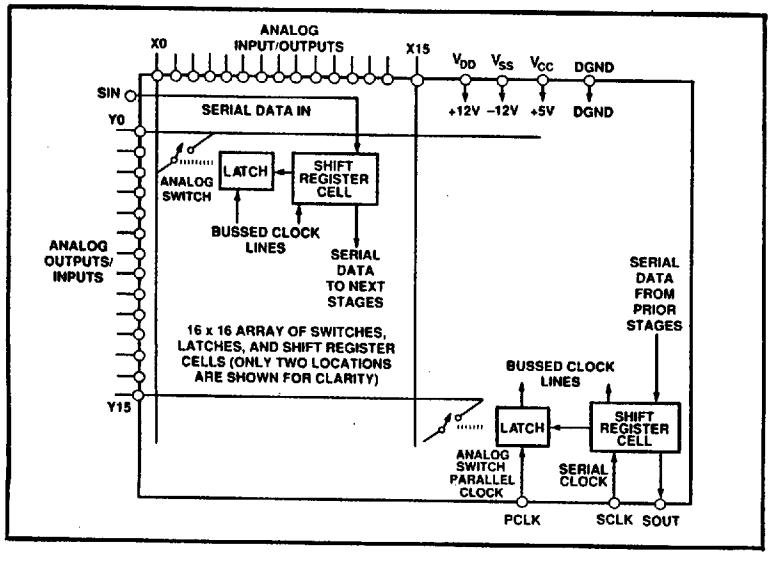
The base LSM can be tailored, through mask changes, to a particular use by changing its functionality, its scale, or its interface. For example, the AD75004 DAC could be modified by allowing a separate reference per channel, adding channels, or providing current outputs.

AD75004 Quad 12-bit Digital-to-Analog Converter



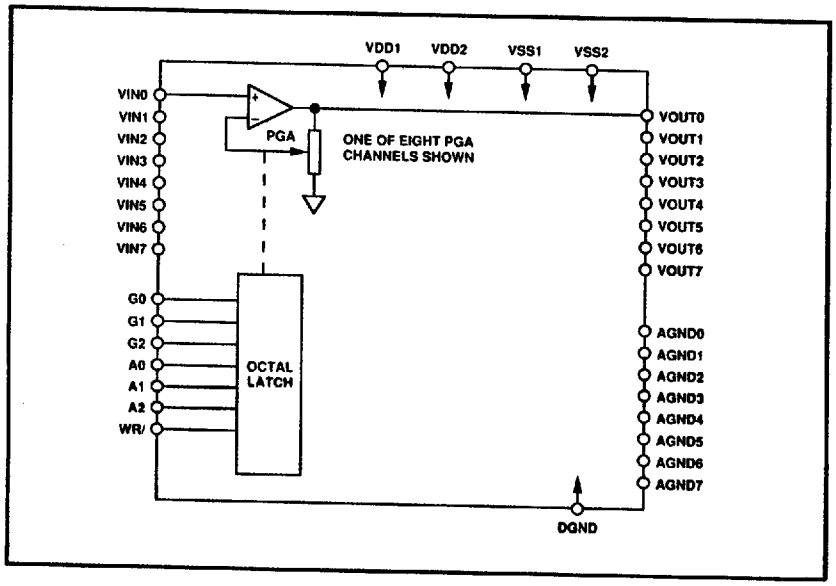
This circuit contains four separate 12-bit digital-to-analog converters with amplifiers for voltage output (±5 V). Each DAC settles to 0.01% within 5 microseconds. Double-buffering latches interface with an 8-bit bus and permit updating of all four channels simultaneously or independently. The chip also includes a 5 volt reference.

AD75019 16 × 16 Crosspoint Switch Array



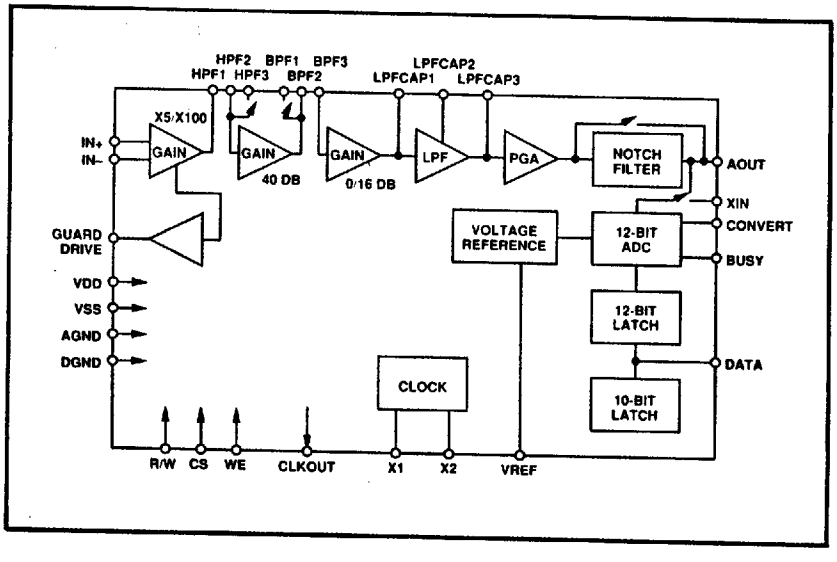
This switch array contains 256 analog switches arranged in a 16 x 16 matrix. Each CMOS switch is fully bi-directional and can handle signals up to the supply rails of ±12 V. Typical on-resistance is under 200 Ω. THD and crosstalk at 1 kHz are better than –80 dB. The chip interfaces via a serial port, and may be cascaded to handle more channels.

AD75068 Octal Programmable-Gain Amplifier



This circuit contains 8 identical programmable-gain amplifiers (PGAs). Each amplifier's gain is independently programmable, from 1 to 128, and is stored in on-chip latches. All amplifiers have high-impedance MOS inputs, and maintain a constant bandwidth of approximately 2 MHz at all gains. This results in excellent phase performance: phase shift is less than 1° at 10 kHz at all gains. The AD75068 is packaged in a 44-terminal J-leaded chip carrier.

AD79015 Small-Signal Data Acquisition System



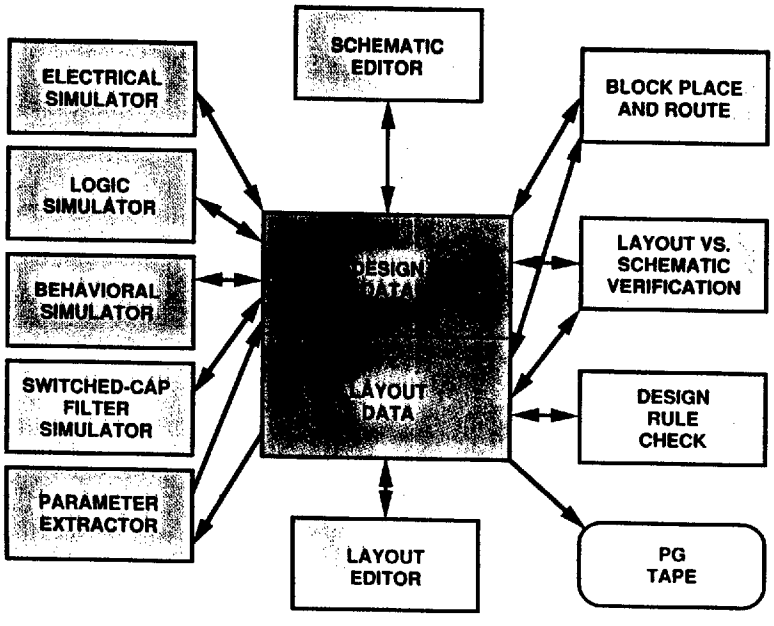
The AD79015 is a complete data acquisition system for low-level signals (e.g., ECG and EEG) with a throughput of 10,000 samples per second. It provides high accuracy, high stability, and functional completeness in a 28-pin PLCC package. It includes a high-performance instrumentation amp, bandpass and notch filters, and a 12-bit ADC with on-chip reference. It also contains a fast 8/12-bit serial port to interface to most microprocessors.

Computer-Aided Design Tools

Designing a high-performance mixed-signal IC is inherently more difficult than designing a gate array. The variety of analog and digital functions requires a cell-based approach. However, the use of powerful tools gives high confidence of functionality at first silicon through thorough simulation and layout verification. Complete computer-generated documentation of all schematics and analog and logic simulation waveforms permits thorough evaluation of Analog's design by your design staff before sign-off for final layout and fabrication.

The overall work flow through the CAD environment is shown below. Key to meeting the special challenges of mixed analog/digital circuitry are the simulation and auto-layout tools, and the unification of design and layout information in a single database. Analog Devices has developed a suite of proprietary computer-aided design tools, called Janus, to address these issues and to implement turn-key designs.

COMPUTER-AIDED DESIGN FLOW

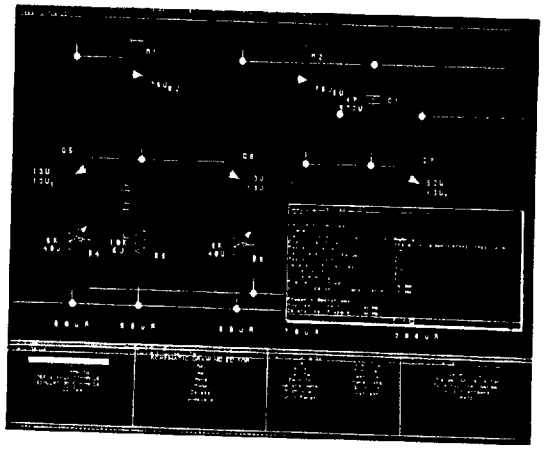


The Janus schematic editor offers numerous time-saving techniques, and provides for specification of such data as wire widths, routing layers, and routing priorities. It automatically generates a netlist used by subsequent tools.

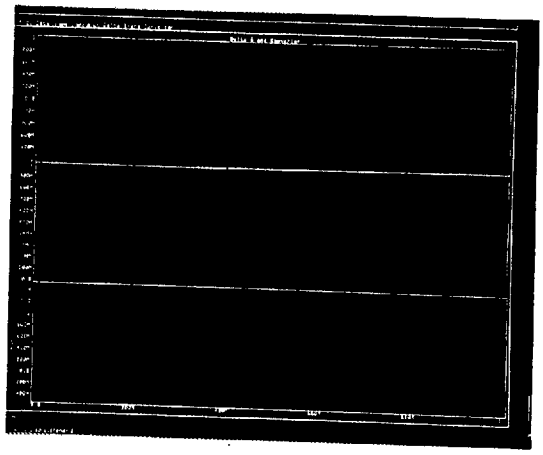
Analog Devices uses several simulators, including electrical, logic, and behavioral types. ADICE, a proprietary enhanced version of the SPICE electrical simulator, gives precision simulation of critical analog sections. It uses Newton-Raphson methods to iteratively solve nonlinear time-dependent simultaneous differential equations. It is efficient for circuits up to about 250 active devices and is used for the frequency domain or transient analysis of analog cells such as opamps, or sensitive digital cells such as dynamic RAM.

Event-driven simulators handle larger circuits, with thousands of devices, and are typically used to simulate logic. The Janus mixed-signal simulator "SPECTRUM" combines an event-driven simulator with Newton-Raphson methods. SPECTRUM dynamically partitions the circuit to apply the faster event-driven techniques where possible, and the matrix methods where necessary. It also dynamically sizes the matrix and time steps to speed simulation further. The simulator can operate at the transistor level or use behavioral models, or both at the same time, allowing trade-offs between accuracy and speed.

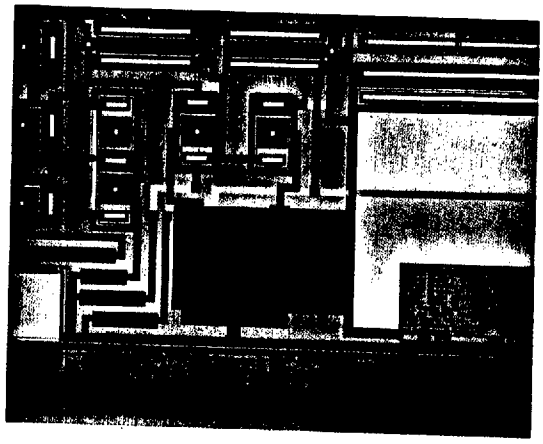
The schematic editor speeds design entry through an efficient user interface which includes menu-controlled device generators.



The mixed-signal simulator combines event-driven techniques for fast logic simulation and matrix methods for accurate analog simulation.



The layout editor optimizes the location of devices and cells based on thermal and noise performance as well as die area and net length.



For layout, the challenge is to increase automation while accommodating the layout sensitivity of analog circuitry. Device generators exist for the full range of active and passive devices available in the technology to create a physical representation of the circuit schematic automatically. This layout may be optimized through conventional interactive polygon-pushing.

The Janus routing editor is driven by the connectivity of the schematics, but allows great freedom to control the routing of critical analog signal paths and power and ground lines manually, while autorouting non-critical nets and spacing the layout to achieve automatic enforcement of layout rules. The Janus routing editor uses up to three interconnect levels, and will automatically expand and compact placement as necessary to achieve 100% routing.

Finally, industry-standard layout verification tools assure conformance of the layout to both the schematic and design rules to give high confidence of functionality in first silicon. The CAD tool suite communicates via industry-standard stream formats to external databases and pattern generators.

Packages

Analog Devices assembles chips into a wide variety of packages, including surface-mount and through-hole, plastic and ceramic. Our engineers will advise you on the best package for your needs, considering pinout, die size, circuit performance, power dissipation, and the operating environment.

The following table shows the standard packages that have 20 or more pins. Packages with lower pin counts are also available. Other types not shown may be procured from outside assembly services.

Type	Material	20	24	28	40	44	48	52	64	68	84	100	108	144
Pin-Grid Array	Ceramic									•	•	•	•	•
Frit-seal Dual In-Line	Ceramic	•	•	•	•									
Side-braze DIP	Ceramic	•	•	•	•		•		•					
Leadless Chip Carrier	Ceramic	•		•		•		•		•				
J-Leaded Chip Carrier	Ceramic					•								
Dual in-line (DIP)	Plastic	•	•	•	•		•		•					
Quad Flat Pack	Plastic											•		
J-Leaded Chip Carrier	Plastic	•		•		•		•		•				
Small Outline (SOIC)	Plastic	•	•	•										

Testing

Testing is as critical as design to assure precision performance. The design and manufacturing process must take full account of the testability of the end product and its functionality in the customer's system. This requires close cooperation between Analog Devices' design and test engineers and those of the customer. From the early stages of the design, these engineers work together to translate system requirements into device specifications and test procedures.

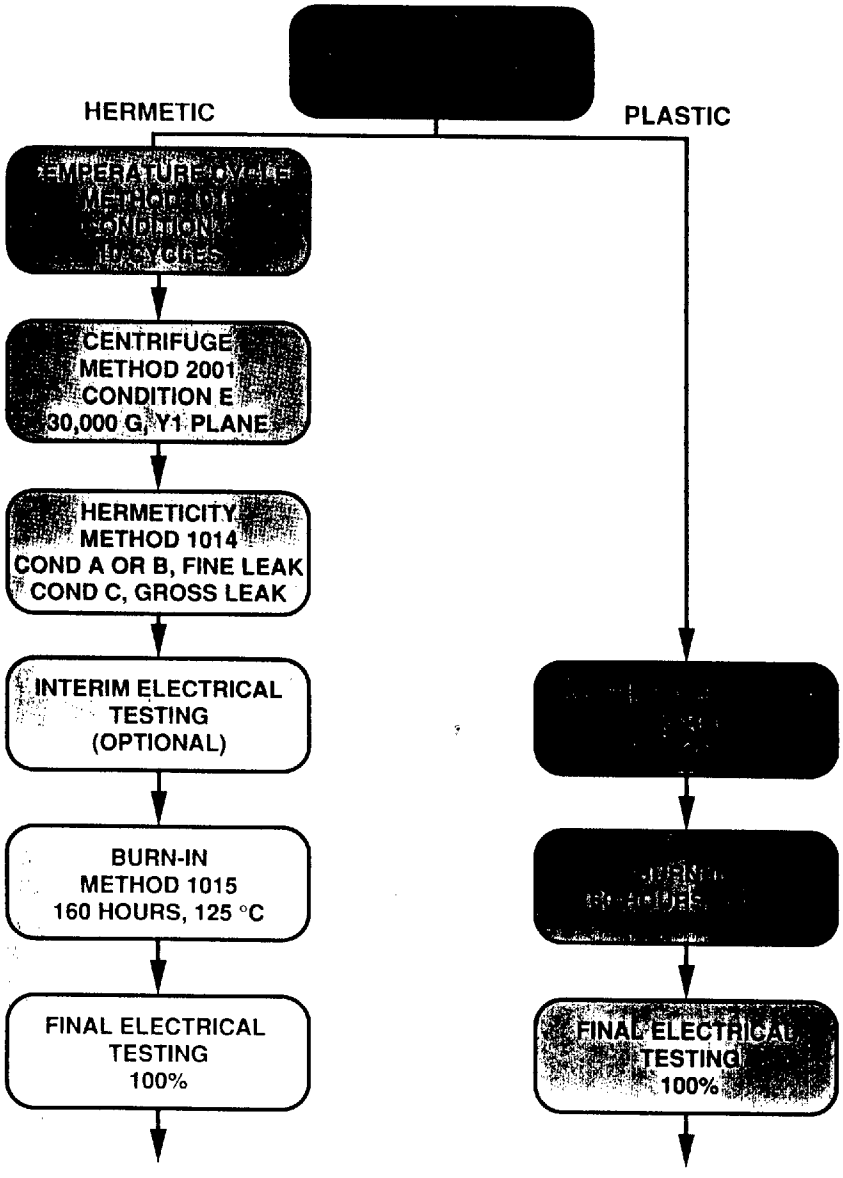
Analog Devices has 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. We pioneered techniques for laser trimming and testing high-accuracy ICs.

ASICs are probed and laser trimmed at the wafer level, and wafers may be laser drift trimmed at elevated temperature to compensate for the effects of temperature on accuracy. Packaged parts can be final-tested at multiple temperatures, from −55 to +125°C.

We use test equipment from the leading manufacturers, including the Teradyne A500 series and Hewlett-Packard 9480, designed specifically for testing mixed-signal LSI parts. All trim and test machines are networked so that device modelers, designers, and process engineers have access to the same data base. This ensures that parts are consistently manufactured at predictably high yields.

Quality & Reliability

PLUS PROCESS FLOWCHART



Analog Devices aims to deliver high quality, cost-effective IC products on time, every time. All departments have a strong quality philosophy and Quality Improvement Programs operate throughout the corporation. The Programs focus on customer service, and QIP teams address such issues as on-time delivery, and reduction of defects and cycle time.

Key elements of the manufacturing flow are under statistical process control. Wafer fab, probe, assembly, and test adhere to strict internal specifications and control procedures. They are also approved, as geographically appropriate, to MIL-M-38510, CECC, and/or UK Defence Standards.

The BiMOS and LC^{2}MOS manufacturing flows are controlled in accordance with MIL-Q-9858. The U.S. and European assembly lines perform MIL-STD-883C, Class B screening.

We also offer PLUS burn-in programs for commercial and industrial applications at lower cost (see inset), and can accommodate special customer needs.

In addition to the normal lot quality acceptances for each product, we regularly monitor and maintain general process reliability through accelerated life testing on each package type and product family. Test results are published in periodic reports.

We manufacture products for the industry's most demanding and quality-conscious customers and have supplied parts to NASA and European Space Agency programs.

Program Flow

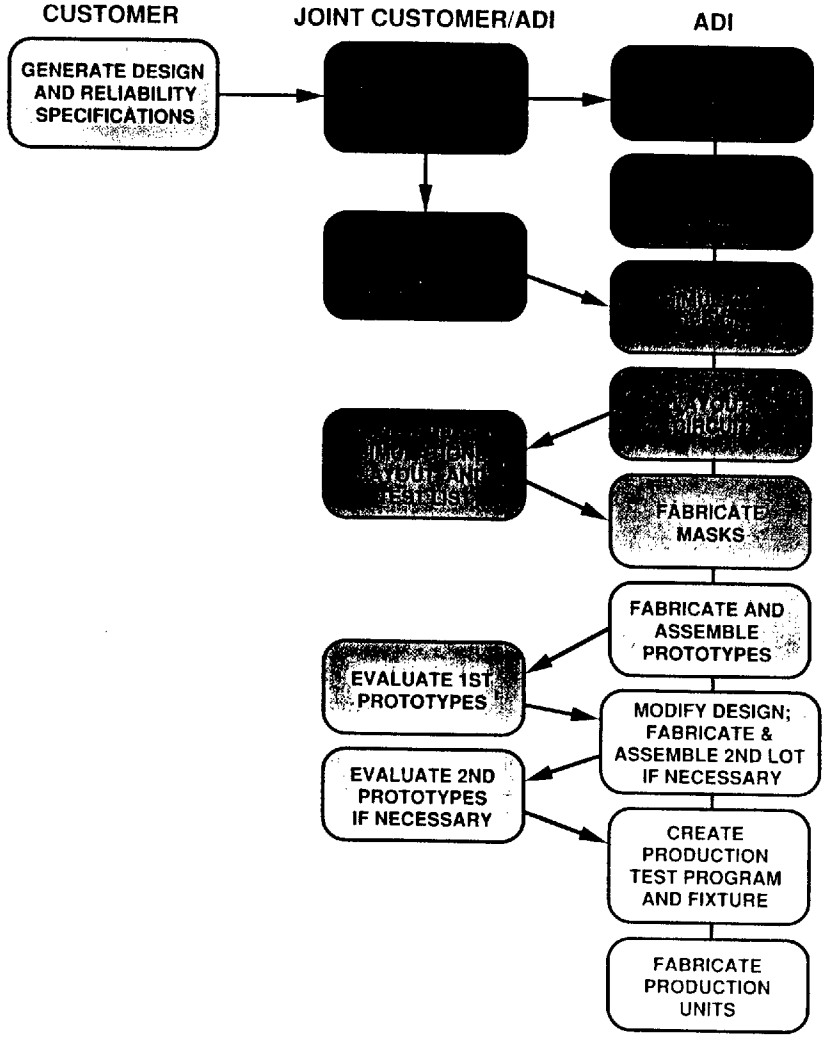
Currently, Analog Devices assumes complete design and manufacturing responsibility for the ASICs we produce. However, we encourage customer participation in the design process through milestone design reviews. At these reviews, we discuss the schematic, simulation results, layout, and test procedures and results.

We work with the customer to generate the specifications for the circuit, including functional, environmental, test, and reliability requirements. From these specifications, we create a detailed circuit design, and new cells, if any are needed. After simulating the design to see that it meets the functional and performance specifications, we review the design with the customer. On approval, we lay out the circuit and create the test program. After the final design review, we have masks made for fabricating the IC, either in our in-house mask shop or by outside vendors. Next we fabricate, assemble, and evaluate the prototypes. On acceptance of the prototypes, we proceed to full-scale production.

The development schedule and expense depend on the overall complexity of the circuit design, the test specifications, and the amount of customization needed. Cell-based and LSM-based designs minimize the required design and test engineering.

Analog Devices can provide a first-pass feasibility study and budgetary proposal for a custom circuit once the customer supplies the following information:

- Functional block diagram
- Functional description
- Prototype schematic, if available
- List of key parametric specs
- Description of system application
- Package requirements
- Environmental requirements
- Screening requirements
- Special test requirements
- Production schedule



For additional information, contact your local Analog Devices Sales Engineer or Representative (see list inside back cover).

This information applies to products under development. Their characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.