



T-46-35

Cascadeable 8K x 9 FIFO  
 Cascadeable 16K x 9 FIFO  
 Cascadeable 32K x 9 FIFO

Features

- 8K x 9, 16K x 9, 32K x 9 FIFO buffer memory
- Asynchronous read/write
- High-speed 33.3-MHz read/write independent of depth/width
- Low operating power
  - $I_{CC}$  (max.) = 160 mA (commercial)
  - $I_{CC}$  (max.) = 165 mA (military)
- Half Full flag in standalone
- Empty and Full flags
- Retransmit in standalone
- Expandable in width and depth
- 5V ± 10% supply
- PLCC, LCC, and 600-mil DIP packaging
- TTL compatible
- Three-state outputs
- Pin compatible to IDT7205 and IDT7206

Functional Description

The CY7C460, CY7C462, and CY7C464 are respectively, 8K, 16K, and 32K words by 9-bit wide first-in-first-out (FIFO) memories. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent overrun and underrun. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the write (W) signal is LOW. Read occurs when read (R) goes LOW. The nine

data outputs go to the high-impedance state when  $\bar{R}$  is HIGH.

A Half Full (HF) output flag is provided that is valid in the standalone (single device) and width expansion configurations. In the depth expansion configuration, this pin provides the expansion out (XO) information that is used to tell the next FIFO that it will be activated.

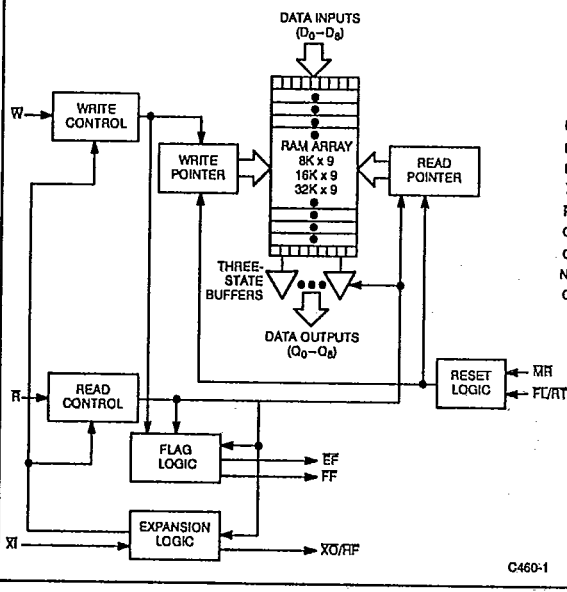
In the standalone and width expansion configurations, a LOW on the retransmit (RT) input causes the FIFOs to retransmit the data. Read enable (R) and write enable (W) must both be HIGH during a retransmit cycle, and then  $\bar{R}$  is used to access the data.

The CY7C460, CY7C462, and CY7C464 are fabricated using an advanced 0.8-micron N-well CMOS technology. Input ESD protection is greater than 2000V and latch-up is prevented by careful layout, guard rings, and a substrate bias generator.

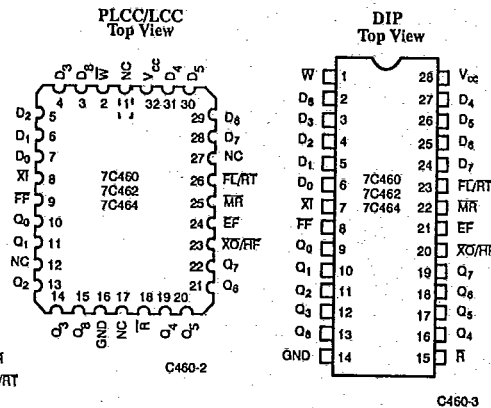


FIFOS

Logic Block Diagram



Pin Configurations





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## Selection Guide

	7C460-15 7C462-15 7C464-15	7C460-20 7C462-20 7C464-20	7C460-25 7C462-25 7C464-25	7C460-40 7C462-40 7C464-40
Frequency (MHz)	33.3	28.5	28.5	20
Maximum Access Time (ns)	15	20	25	40
Maximum Operating Current (mA)	Commercial	160	145	125
	Military		165	145

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with

Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -3.0V to +7.0V

Power Dissipation ..... 1.0W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >200V  
(per MIL-STD-883, Method 3015)

Latch-Up Current ..... &gt;200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Military <sup>[1]</sup>	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range<sup>[2]</sup>

Parameter	Description	Test Conditions	7C460-15 7C462-15 7C464-15		7C460-20 7C462-20 7C464-20		7C460-25 7C462-25 7C464-25		7C460-40 7C462-40 7C464-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -2.0 mA	2.4		2.4		2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage	Com'l Mil/Ind	2.0		2.2		2.2		2.2		V
V <sub>IL</sub>	Input LOW Voltage			0.8		0.8		0.8		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	-10	+10	μA
I <sub>OZ</sub>	Output Leakage Current	R̄ ≥ V <sub>IH</sub> , GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub>	-10	+10	-10	+10	-10	+10	-10	+10	μA
I <sub>CC</sub>	Operating Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA	Com'l <sup>[3]</sup>	160				145		125	mA
			Mil/Ind <sup>[4]</sup>			165		165		145	
I <sub>SB1</sub>	Standby Current	All Inputs = V <sub>IH</sub> Min.	Com'l	25				25		25	mA
			Mil/Ind			30		30		30	
I <sub>SB2</sub>	Power-Down Current	All Inputs V <sub>CC</sub> - 0.2V	Com'l	20				20		20	mA
			Mil/Ind			25		25		25	
I <sub>OS</sub>	Output Short Circuit Current <sup>[5]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-90		-90		-90		-90	mA

## Notes:

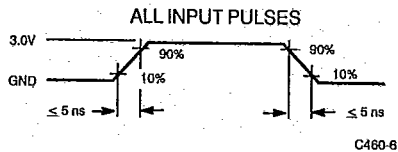
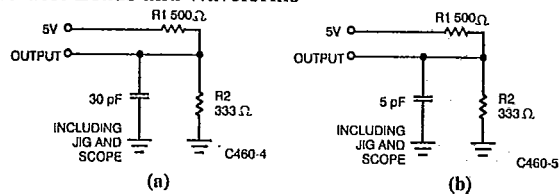
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- I<sub>CC</sub>(commercial) = 125 mA + [(f̄ - 20) \* 2.5 mA/MHz]  
for f̄ ≥ 20 MHz  
where f̄ = the larger of the write or read operating frequency.
- I<sub>CC</sub>(military) = 145 mA + [(f̄ - 20) \* 2.5 mA/MHz]  
for f̄ ≥ 20 MHz  
where f̄ = the larger of the write or read operating frequency.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

Capacitance<sup>[6]</sup>

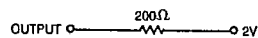
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Parameters	Description	Test Conditions	Max.	Units
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ ,	5	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 5.0\text{V}$	7	pF

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range<sup>[2,7]</sup>

Parameters	Description	7C460-15 7C462-15 7C464-15		7C460-20 7C462-20 7C464-20		7C460-25 7C462-25 7C464-25		7C460-40 7C462-40 7C464-40		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	30		30		35		50		ns
$t_A$	Access Time		15		20		25		40	ns
$t_{RR}$	Read Recovery Time	15		15		10		10		ns
$t_{PR}$	Read Pulse Width	15		20		25		40		ns
$t_{LZR}$	Read LOW to Low Z	3		3		3		3		ns
$t_{DVR}^{[8]}$	Read HIGH to Data Valid	3		3		3		3		ns
$t_{HZR}^{[8]}$	Read HIGH to High Z		15		15		18		25	ns
$t_{WC}$	Write Cycle Time	30		30		35		50		ns
$t_{PW}$	Write Pulse Width	15		20		25		40		ns
$t_{HWZ}$	Write HIGH to Low Z	5		5		5		5		ns
$t_{WR}$	Write Recovery Time	15		15		10		10		ns
$t_{SD}$	Data Set-Up Time	11		12		15		20		ns
$t_{HD}$	Data Hold Time	0		0		0		0		ns
$t_{MRSC}$	$\overline{MR}$ Cycle Time	30		30		35		50		ns
$t_{PMR}$	$\overline{MR}$ Pulse Width	15		20		25		40		ns
$t_{RMR}$	$\overline{MR}$ Recovery Time	15		15		10		10		ns
$t_{RPW}$	Read HIGH to $\overline{MR}$ HIGH	15		20		25		40		ns
$t_{WPW}$	Write HIGH to $\overline{MR}$ HIGH	15		20		25		40		ns
$t_{RTC}$	Retransmit Cycle Time	30		35		35		50		ns
$t_{PRT}$	Retransmit Pulse Width	15		20		25		40		ns
$t_{RTR}$	Retransmit Recovery Time	15		15		10		10		ns
$t_{EFL}$	$\overline{MR}$ to $\overline{EF}$ LOW		30		35		35		50	ns
$t_{HFH}$	$\overline{MR}$ to $\overline{HF}$ HIGH		30		35		35		50	ns
$t_{FFH}$	$\overline{MR}$ to $\overline{FF}$ HIGH		30		35		35		50	ns



FIFOS



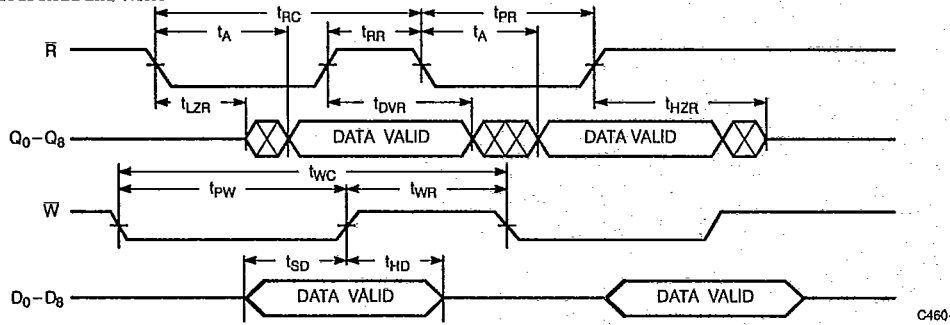
Switching Characteristics Over the Operating Range<sup>[2,7]</sup> (continued)

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Parameters	Description	7C460-15		7C460-20		7C460-25		7C460-40		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>REF</sub>	Read LOW to $\overline{EF}$ LOW		15		20		25		40	ns
t <sub>RFF</sub>	Read HIGH to $\overline{FF}$ HIGH		15		20		25		40	ns
t <sub>WEF</sub>	Write HIGH to $\overline{EF}$ HIGH		15		20		25		40	ns
t <sub>WFF</sub>	Write LOW to $\overline{FF}$ LOW		15		20		25		40	ns
t <sub>WHF</sub>	Write LOW to $\overline{HF}$ LOW		30		35		35		50	ns
t <sub>RHF</sub>	Read HIGH to $\overline{HF}$ HIGH		30		35		35		50	ns
t <sub>RAE</sub>	Effective Read from Write HIGH		15		20		25		40	ns
t <sub>RPE</sub>	Effective Read Pulse Width After $\overline{EF}$ HIGH	15		20		25		40		ns
t <sub>WAF</sub>	Effective Write from Read HIGH		15		20		25		40	ns
t <sub>WPF</sub>	Effective Write Pulse Width After $\overline{FF}$ HIGH	15		20		25		40		ns
t <sub>XOL</sub>	Expansion Out LOW Delay from Clock		15		20		25		40	ns
t <sub>XOH</sub>	Expansion Out HIGH Delay from Clock		30		35		35		50	ns

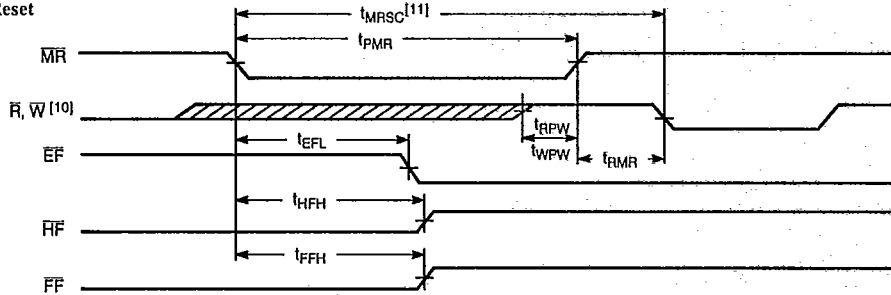
Switching Waveforms<sup>[9]</sup>

Asynchronous Read and Write



C460-7

Master Reset



C460-8

Notes:

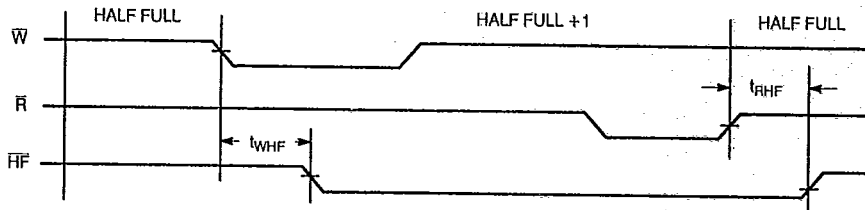
- Test conditions assume signal transmission time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance, as in part (a) of AC Test Load, unless otherwise specified.
- t<sub>HZR</sub> and t<sub>DVR</sub> use capacitance loading as in part (b) of AC Test Load.
- A HIGH-to-LOW transition of either the write or read strobe causes a HIGH-to-LOW transition of the responding flag. Correspondingly, a low-to-high strobe transition causes a LOW-to-HIGH flag transition.
- W and R = V<sub>IH</sub> around the rising edge of MR.
- t<sub>MRSC</sub> = t<sub>PMR</sub> + t<sub>RMR</sub>.



Switching Waveforms

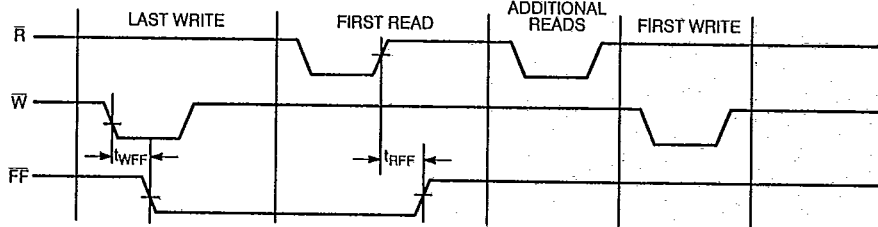
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Half Full Flag



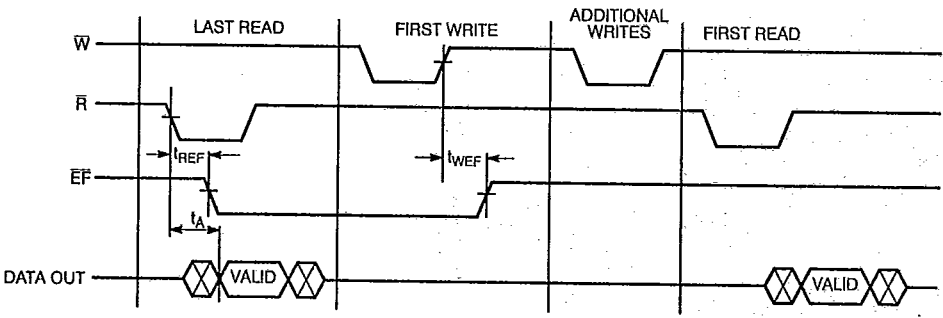
C460-9

Last Write to First Read Full Flag



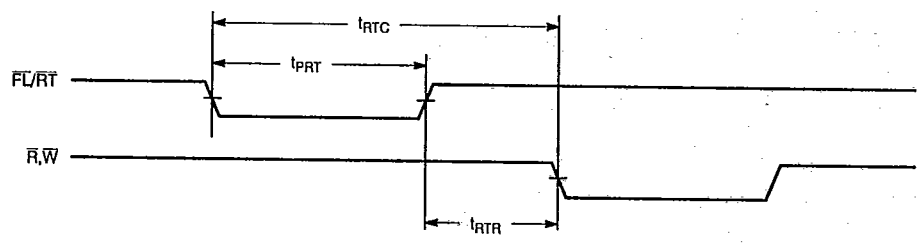
C460-10

Last READ to First WRITE Empty Flag



C460-11

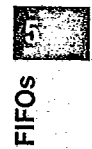
Retransmit<sup>[12,13]</sup>



C460-12

Notes:  
12.  $t_{RTC} = t_{PRT} + t_{RTR}$ .

13.  $\overline{EF}$ ,  $\overline{HF}$  and  $\overline{FF}$  may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at  $t_{RTC}$ .

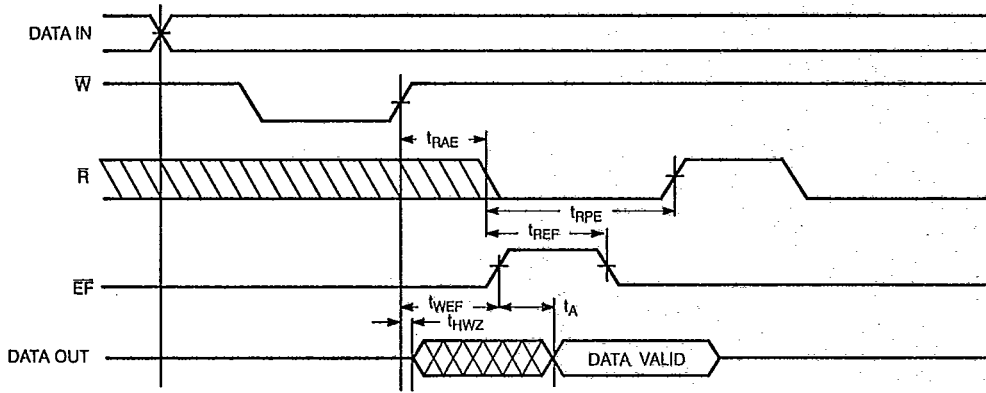




Switching Waveforms (continued)

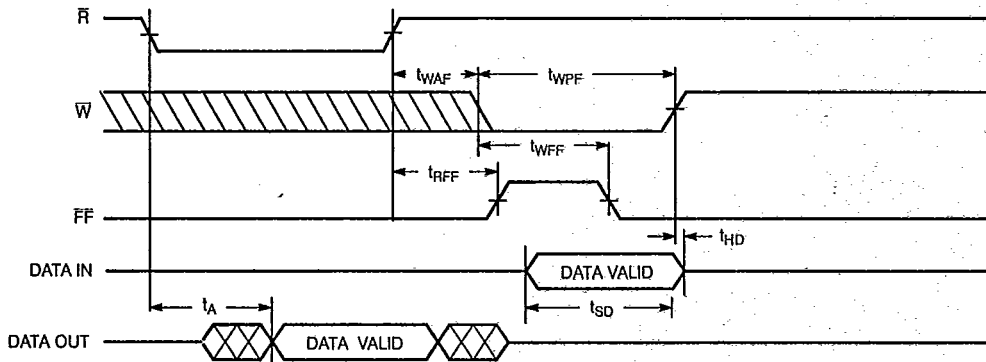
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Empty Flag and Read Bubble-Through Mode



C460-13

Full Flag and Write Bubble-Through Mode



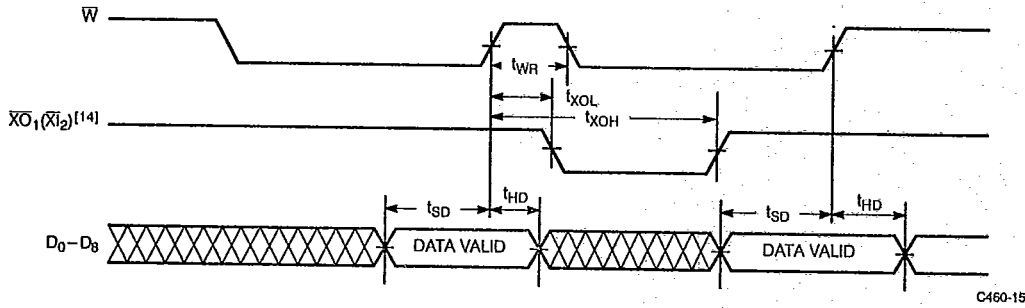
C460-14



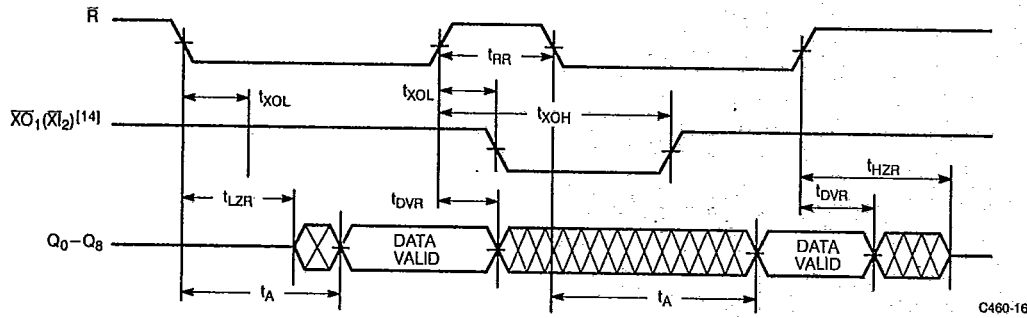
Switching Waveforms (continued)

Expansion Timing Diagrams

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FIFOS



Notes:  
14. Expansion out of device 1 ( $\overline{XO}_1$ ) is connected to expansion in of device 2 ( $\overline{XI}_2$ ).



## Architecture

### Resetting the FIFO

Upon power up, the FIFO must be reset with a master reset ( $\overline{MR}$ ) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ( $\overline{EF}$ ) being LOW, and both the Half Full ( $\overline{HF}$ ), and Full flags ( $\overline{FF}$ ) being HIGH. Read ( $\overline{R}$ ) and write ( $\overline{W}$ ) must be HIGH  $t_{RPW}/t_{WPW}$  before and  $t_{RMR}$  after the rising edge of  $\overline{MR}$  for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs will all be in the high-impedance state.

### Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH  $\overline{EF}$ . The falling edge of  $\overline{W}$  initiates a write cycle. Data appearing at the inputs ( $D_0 - D_8$ )  $t_{SD}$  before and  $t_{ID}$  after the rising edge of  $\overline{W}$  will be stored sequentially in the FIFO.

The  $\overline{EF}$  LOW-to-HIGH transition occurs  $t_{WFF}$  after the first LOW-to-HIGH transition of  $\overline{W}$  for an empty FIFO.  $\overline{HF}$  goes LOW  $t_{WHF}$  after the falling edge of  $\overline{W}$  following the FIFO actually being half full. Therefore, the  $\overline{HF}$  is active once the FIFO is filled to half its capacity plus one word.  $\overline{HF}$  will remain LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of  $\overline{HF}$  occurs  $t_{RHF}$  after the rising edge of  $\overline{R}$  when the FIFO goes from half full + 1 to half full.  $\overline{HF}$  is available in standalone and width expansion modes.  $\overline{FF}$  goes LOW  $t_{WFF}$  after the falling edge of  $\overline{W}$ , during the cycle in which the last available location is filled. Internal logic prevents overrunning a full FIFO. Writes to a full FIFO are ignored and the write pointer is not incremented.  $\overline{FF}$  goes HIGH  $t_{RFF}$  after a read from a full FIFO.

### Reading Data from the FIFO

The falling edge of  $\overline{R}$  initiates a read cycle if the  $\overline{EF}$  is not LOW. Data outputs ( $Q_0 - Q_8$ ) are in a high-impedance condition between read operations ( $\overline{R}$  HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of  $\overline{R}$  initiates a HIGH-to-LOW transition of  $\overline{EF}$ . When the FIFO is empty, the outputs are in a high-impedance state. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read  $t_{WER}$  after a valid write.

### Retransmit

The retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be acknowledged by the receiver and retransmitted if necessary. The retransmit ( $\overline{RT}$ ) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal-to-or-less-than the depth of the FIFO have occurred since the last  $\overline{MR}$  cycle. A LOW pulse on  $\overline{RT}$  resets the internal read pointer to the first physical location of the FIFO.  $\overline{R}$  and  $\overline{W}$  must both be HIGH while and  $t_{RTR}$  after retransmit is LOW. With every read cycle after retransmit, previously accessed data is read and the read pointer incremented until equal to the write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of  $\overline{RT}$  are transmitted also.

The full depth of the FIFO can be repeatedly retransmitted.

### Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding expansion in ( $\overline{XI}$ ) and tying first load ( $\overline{FL}$ ) to  $V_{CC}$  prior to a  $\overline{MR}$  cycle. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

### Depth Expansion Mode (see Figure 1)

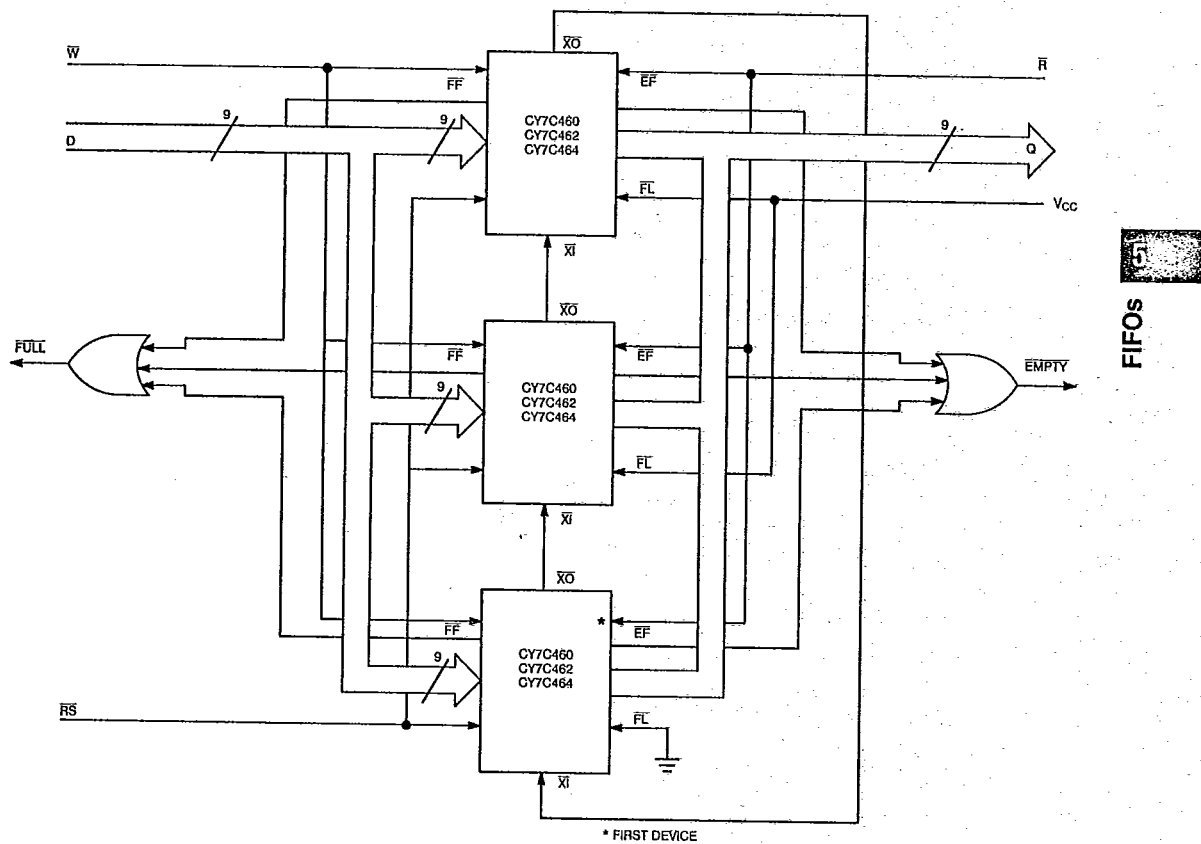
Depth expansion mode is entered when, during a  $\overline{MR}$  cycle, expansion out ( $\overline{XO}$ ) of one device is connected to expansion in ( $\overline{XI}$ ) of the next device, with  $\overline{XO}$  of the last device connected to  $\overline{XI}$  of the first device. In the depth expansion mode, the first load ( $\overline{FL}$ ) input, when grounded, indicates that this is the first part to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO,  $\overline{XO}$  is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created with word widths in increments of nine. When expanding in depth, a composite  $\overline{FF}$  is created by ORing the  $\overline{FF}$ s together. Likewise, a composite  $\overline{EF}$  is created by ORing  $\overline{EF}$ s together.  $\overline{HF}$  and  $\overline{RT}$  functions are not available in depth expansion mode.





T-46-35



\* FIRST DEVICE

C460-17

Figure 1. Depth Expansion

CYPRESS SEMICONDUCTOR  
PRELIMINARY

CY7C460  
CY7C462  
CY7C464



T-46-35

## Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range	
15	CY7C460-15DC	D16	Commercial	
	CY7C460-15JC	J65		
	CY7C460-15LC	L55		
	CY7C460-15PC	P15		
	CY7C460-15JI	J65	Industrial	
	CY7C460-15PI	P15		
20	CY7C460-20DMB	D16	Military	
	CY7C460-20LMB	L55		
25	CY7C460-25DC	D16	Commercial	
	CY7C460-25JC	J65		
	CY7C460-25LC	L55		
	CY7C460-25PC	P15		
	CY7C460-25JI	J65	Industrial	
	CY7C460-25PI	P15		
	CY7C460-25DMB	D16	Military	
	CY7C460-25LMB	L55		
	40	CY7C460-40DC	D16	Commercial
CY7C460-40JC		J65		
CY7C460-40LC		L55		
CY7C460-40PC		P15		
CY7C460-40JI		J65	Industrial	
CY7C460-40PI		P15		
CY7C460-40DMB		D16	Military	
CY7C460-40LMB		L55		
15		CY7C462-15DC	D16	Commercial
		CY7C462-15JC	J65	
	CY7C462-15LC	L55		
	CY7C462-15PC	P15		
	CY7C462-15JI	J65	Industrial	
	CY7C462-15PI	P15		
	20	CY7C462-20DMB	D16	Military
		CY7C462-20LMB	L55	
	25	CY7C462-25DC	D16	Commercial
		CY7C462-25JC	J65	
CY7C462-25LC		L55		
CY7C462-25PC		P15		
CY7C462-25JI		J65	Industrial	
CY7C462-25PI		P15		
CY7C462-25DMB		D16	Military	
CY7C462-25LMB		L55		
40		CY7C462-40DC	D16	Commercial
	CY7C462-40JC	J65		
	CY7C462-40LC	L55		
	CY7C462-40PC	P15		
	CY7C462-40JI	J65	Industrial	
	CY7C462-40PI	P15		
	CY7C462-40DMB	D16	Military	
	CY7C462-40LMB	L55		

CYPRESS SEMICONDUCTOR  
PRELIMINARYCY7C460  
CY7C462  
CY7C464

## Ordering Information (continued)

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Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C464-15DC	D16	Commercial
	CY7C464-15JC	J65	
	CY7C464-15LC	L55	
	CY7C464-15PC	P15	
	CY7C464-15JI	J65	Industrial
	CY7C464-15PI	P15	
20	CY7C464-20DMB	D16	Military
	CY7C464-20LMB	L55	
25	CY7C464-25DC	D16	Commercial
	CY7C464-25JC	J65	
	CY7C464-25LC	L55	
	CY7C464-25PC	P15	
	CY7C464-25JI	J65	Industrial
	CY7C464-25PI	P15	
	CY7C464-25DMB	D16	Military
	CY7C464-25LMB	L55	
40	CY7C464-40DC	D16	Commercial
	CY7C464-40JC	J65	
	CY7C464-40LC	L55	
	CY7C464-40PC	P15	
	CY7C464-40JI	J65	Industrial
	CY7C464-40PI	P15	
	CY7C464-40DMB	D16	Military
	CY7C464-40LMB	L55	



FIFOS


**MILITARY SPECIFICATIONS**  
**Group A Subgroup Testing**  
**DC Characteristics**

T-46-35

Parameters	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL Max.</sub>	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB1</sub>	1, 2, 3
I <sub>SB2</sub>	1, 2, 3
I <sub>OS</sub>	1, 2, 3

**Switching Characteristics**

Parameters	Subgroups
t <sub>RC</sub>	9, 10, 11
t <sub>A</sub>	9, 10, 11
t <sub>RR</sub>	9, 10, 11
t <sub>PR</sub>	9, 10, 11
t <sub>LZR</sub>	9, 10, 11
t <sub>DVR</sub>	9, 10, 11
t <sub>HZR</sub>	9, 10, 11
t <sub>WC</sub>	9, 10, 11
t <sub>PW</sub>	9, 10, 11
t <sub>HWZ</sub>	9, 10, 11
t <sub>WR</sub>	9, 10, 11
t <sub>SD</sub>	9, 10, 11
t <sub>HD</sub>	9, 10, 11
t <sub>MRSC</sub>	9, 10, 11
t <sub>PMR</sub>	9, 10, 11
t <sub>RMR</sub>	9, 10, 11
t <sub>RPW</sub>	9, 10, 11
t <sub>WPW</sub>	9, 10, 11
t <sub>RTC</sub>	9, 10, 11
t <sub>PRT</sub>	9, 10, 11
t <sub>RTR</sub>	9, 10, 11
t <sub>EFL</sub>	9, 10, 11
t <sub>HFH</sub>	9, 10, 11
t <sub>FFH</sub>	9, 10, 11
t <sub>REF</sub>	9, 10, 11
t <sub>RFF</sub>	9, 10, 11
t <sub>WEF</sub>	9, 10, 11
t <sub>WFF</sub>	9, 10, 11
t <sub>WHE</sub>	9, 10, 11
t <sub>RHE</sub>	9, 10, 11
t <sub>RAE</sub>	9, 10, 11
t <sub>RPE</sub>	9, 10, 11
t <sub>WAF</sub>	9, 10, 11
t <sub>WPF</sub>	9, 10, 11
t <sub>XOL</sub>	9, 10, 11
t <sub>XOH</sub>	9, 10, 11

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