

4-bit Single Chip Microcomputer



- Core CPU Architecture
- R-f Converter
- Serial Interface

■ DESCRIPTION

The E0C6256 is a CMOS 4-bit single-chip microcomputer, built-in core CPU E0C6200A, ROM, RAM, A/D converter (R-f conversion type), SVD circuit, LCD driver, serial interface, watchdog timer, programmable timer, time base counter, and others.

It can realize system to measure temperature and/or humidity by the built-in A/D converter and externally attached parts.

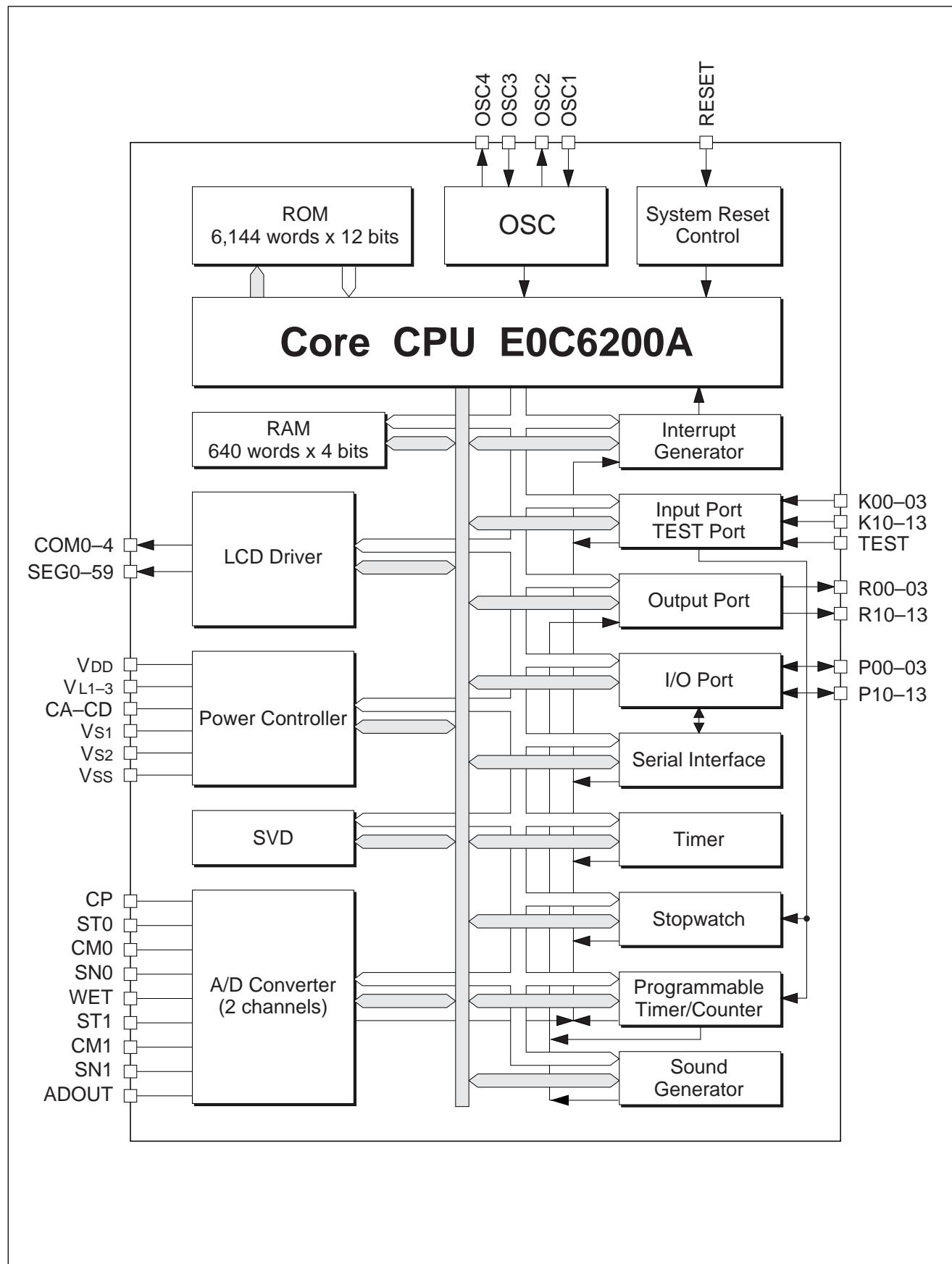
Because of its low-voltage operation and low power consumption, this series is ideal for a wide range of applications, and is especially suitable for battery-driven systems.

■ FEATURES

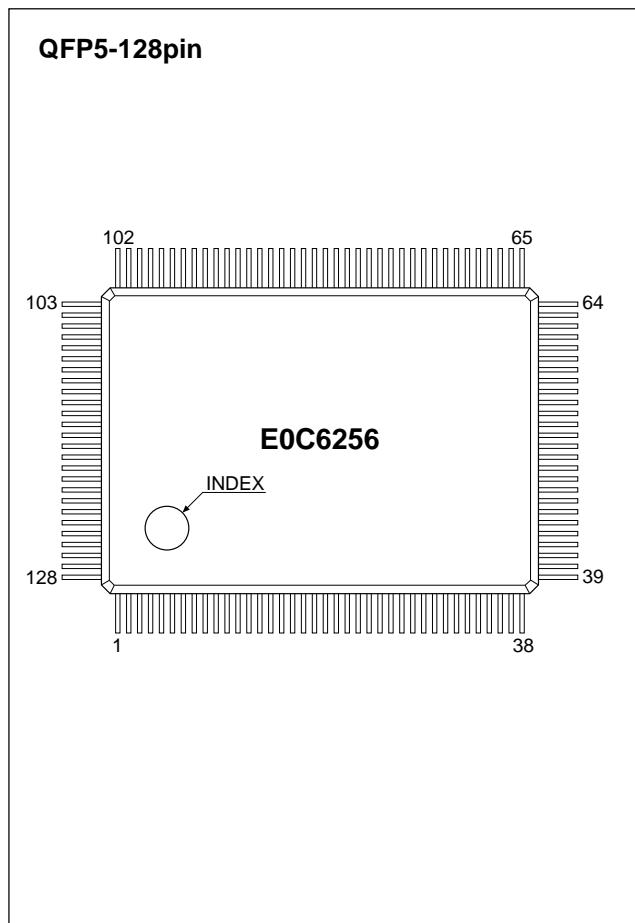
- CMOS LSI 4-bit parallel processing
- Twin clock Crystal oscillation circuit (with built-in drain capacitance) : 32.768kHz (Typ.)
CR or Ceramic oscillation circuit (mask option) : 1MHz (Typ.)
- Instruction set 108 instructions
- Instruction cycle time 32.768kHz clock : 153μsec, 214μsec, 366μsec
1MHz clock : 5μsec, 7μsec, 12μsec
- ROM 6,144 × 12 bits
- RAM 640 × 4 bits
- Input port 8 bits (pull-down resistors are available by mask option)
- Output port 8 bits (BZ, FOUT and PTOVF outputs can be selected by software)
- I/O port 8 bits (4 bits can be switched to serial I/O by software)
- Serial interface 1 port (8-bit clock synchronous type)
- A-D converter R-f (resistance/frequency) conversion type, 2 channels
- LCD driver 60 segments × 5, 4, 3 or 2 commons (selected by software)
LCD drive voltage: 1.05V to 1.40V, programmable (step by 0.05V)
- Time base counter Clock timer 1 channel
1/1000sec stopwatch timer 1 channel
- Programmable timer 8-bit : 1 channel, with event counter function
- Watchdog timer
- Supply voltage detection (SVD) circuit .. 1.05/1.20/1.35V, programmable
(when 1.5V system is selected by mask option)
2.30/2.45/2.60V, programmable
(when 3.0V system is selected by mask option)
- Interrupt External : Input port 2 interrupts
Internal : Clock timer 3 interrupts
Serial interface 1 interrupt
A/D converter 1 interrupt
- Supply voltage 0.9V to 3.6V
(2.2–3.6V when OSC3 is used, 1.35–3.6V when A/D converter is used)
- Current consumption HALT mode (32.768kHz/1.5V, normal) : 1.2μA (Typ.)
HALT mode (32.768kHz/3.0V, halver) : 650nA (Typ.)
OPERATING mode (32.768kHz/1.5V, normal) : 3.5μA (Typ.)
OPERATING mode (32.768kHz/3.0V, halver) : 2.0μA (Typ.)
OPERATING mode (1MHz/3.0V, ceramic) : 170μA (Typ.)
OPERATING mode (1MHz/3.0V, CR) : 220μA (Typ.)
- Package QFP5-128pin (plastic), QFP5-100pin (plastic)
Die form

E0C6256

■ BLOCK DIAGRAM

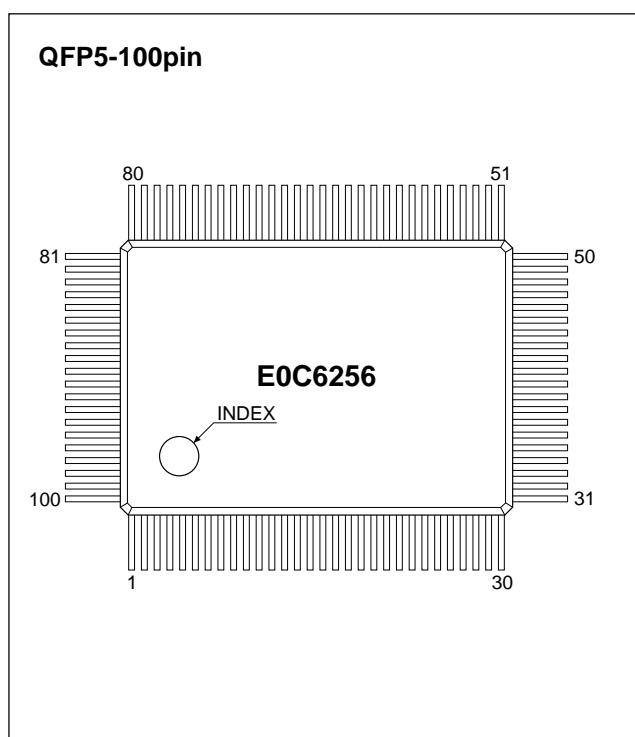


■ PIN CONFIGURATION



Pin No.	Pin name						
1	N.C.	33	OSC4	65	SEG58	97	Vss
2	SEG27	34	Vs1	66	SEG59	98	N.C.
3	SEG28	35	SEG30	67	N.C.	99	N.C.
4	SEG29	36	SEG31	68	N.C.	100	N.C.
5	COM0	37	SEG32	69	N.C.	101	SEG0
6	COM1	38	N.C.	70	VDD	102	SEG1
7	COM2	39	N.C.	71	RESET	103	SEG2
8	COM3	40	SEG33	72	TEST	104	SEG3
9	COM4	41	SEG34	73	K00	105	SEG4
10	CB	42	SEG35	74	K01	106	SEG5
11	CA	43	SEG36	75	K02	107	SEG6
12	VL3	44	SEG37	76	K03	108	SEG7
13	VL2	45	SEG38	77	K10	109	SEG8
14	VL1	46	SEG39	78	K11	110	SEG9
15	CC	47	SEG40	79	K12	111	SEG10
16	CD	48	SEG41	80	K13	112	SEG11
17	Vs2	49	SEG42	81	R00	113	SEG12
18	Vss	50	SEG43	82	R01	114	SEG13
19	ADOUT	51	SEG44	83	R02	115	SEG14
20	SN1	52	SEG45	84	R03	116	SEG15
21	WET	53	SEG46	85	R10	117	SEG16
22	ST1	54	SEG47	86	R11	118	SEG17
23	CM1	55	SEG48	87	R12	119	SEG18
24	SN0	56	SEG49	88	R13	120	SEG19
25	CM0	57	SEG50	89	P00	121	SEG20
26	ST0	58	SEG51	90	P01	122	SEG21
27	CP	59	SEG52	91	P02	123	SEG22
28	VDD	60	SEG53	92	P03	124	SEG23
29	N.C.	61	SEG54	93	P10	125	SEG24
30	OSC1	62	SEG55	94	P11	126	SEG25
31	OSC2	63	SEG56	95	P12	127	SEG26
32	OSC3	64	SEG57	96	P13	128	N.C.

N.C. : No Connection



Pin No.	Pin name						
1	SEG29	26	OSC2	51	SEG59	76	P11
2	COM0	27	OSC3	52	VDD	77	P12
3	COM1	28	OSC4	53	RESET	78	P13
4	COM2	29	Vs1	54	TEST	79	Vss
5	COM3	30	SEG30	55	K00	80	SEG0
6	COM4	31	SEG31	56	K01	81	SEG1
7	CB	32	SEG32	57	K02	82	SEG2
8	CA	33	SEG34	58	K03	83	SEG4
9	VL3	34	SEG36	59	K10	84	SEG6
10	VL2	35	SEG38	60	K11	85	SEG8
11	VL1	36	SEG40	61	K12	86	SEG10
12	CC	37	SEG41	62	K13	87	SEG12
13	CD	38	SEG42	63	R00	88	SEG13
14	Vs2	39	SEG43	64	R01	89	SEG14
15	ADOUT	40	SEG44	65	R02	90	SEG15
16	SN1	41	SEG45	66	R03	91	SEG16
17	WET	42	SEG46	67	R10	92	SEG17
18	ST1	43	SEG47	68	R11	93	SEG18
19	CM1	44	SEG48	69	R12	94	SEG19
20	SN0	45	SEG49	70	R13	95	SEG21
21	CM0	46	SEG51	71	P00	96	SEG23
22	ST0	47	SEG53	72	P01	97	SEG25
23	CP	48	SEG55	73	P02	98	SEG26
24	VDD	49	SEG57	74	P03	99	SEG27
25	OSC1	50	SEG58	75	P10	100	SEG28

E0C6256

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-128pin	QFP5-100pin		
VDD	28, 70	24, 52	-	Power supply pin (+)
VSS	18, 97	79	-	Power supply pin (-)
Vs1	34	29	O	Regulated voltage output pin for oscillation and internal logic
Vs2	17	14	O	Boosting/reducing power supply output pin
VL1	14	11	O	Output pin for regulated power supply for LCD
VL2	13	10	O	Output pin for LCD booster (VL1 × 2)
VL3	12	9	O	Output pin for LCD booster (VL1 × 3)
CA, CB	11, 10	8, 7	-	Capacitor connection pin for LCD booster
CC, CD	15, 16	12, 13	-	Capacitor connecting pin for boosting/reducing power supply
OSC1	30	25	I	Crystal oscillation input pin
OSC2	31	26	O	Crystal oscillation output pin
OSC3	32	27	I	Ceramic or CR oscillation input pin (selected by mask option)
OSC4	33	28	O	Ceramic or CR oscillation output pin (selected by mask option)
K00-K03	73-76	55-58	I	Input port pin
K10-K13	77-80	59-62	I	Input port pin
P00-P03	89-92	71-74	I/O	I/O port pin
P10-P13	93-96	75-78	I/O	I/O port pin (switching to SIN, SOUT, SCLK, SRDY pin is possible by software)
R00-R03	81-84	63-66	O	Output port pin
R10-R13	85-88	67-70	O	Output port pin (switching to BZ, PTOVF, FOUT output is possible by software)
COM0-COM4	5-9	2-6	O	LCD common output pin (1/5, 1/4, 1/3, 1/2 duty, programmable)
SEG0-SEG59*	101-127, 2-4 35-37, 40-66	80-100 1, 30-51	O	LCD segment output pin (DC output may be selected by mask option)
CP	27	23	O	A/D converter test output pin
ST0	26	22	O	A/D converter CH0 CR oscillation output pin
CM0	25	21	O	A/D converter CH0 CR oscillation output pin
SN0	24	20	I	A/D converter CH0 CR oscillation input pin
WET	21	17	O	A/D converter CH1 CR oscillation output pin
ST1	22	18	O	A/D converter CH1 CR oscillation output pin
CM1	23	19	O	A/D converter CH1 CR oscillation output pin
SN1	20	16	I	A/D converter CH1 CR oscillation input pin
ADOUT	19	15	O	A/D converter oscillation frequency output pin
RESET	71	53	I	Initial reset input pin
TEST	72	54	I	Testing input pin

* The following SEG pins are not included in the QFP5-100pin package, so they cannot be used.

SEG3, SEG5, SEG7, SEG9, SEG11, SEG20, SEG22, SEG24, SEG33, SEG35, SEG37, SEG39, SEG50, SEG52, SEG54, SEG56

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(VDD=0V)

Rating	Symbol	Value	Unit
Supply voltage	Vss	-7.0 to 0.5	V
Input voltage (1)	Vi	Vss - 0.3 to 0.5	V
Input voltage (2)	Viosc	Vs1 - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{vss}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	-
Allowable dissipation *2	Pd	250	mW

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is drawn in).

*2 In case of plastic package (QFP5-100pin, QFP5-128pin).

● Recommended Operating Conditions

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit	
Supply voltage	Vss	VDD=0V	Normal mode (OSC3: OFF)	-3.6	-3.0/-1.5	-1.3	V
			Normal mode (OSC3: ON)	-3.6	-3.0	-2.2	V
			Halver mode	-3.6	-3.0	-2.55	V
			Doubler mode	-1.4	-1.1	-0.9	V
Oscillation frequency (1)	fosc1		-	32.768	-	kHz	
Oscillation frequency (2)	fosc3	Duty 50±5%	300	1,000	1,200	kHz	

● DC Characteristics

(Unless otherwise specified, the values listed below are standard values under the following conditions:
 $V_{DD}=0V$, $V_{SS}=-1.5V/-3.0V$, $f_{osc1}=32.768kHz$, $T_a=25^\circ C$, $V_{S1}/V_{L1}/V_{L2}/V_{L3}$ are internal voltage, $C1-C7=0.1\mu F$)

Characteristic	Symbol	Condition			Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	$K00-03, K10-13, P00-03, P10-13$			$0.2 \cdot V_{SS}$		0	V
High level input voltage (2)	V_{IH2}	RESET, TEST			$0.1 \cdot V_{SS}$		0	V
Low level input voltage (1)	V_{IL1}	$K00-03, K10-13, P00-03, P10-13$			V_{SS}		$0.8 \cdot V_{SS}$	V
Low level input voltage (2)	V_{IL2}	RESET, TEST			V_{SS}		$0.9 \cdot V_{SS}$	V
High level input current (1)	I_{IH1}	$V_{IH1}=0V$, Without pull down resistor K00-03, K10-13, P00-03, P10-13 RESET, TEST			0		0.5	μA
High level input current (2)	I_{IH2}	$V_{IH2}=0V$, With pull down resistor K00-03, K10-13, P00-03 $P10-13$, RESET, TEST	$V_{SS}=-1.5V$	2			10	μA
			$V_{SS}=-3.0V$	4			16	μA
Low level input current	I_{IL}	$V_{IL}=V_{SS}$ K00-03, K10-13, P00-03, P10-13 RESET, TEST			-0.5		0	μA
High level output current	I_{OH1}	$V_{OH1}=0.1 \cdot V_{SS}$	$P00-03, P10-13$	$V_{SS}=-1.5V$			-150	μA
			$R00-03, R10-13$	$V_{SS}=-3.0V$			-0.9	mA
Low level output current	I_{OL1}	$V_{OL1}=0.9 \cdot V_{SS}$	$P00-03, P10-13$	$V_{SS}=-1.5V$	400			μA
			$R00-03, R10-13$	$V_{SS}=-3.0V$	1.8			mA
Common output current	I_{OH2}	$V_{OH2}=-0.05V$	COM0-COM4				-3	μA
	I_{OL2}	$V_{OL2}=V_{L3}+0.05V$		3		μA		
Segment output current (during LCD output)	I_{OH3}	$V_{OH3}=-0.05V$	SEG0-SEG59				-3	μA
	I_{OL3}	$V_{OL3}=V_{L3}+0.05V$		3		μA		
Segment output current (during DC output)	I_{OH4}	$V_{OH4}=0.1 \cdot V_{SS}$	SEG0-SEG59	$V_{SS}=-1.5V$			100	μA
				$V_{SS}=-3.0V$			-200	μA
	I_{OL4}	$V_{OL4}=0.9 \cdot V_{SS}$		$V_{SS}=-1.5V$	100			μA
				$V_{SS}=-3.0V$	200			μA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified, the values listed below are standard values under the following conditions:
 $V_{DD}=0V$, $V_{SS}=-1.5V/-3.0V$, $f_{osc1}=32.768kHz$, $C_g=25pF$, $T_a=25^\circ C$, $V_{S1}/V_{L1}/V_{L2}/V_{L3}$ are internal voltage, $C1-C7=0.1\mu F$)
(During A/D operation: $C=2,200pF$, Reference resistance=10kΩ, Sensor=10kΩ)

Characteristic	Symbol	Condition			Min.	Typ.	Max.	Unit
LCD drive voltage *6	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (no panel load)	$VLCHG2-VLCHG0 = "0"$		-1.15	-1.05	-0.95	V
			$VLCHG2-VLCHG0 = "1"$		-1.20	-1.10	-1.00	V
			$VLCHG2-VLCHG0 = "2"$		-1.25	-1.15	-1.05	V
			$VLCHG2-VLCHG0 = "3"$		-1.30	-1.20	-1.10	V
			$VLCHG2-VLCHG0 = "4"$		-1.35	-1.25	-1.15	V
			$VLCHG2-VLCHG0 = "5"$		-1.40	-1.30	-1.20	V
			$VLCHG2-VLCHG0 = "6"$		-1.45	-1.35	-1.25	V
			$VLCHG2-VLCHG0 = "7"$		-1.50	-1.40	-1.30	V
SVD voltage (1)	V_{SVD1}	1.5V system	$SVDS1 = "0"$, $SVDS0 = "0"$		-1.10	-1.05	-1.00	V
			$SVDS1 = "0"$, $SVDS0 = "1"$		-1.25	-1.20	-1.15	V
SVD voltage (2)	V_{SVD2}	3.0V system	$SVDS1 = "1"$, $SVDS0 = "0"$		-1.40	-1.35	-1.30	V
			$SVDS1 = "1"$, $SVDS0 = "1"$		-1.40	-1.35	-1.30	V
SVD circuit response time	t_{SVD}						100	μsec
Power current consumption *1	I_{OP}	During HALT (32kHz) During HALT (32kHz) During HALT (32kHz) During execution (32kHz) *2 During execution (32kHz) *2 During execution (32kHz) *2 During A/D operation (32kHz, $V_{SS}=-1.5V$) *3 During A/D operation (32kHz, $V_{SS}=-3.0V$) *3 During SVD operation (32kHz) *4 During execution (1 MHz, ceramic oscillation) *2	Normal mode	no panel load			1.2	$2.5 \mu A$
			Halver mode				650	$1,200 nA$
			Doubler mode				2.5	$5.0 \mu A$
			OSCC = "0"				3.5	$6.0 \mu A$
			Normal mode				2.0	$4.0 \mu A$
			Halver mode	VSCHG = "0"			7.5	$15.0 \mu A$
			Doubler mode				100	$150 \mu A$
			Normal mode				200	$300 \mu A$
			Halver mode				10	$20 \mu A$
			Normal mode				170	$300 \mu A$
			Execution (1 MHz, CR oscillation) *2	no panel load			220	$350 \mu A$
			Execution (1 MHz, CR oscillation) *2, *5					

*1 LPWR = "1", $VLCHG2-VLCHG0 = "0"$, within the operating voltage in each operating mode.

*2 The A/D converter and SVD circuit are OFF status.

*3 The SVD circuit is OFF status. Current consumed during HALT (32kHz, Normal mode) + A/D operating current

*4 The A/D converter is OFF status. Current consumed during HALT (32kHz, Normal mode) + SVD operating current

*5 The value in μA can be found by the following expression: $I_{OP} (f_{osc3} = \chi \text{MHz}) = I_{OP} (f_{osc3} = 1\text{MHz}) \times \chi$

*6 $V_{SS}/V_{S2} \leq V_{L1} - 0.2V$

E0C6256

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

Crystal oscillation circuit (OSC1)

(Unless otherwise specified, the values listed below are standard values under the following conditions:

$V_{DD}=0V$, $V_{SS}=-1.5/-3.0V$, Crystal: C-002R ($C_l=35k\Omega$), $C_g=25pF$, $C_d=\text{built-in}$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	$t_{STA} \leq 5\text{sec}$ (V_{SS})	-1.35			V
Oscillation stop voltage	V_{STP}	$t_{STP} \leq 10\text{sec}$ (V_{SS})	-1.35			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC (in chip)		20		pF
Frequency/voltage deviation	f/V	$V_{SS}=-0.9$ to $-3.6V$			5	ppm
Frequency/IC deviation	f/IC		-10		10	ppm
Frequency adjustment range	f/C_g	$C_g=5$ to $25pF$	35	45		ppm
Harmonic oscillation start voltage	V_{HHO}	$C_g=5pF$ (V_{SS})			-3.5	V
Permitted leak resistance	R_{LEAK}	Between OSC1 and V_{DD} , V_{SS}	200			MΩ

CR oscillation circuit (OSC3)

(Unless otherwise specified, the values listed below are standard values under the following conditions:

$V_{DD}=0V$, $V_{SS}=-3.0V$, $R_{CR}=40k\Omega$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	900kHz	30	%
Oscillation start voltage	V_{STA}	(V_{SS})	-2.2			V
Oscillation start time	t_{STA}	$V_{SS}=-2.2$ to $-3.6V$			3	msec
Oscillation stop voltage	V_{STP}	(V_{SS})	-2.2			V

Ceramic oscillation circuit (OSC3)

(Unless otherwise specified, the values listed below are standard values under the following conditions:

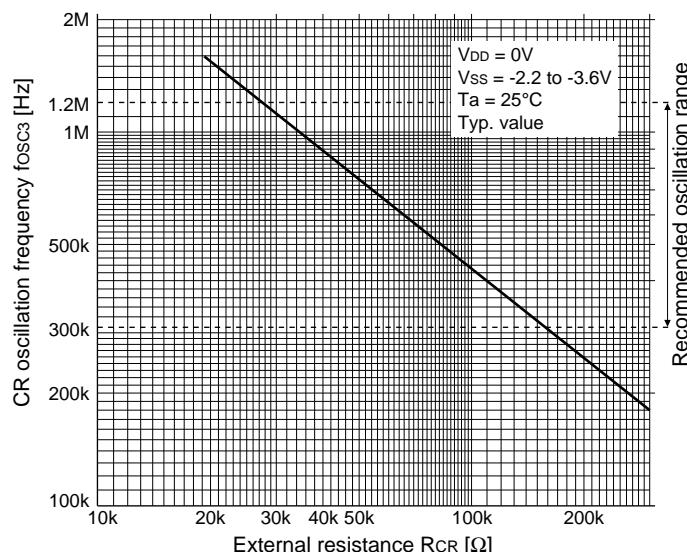
$V_{DD}=0V$, $V_{SS}=-3.0V$, Ceramic oscillator: 1MHz, $C_{GC}=C_{DC}=100pF$, $T_a=25^\circ C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{STA}	(V_{SS})	-2.2			V
Oscillation start time	t_{STA}	$V_{SS}=-2.2$ to $-3.6V$			3	msec
Oscillation stop voltage	V_{STP}	(V_{SS})	-2.2			V

● Characteristic Curves

• CR oscillation frequency characteristic

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values and evaluate the characteristics on the actual product.

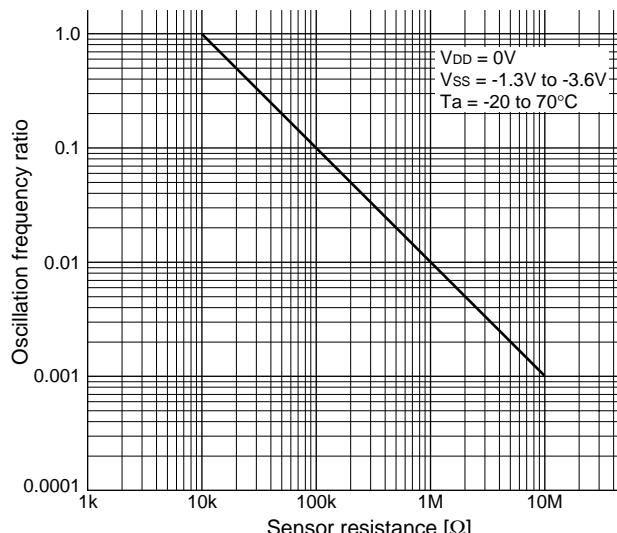


• **A/D converter sensor resistance - oscillation frequency ratio characteristic**

The following figure shows the oscillation frequency ratio (ratio of oscillation frequency by the reference resistance to oscillation frequency by the sensor resistance) when the following elements are connected. (Typ.)

Reference resistance 10 kΩ
 Sensor resistance 10 kΩ to 20 MΩ¹
 Oscillating capacitor 2,200 pF

Note: If the R-f conversion uses a resistive sensor for channel 0 and channel 1, and the R-f conversion uses a resistive humidity sensor for channel 1, both characteristics will be the same.

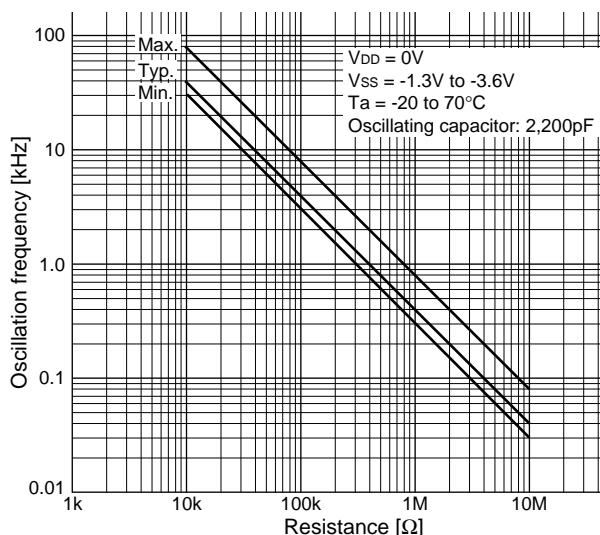


• **A/D converter resistance - oscillation frequency characteristic**

CR oscillation frequency of the A/D converter disperses in each sampling. Therefore, the count number of the up-counter should be decided after considering the fluctuation margin of the CR oscillation frequency by the reference resistance and sensor resistance to be used for the measurement.

Note:

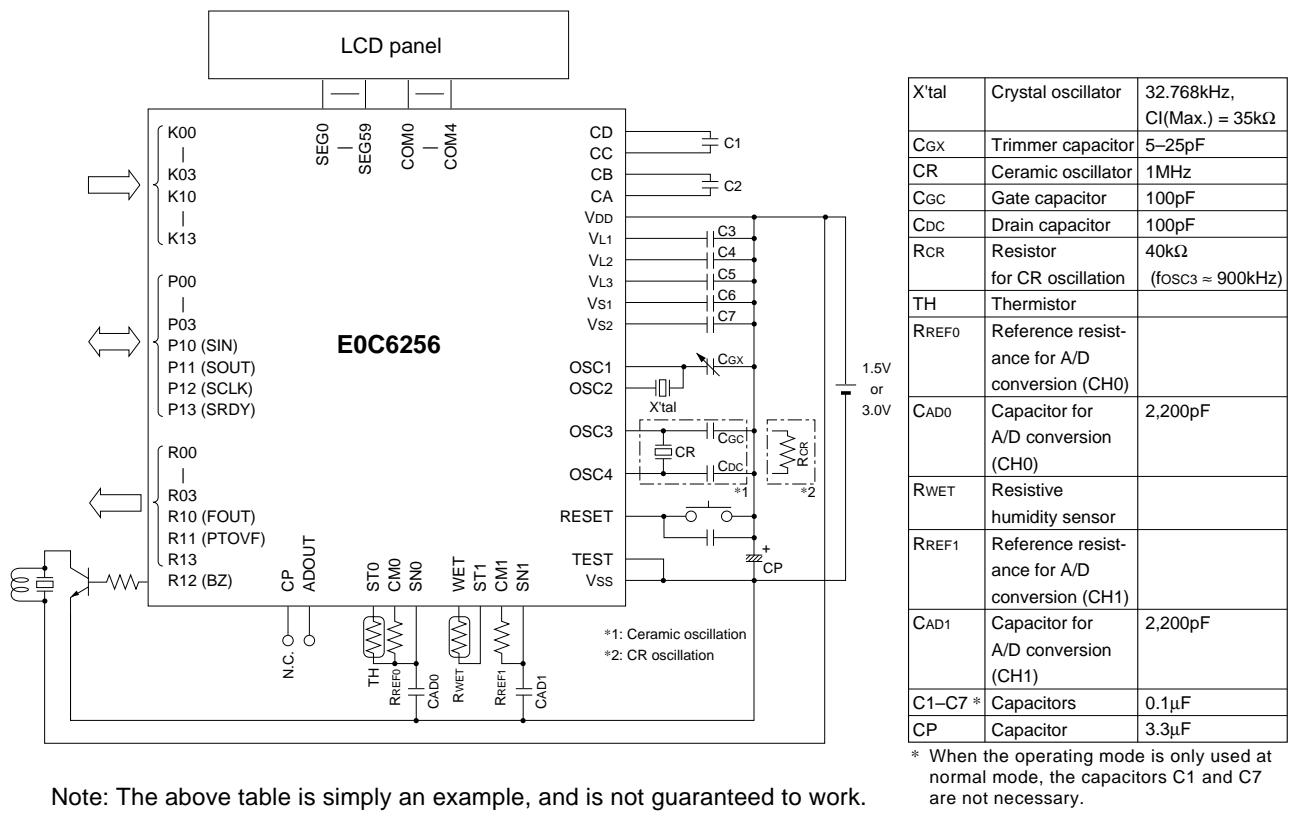
- The following curves are characteristic when the oscillating capacitor is 2,200 pF.
- Typical oscillation frequency is characteristic when V_{SS} = -3.0 V.
- The resistance value applies to both reference resistance and sensor resistance.
- If the R-f conversion uses a resistive sensor for channel 0 and channel 1, and the R-f conversion uses a resistive humidity sensor for channel 1, both characteristics will be the same.



E0C6256

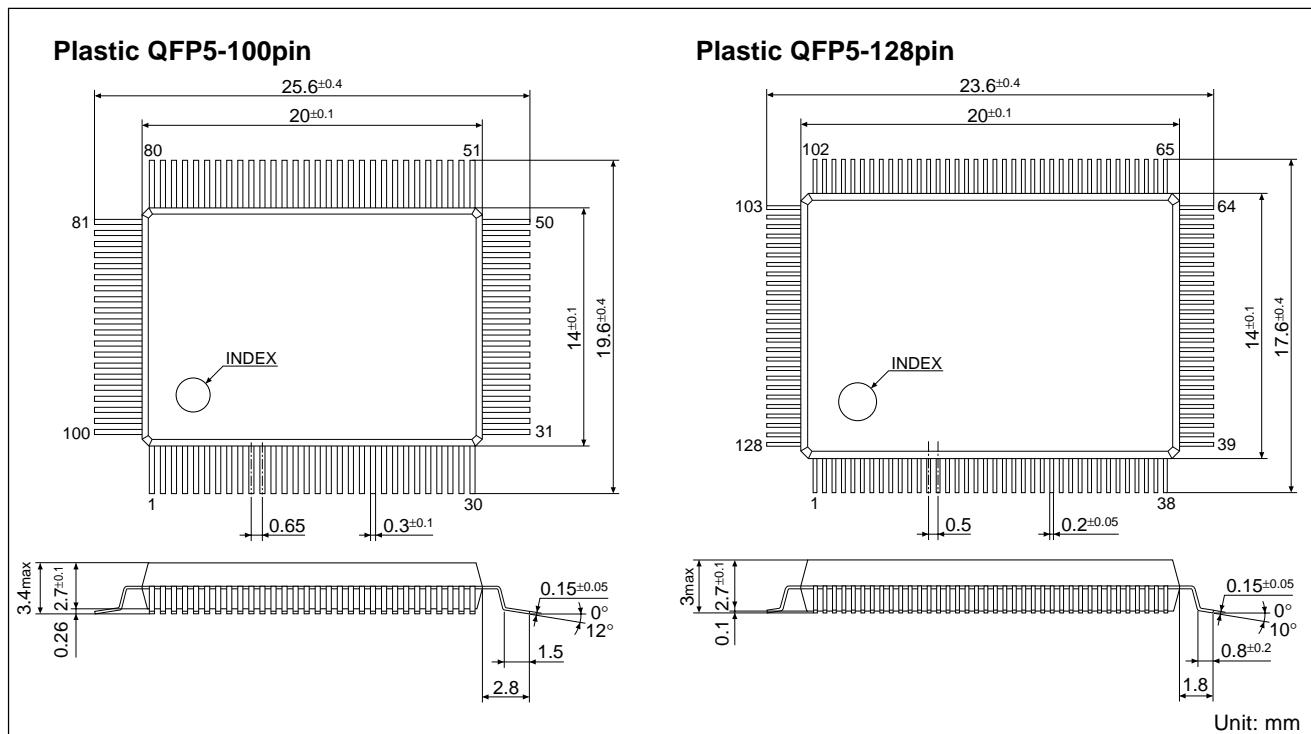
■ BASIC EXTERNAL CONNECTION DIAGRAM

- For temperature measurement using thermistor (CH0) and humidity measurement using resistive humidity sensor (CH1)



Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS



NOTICE:

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Control Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

© Seiko Epson Corporation 1999 All right reserved.

SEIKO EPSON CORPORATION

ELECTRONIC DEVICES MARKETING DIVISION

IC Marketing & Engineering Group

ED International Marketing Department I (Europe & U.S.A.)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN

Phone : 042-587-5812 FAX : 042-587-5564

ED International Marketing Department II (Asia)

421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN

Phone : 042-587-5814 FAX : 042-587-5110

