PRELIMINARY DATA SHEET

KEY FEATURES

- **SMPTE 259M-C compliant descrambling and NRZI → NRZ decoding (with bypass)**

- **DVB-ASI sync word detection and 8b/10b decoding**

- **serial loop-through cable driver output selectable as reclocked or non-reclocked**

- **dual serial digital input buffers with 2 x 1 mux**

- **integrated serial digital signal termination**

- **integrated reclocker**

- **descrambler bypass option**

- **adjustable loop bandwidth**

- **user selectable additional processing features including:**
    - **- TRS, ANC data checksum and EDH CRC error detection and correction**
    - **- programmable ANC data detection**
    - **- illegal code remapping**

- **internal flywheel for noise immune H, V, F extraction**

- **FIFO load Pulse**

- **20-bit / 10-bit CMOS parallel output data bus**

- **27MHz / 13.5MHz parallel digital output**

- **automatic standards detection and indication**

- **1.8V core power supply and 3.3V charge pump power supply**

- **3.3V digital I/O supply**

- **JTAG test interface**

- **small footprint compatible with GS1560A, GS1561, GS1532 and GS9062**

APPLICATIONS

- SMPTE 259M-C Serial Digital Interfaces

- DVB-ASI Serial Digital Interfaces

DESCRIPTION

The GS9060 is a reclocking deserializer with a serial loop-through cable driver. When used in conjunction with any Gennum cable equalizer and the GO1525 Voltage Controlled Oscillator, a receive solution can be realized for SD-SDI and DVB-ASI applications.

In addition to reclocking and deserializing the input data stream, the GS9060 performs NRZI-to-NRZ decoding, descrambling as per SMPTE 259M-C, and word alignment when operating in SMPTE mode. When operating in DVB-ASI mode, the device will word align the data to K28.5 sync characters and 8b/10b decode the received stream.

Two serial digital input buffers are provided with a 2x1 multiplexer to allow the device to select from one of two serial digital input signals.
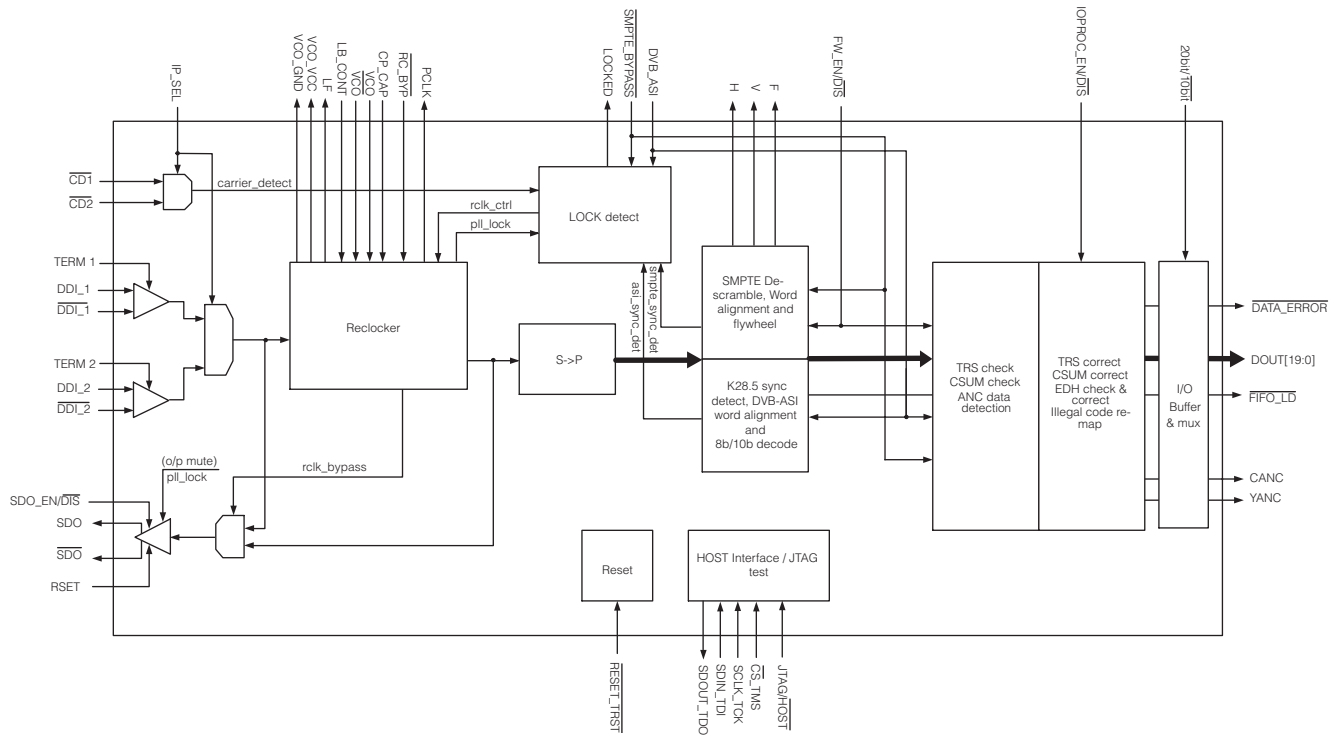
The integrated reclocker features a very wide Input Jitter Tolerance of ±0.3 UI (total 0.6 UI), a rapid asynchronous lock time, and full compliance with DVB-ASI data streams.

An integrated cable driver is provided for serial input loop-through applications and can be selected to output either buffered or reclocked data. This cable driver also features an output mute on loss of signal, high impedance mode, and adjustable signal swing.

The GS9060 also includes a range of data processing functions such as error detection and correction, automatic standards detection, and EDH support. The device can also detect and extract SMPTE 352M payload identifier packets and independently identify the received video standard. This information is read from internal registers via the host interface port.

TRS errors, EDH CRC errors and ancillary data checksum errors can all be detected. A single 'DATA_ERROR' pin is provided which is a logical 'OR'ing of all detectable errors. Individual error status is stored in internal 'ERROR_STATUS' registers.

Finally, the device can correct detected errors and insert new TRS ID words, ancillary data checksum words, and EDH CRC words. Illegal code re-mapping is also available. All processing functions may be individually enabled or disabled via host interface control.
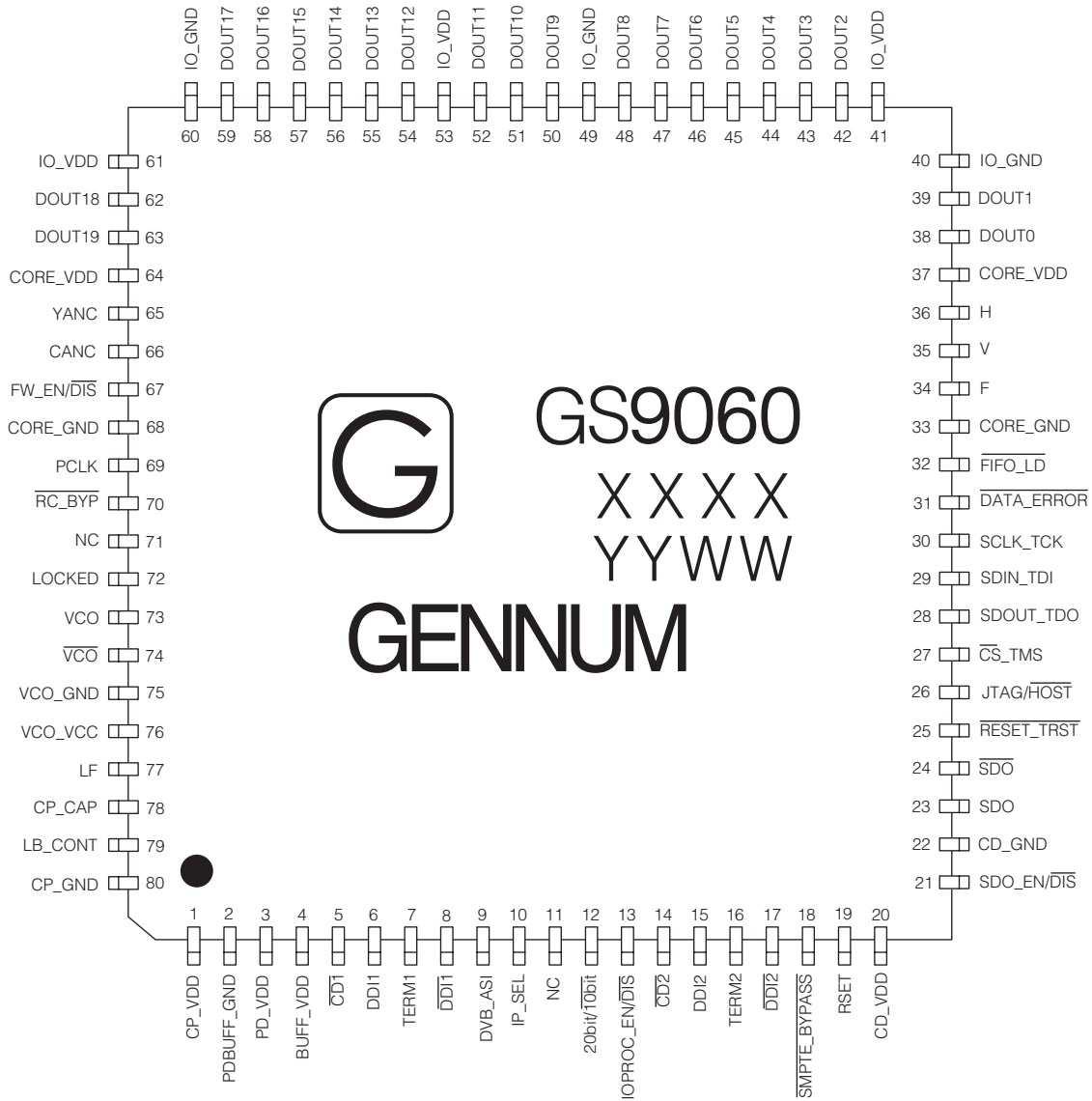
GS9060 FUNCTIONAL BLOCK DIAGRAM

TABLE OF CONTENTS

GS9060

GENNUM CORPORATION

GS9060

GENNUM CORPORATION

22208 - 0

1. PIN OUT

1.1 PIN ASSIGNMENT

Top pins (left to right): 60 IO_GND, 59 DOUT17, 58 DOUT16, 57 DOUT15, 56 DOUT14, 55 DOUT13, 54 DOUT12, 53 IO_VDD, 52 DOUT11, 51 DOUT10, 50 DOUT9, 49 IO_GND, 48 DOUT8, 47 DOUT7, 46 DOUT6, 45 DOUT5, 44 DOUT4, 43 DOUT3, 42 DOUT2, 41 IO_VDD

Left pins (top to bottom): IO_VDD 61, DOUT18 62, DOUT19 63, CORE_VDD 64, YANC 65, CANC 66, FW_EN/$\overline{DIS}$ 67, CORE_GND 68, PCLK 69, $\overline{RC\_BYP}$ 70, NC 71, LOCKED 72, VCO 73, $\overline{VCO}$ 74, VCO_GND 75, VCO_VCC 76, LF 77, CP_CAP 78, LB_CONT 79, CP_GND 80

Center: G, GS9060, X X X X, YYWW, GENNUM

Right pins (top to bottom): 40 IO_GND, 39 DOUT1, 38 DOUT0, 37 CORE_VDD, 36 H, 35 V, 34 F, 33 CORE_GND, 32 $\overline{FIFO\_LD}$, 31 $\overline{DATA\_ERROR}$, 30 SCLK_TCK, 29 SDIN_TDI, 28 SDOUT_TDO, 27 $\overline{CS\_TMS}$, 26 JTAG/$\overline{HOST}$, 25 $\overline{RESET\_TRST}$, 24 $\overline{SDO}$, 23 SDO, 22 CD_GND, 21 SDO_EN/$\overline{DIS}$

Bottom pins (left to right): 1 CP_VDD, 2 PDBUFF_GND, 3 PD_VDD, 4 BUFF_VDD, 5 $\overline{CD1}$, 6 DDI1, 7 TERM1, 8 $\overline{DDI1}$, 9 DVB_ASI, 10 IP_SEL, 11 NC, 12 20bit/$\overline{10bit}$, 13 IOPROC_EN/$\overline{DIS}$, 14 $\overline{CD2}$, 15 DDI2, 16 TERM2, 17 $\overline{DDI2}$, 18 SMPTE_BYPASS, 19 RSET, 20 CD_VDD

1.2 PIN DESCRIPTIONS

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
1	CP_VDD	-	Power	Power supply connection for the charge pump. Connect to +3.3V DC analog.
2	PDBUFF_GND	-	Power	Ground connection for the phase detector and serial digital input buffers. Connect to analog GND.
3	PD_VDD	-	Power	Power supply connection for the phase detector. Connect to +1.8V DC analog.
4	BUFF_VDD	-	Power	Power supply connection for the serial digital input buffers. Connect to +1.8V DC analog.
5	$\overline{CD1}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic cable equalizer. When LOW, the serial digital input signal received at the DDI1 and $\overline{DDI1}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.
6,8	DDI1, $\overline{DDI1}$	Analog	Input	Differential input pair for serial digital input 1.
7	TERM1	Analog	Input	Termination for serial digital input 1. AC couple to PDBUFF_GND.
9	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH in conjunction with $\overline{SMPTE\_BYPASS}$ = LOW, the device will be configured to operate in DVB-ASI mode. When set LOW, the device will not support the decoding or word alignment of received DVB-ASI data.
10	IP_SEL	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select DDI1 / $\overline{DDI1}$ or DDI2 / $\overline{DDI2}$ as the serial digital input signal, and $\overline{CD1}$ or $\overline{CD2}$ as the carrier detect input signal. When set HIGH, DDI1 / $\overline{DDI1}$ is selected as the serial digital input and $\overline{CD1}$ is selected as the carrier detect input signal. When set LOW, DDI2 / $\overline{DDI2}$ serial digital input and $\overline{CD2}$ carrier detect input signal is selected.
11	NC	-	-	No Connect.
12	20bit/$\overline{10bit}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select the output data bus width in SMPTE or Data-Through modes. This signal is ignored in DVB-ASI mode. When set HIGH, the parallel output will be 20-bit demultiplexed data. When set LOW, the parallel outputs will be 10-bit multiplexed data.

GS9060

GENNUM CORPORATION

GS9060

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
13	IOPROC_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • EDH CRC Error Correction • ANC Data Checksum Correction • TRS Error Correction • Illegal Code Remapping To enable a subset of these features, keep IOPROC_EN/$\overline{\text{DIS}}$ HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accesible via the host interface. When set LOW, the I/O processing features of the device are disabled, regardless of whether the features are enabled in the IOPROC_DISABLE register.
14	$\overline{\text{CD2}}$	Non Synchronous	Input	STATUS SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of a serial digital input signal. Normally generated by a Gennum automatic cable equalizer. When LOW, the serial digital input signal received at the DDI2 and $\overline{\text{DDI2}}$ pins is considered valid. When HIGH, the associated serial digital input signal is considered to be invalid. In this case, the LOCKED signal is set LOW and all parallel outputs are muted.
15,17	DDI_2, $\overline{\text{DDI\_2}}$	Analog	Input	Differential input pair for serial digital input 2.
16	TERM2	Analog	Input	Termination for serial digital input 2. AC couple to PDBUFF_GND.
18	$\overline{\text{SMPTE\_BYPASS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode. When set LOW, the device will not support the descrambling, decoding or word alignment of received SMPTE data. No I/O processing features will be available.
19	RSET	Analog	Input	Used to set the serial digital loop-through output signal amplitude. Connect to CD_VDD through 281Ω +/- 1% for 800mV$_{p-p}$ single-ended output swing.
20	CD_VDD	-	Power	Power supply connection for the serial digital cable driver. Connect to +1.8V DC analog.
21	SDO_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the serial digital output loop-through stage. When set LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When set HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.

22208 - 0

GS9060

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
22	CD_GND	-	Power	Ground connection for the serial digital cable driver. Connect to analog GND.
23, 24	SDO, $\overline{SDO}$	Analog	Output	Serial digital loop-through output signal operating at 270Mb/s. The slew rate of these outputs is automatically controlled to meet SMPTE 259M specifications.
25	$\overline{RESET\_TRST}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Host Mode (JTAG/$\overline{HOST}$ = LOW) When asserted LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance, including the serial digital outputs SDO and $\overline{SDO}$. Must be set HIGH for normal device operation. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH) When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.
26	JTAG/$\overline{HOST}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{CS}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing. When set LOW, $\overline{CS}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as GSPI pins for normal host interface operation.
27	$\overline{CS}$_TMS	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select / Test Mode Select Host Mode (JTAG/$\overline{HOST}$ = LOW) $\overline{CS}$_TMS operates as the host interface chip select, $\overline{CS}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH) $\overline{CS}$_TMS operates as the JTAG test mode select, TMS, and is active HIGH.
28	SDOUT_TDO	Synchronous with SCLK_TCK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{HOST}$ = LOW) SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{HOST}$ = HIGH) SDOUT_TDO operates as the JTAG test data output, TDO.

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION
29	SDIN_TDI	Synchronous with SCLK_TCK	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data In / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SDIN_TDI operates as the JTAG test data input, TDI.
30	SCLK_TCK	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock / Test Clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) SCLK_TCK operates as the JTAG test clock, TCK.
31	$\overline{\text{DATA\_ERROR}}$	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. The $\overline{\text{DATA\_ERROR}}$ signal will be LOW when an error within the received data stream has been detected by the device. This pin is a logical 'OR'ing of all detectable errors listed in the internal ERROR_STATUS register. Once an error is detected, $\overline{\text{DATA\_ERROR}}$ will remain LOW until the start of the next video frame / field, or until the ERROR_STATUS register is read via the host interface. The $\overline{\text{DATA\_ERROR}}$ signal will be HIGH when the received data stream has been detected without error. NOTE: It is possible to program which error conditions are monitored by the device by setting appropriate bits of the ERROR_MASK register HIGH. All error conditions are detected by default.
32	$\overline{\text{FIFO\_LD}}$	Synchronous with PCLK	Output	CONTROL SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used as a control signal for external FIFO(s). Normally HIGH but will go LOW for one PCLK period at SAV.
33, 68	CORE_GND	-	Power	Ground connection for the digital core logic. Connect to digital GND.
34	F	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the ODD / EVEN field of the video signal. The F signal will be HIGH for the entire period of field 2 as indicated by the F bit in the received TRS signals. The F signal will be LOW for all lines in field 1 and for all lines in progressive scan systems.

GS9060

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION	
35	V	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video field / frame that is used for vertical blanking. The V signal will be HIGH for the entire vertical blanking period as indicated by the V bit in the received TRS signals. The V signal will be LOW for all lines outside of the vertical blanking interval.	
36	H	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the portion of the video line containing active video data. H signal timing is configurable via the H_CONFIG bit of the IOPROC_DISABLE register accessible via the host interface. Active Line Blanking (H_CONFIG = 0_h) The H signal will be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting. TRS Based Blanking (H_CONFIG = 1_h) The H signal will be HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise.	
37, 64	CORE_VDD	-	Power	Power supply connection for the digital core logic. Connect to +1.8V DC digital.	
38, 39, 42–48, 50	DOUT[0:9]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT9 is the MSB and DOUT0 is the LSB.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW Forced LOW in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
				10-bit mode 20bit/$\overline{10bit}$ = LOW	Forced LOW in all modes.
40, 49, 60	IO_GND	-	Power	Ground connection for digital I/O buffers. Connect to digital GND.	
41, 53, 61	IO_VDD	-	Power	Power supply connection for digital I/O buffers. Connect to +3.3V DC digital.	

GS9060

GS9060

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION	
51, 52, 54–59, 62, 63	DOUT[10:19]	Synchronous with PCLK	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DOUT19 is the MSB and DOUT10 is the LSB.	
				20-bit mode 20bit/$\overline{10bit}$ = HIGH	Luma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data output in Data-Through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
				10-bit mode 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data output in SMPTE mode $\overline{SMPTE\_BYPASS}$ = HIGH DVB_ASI = LOW Data input in data through mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data in DVB-ASI mode $\overline{SMPTE\_BYPASS}$ = LOW DVB_ASI = HIGH
65	YANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the YANC signal will be HIGH when VANC or HANC data is detected in the luma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the YANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.	
66	CANC	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Used to indicate the presence of ancillary data in the video stream. For 20-bit demultiplexed data (20bit/$\overline{10bit}$ = HIGH), the CANC signal will be HIGH when VANC or HANC data is detected in the chroma video stream and LOW otherwise. For 10-bit multiplexed data (20bit/$\overline{10bit}$ = LOW), the CANC signal will be HIGH when VANC or HANC data is detected anywhere in the data stream and LOW otherwise.	
67	FW_EN/$\overline{DIS}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the noise immune flywheel of the device. When set HIGH, the internal flywheel is enabled. This flywheel is used in the extraction and generation of TRS timing signals, in automatic video standards detection, and in manual switch line lock handling. When set LOW, the internal flywheel is disabled and TRS correction and insertion is unavailable.	

PIN NUMBER	NAME	TIMING	TYPE	DESCRIPTION	
69	PCLK	-	Output	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible.	
				20-bit mode	PCLK = 13.5MHz
				10-bit mode	PCLK = 27MHz
70	$\overline{RC\_BYP}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH, the serial digital output will be a reclocked version of the input signal regardless of whether the device is in SMPTE, DVB-ASI or Data-Through mode. When set LOW, the serial digital output will be a buffered version of the input signal in all modes.	
71	NC	-	-	No connect.	
72	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode, or when the reclocker has achieved lock in Data-Through mode. It will be LOW otherwise.	
73, 74	VCO, $\overline{VCO}$	Analog	Input	Differential inputs for the external VCO reference signal. For single ended devices such as the GO1525, $\overline{VCO}$ should be AC coupled to VCO_GND.	
75	VCO_GND	-	Output Power	Ground reference for the external voltage controlled oscillator. Connect to pins 2, 4, 6, and 8 of the GO1525. This pin is an output. Should be isolated from all other grounds.	
76	VCO_VCC	-	Output Power	Power supply for the external voltage controlled oscillator. Connect to pin 5 of the GO1525. This pin is an output. Should be isolated from all other power supplies.	
77	LF	Analog	Output	Control voltage to external voltage controlled oscillator. Nominally +1.25V DC.	
78	CP_CAP	Analog	Input	PLL lock time constant capacitor connection. Normally connected to VCO_GND through 2.2nF.	
79	LB_CONT	Analog	Input	Control voltage to set the loop bandwidth of the integrated reclocker. Normally connected to VCO_GND through 40kΩ.	
80	CP_GND	-	Power	Ground connection for the charge pump. Connect to analog GND.	

GS9060

2. ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIUMUM RATINGS

PARAMETER	VALUE/UNITS
Supply Voltage Core	-0.3V to +2.1V
Supply Voltage I/O	-0.3V to +4.6V
Input Voltage Range (any input)	-2.0V to + 5.25V
Ambient Operating Temperature	$-20°C \leq T_A \leq 85°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
Lead Temperature (soldering, 10 sec)	230°C

NOTES:

1. See reflow solder profile
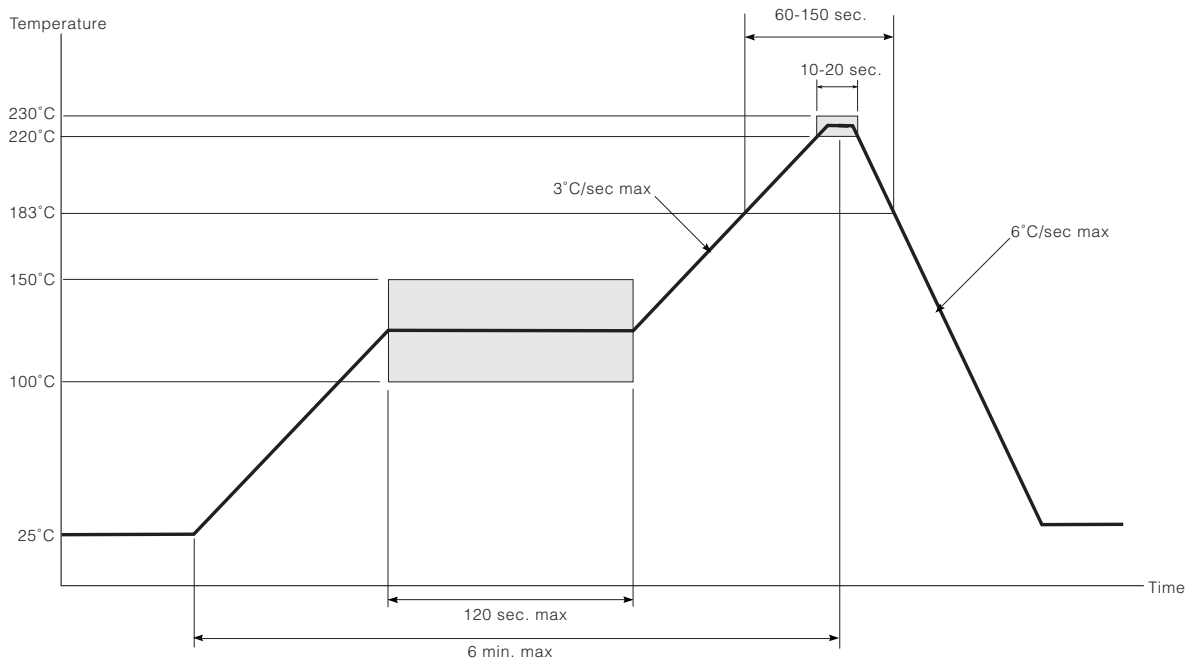

Figure 1   Reflow Solder Profile

13 of 47

2.2 DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL	NOTES
SYSTEM								
Operation Temperature Range	T_A		0	-	70	°C	-	1
Function Temperature Range			-25	-	85	°C	-	2
Digital Core Supply Voltage	CORE_VDD		1.65	1.8	1.95	V	1	1
Digital I/O Supply Voltage	IO_VDD		3.0	3.3	3.6	V		
Charge Pump Supply Voltage	CP_VDD		3.0	3.3	3.6	V		
Phase Detector Supply Voltage	PD_VDD		1.65	1.8	1.95	V		
Input Buffer Supply Voltage	BUFF_VDD		1.65	1.8	1.95	V		
Cable Driver Supply Voltage	CD_VDD		1.71	1.8	1.89	V		
External VCO Supply Voltage Output	VCO_VCC		2.25	2.50	2.75	V	1	-
+1.8V Supply Current	I_{1V8}		-	-	245	mA	7	6
+3.3V Supply Current	I_{3V3}		-	-	55	mA	7	-
Total Device Power	P_D		-	-	625	mW	7	6
ESD Protection on all Pins	-		1	-	-	kV	-	3
DIGITAL I/O								
Input Logic LOW	V_{IL}		-	-	0.8	V	1	-
Input Logic HIGH	V_{IH}		2.1	-	-	V	1	-
Output Logic LOW	V_{OL}		-	0.2	0.4	V	1	-
Output Logic HIGH	V_{OH}		IO_VDD - 0.4	-	-	V	1	-
INPUT								
Input Common Mode Voltage	V_{CMIN}		-	1.45	-	V	6	4
RSET Voltage	V_{RSET}	RSET=281Ω	0.54	0.6	0.66	V	1	5
OUTPUT								
Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET=281Ω	0.8	1.0	1.2	V	1	-

TEST LEVELS
1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES
1. All DC and AC electrical parameters within specification.
2. Guaranteed functional.
3. MIL STD 883 ESD protection will be applied to all pins on the device.
4. Input common mode is set by internal biasing resistors.
5. Set by the value of the RSET resistor.
6. Loop-through enabled.

2.3 AC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $70°C$, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL	NOTES
SYSTEM								
Serial Digital Input Jitter Tolerance	IJT	Nominal loop bandwidth	0.6	-	-	UI	1	1
Slave Mode Asynchronous Lock Time		No data to SD	-	-	197	us	6,7	2
		No data to DVB-ASI	-	-	68			
Device Latency		SMPTE and Data-Through modes	-	21	-	PCLK	6	-
		DVB-ASI mode	-	11	-			
Reset Pulse Width	t_{reset}		1	-	-	ms	7	6
SERIAL DIGITAL DIFFERENTIAL INPUT								
Serial Input Data Rate	DR_{DDI}		-	270	-	Mb/s	1	-
Serial Digital Input Signal Swing	ΔV_{DDI}	Differential with internal 100Ω input termination	200	600	1000	mV_{p-p}	1	-
SERIAL DIGITAL OUTPUT								
Serial Output Data Rate	DR_{SDO}		-	270	-	Mb/s	1	-
Serial Output Swing	ΔV_{SDO}	RSET = 281Ω Load = 75Ω	-	800	-	mVp-p	1	-
Serial Output RiseTime 20% ~ 80%	tr_{SDO}	ORL compensation using recommended circuit	400	550	1500	ps	1	-
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	ORL compensation using recommended circuit	400	550	1500	ps	1	-
Serial Output Intrinsic Jitter	t_{IJ}	Pseudorandom and pathological	-	270	350	ps	1	3
Serial Output Duty Cycle Distortion	DCD_{SDO}		-	20	-	ps	1	4
PARALLEL OUTPUT								
Parallel Clock Frequency	f_{PCLK}		13.5	-	27.0	MHz	1	
Parallel Clock Duty Cycle	DC_{PCLK}		40	50	60	%	1	
Output Data Hold Time	t_{OH}		19.5	-	-	ns	1	5
Output Data Delay Time	t_{OD}		-	-	22.8	ns	1	5
Output Data Rise/Fall Time	tr/tf		-	-	1.5	ns	3	5

GS9060

2.3   AC ELECTRICAL CHARACTERISTICS (CONTINUED)

T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL	NOTES
GSPI								
GSPI Input Clock Frequency	f_{SCLK}		-	-	6.6	MHz	1	-
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	3	-
GSPI Input Data Setup Time			0	-	-	ns	3	-
GSPI Input Data Hold Time			-	-	1.43	ns	3	-
GSPI Output Data Hold Time			2.10	-	-	ns	3	-
GSPI Output Data Delay Time			-	-	7.27	ns	3	-

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. 6MHz sinewave modulation.
2. SD = 525i
3. Serial Digital Output Reclocked ($\overline{RC\_BYP}$ = HIGH).
4. Serial Duty Cycle Distortion is defined here to be the difference between the width of a '1' bit, and the width of a '0' bit.
5. With 15pF load.
6. See Section 3.15, Figure 21.

2.4 INPUT/OUTPUT CIRCUITS

All resistors in ohms, all capacitors in farads, unless otherwise shown.
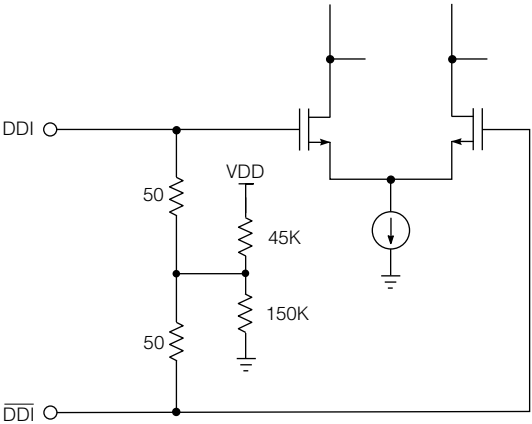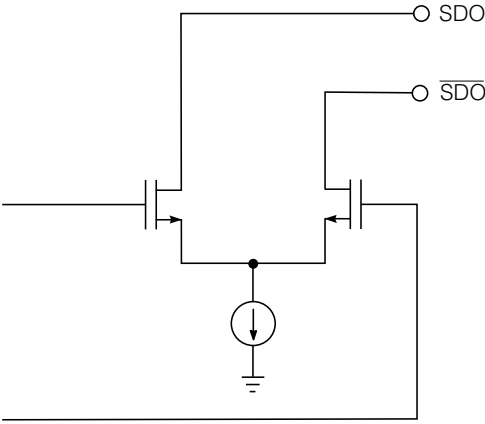
Figure 2   Serial Digital Input
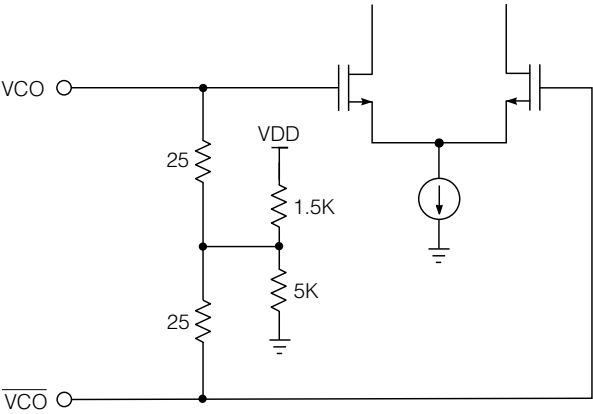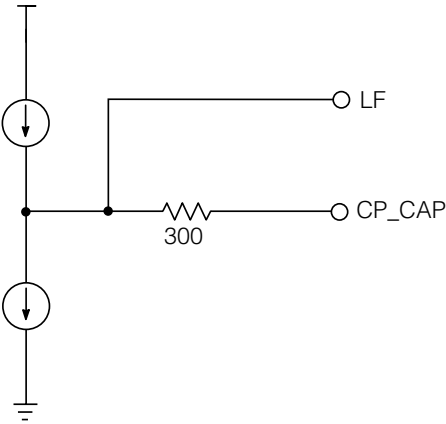
Figure 5   Serial Digital Output

Figure 3   VCO Input
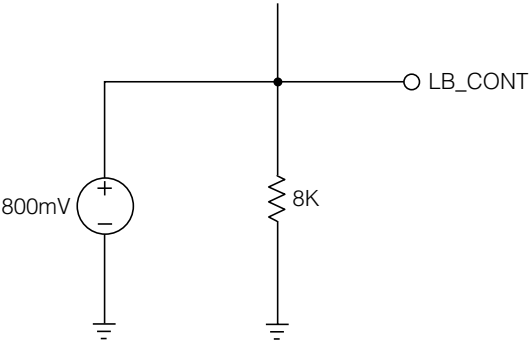
Figure 6   VCO Control Output & PLL Lock Time Capacitor

Figure 4   PLL Loop Bandwidth Control

2.5 HOST INTERFACE MAP

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR_MASK	1Ah	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR_MASK	FF_CRC_ERR_MASK	AP_CRC_ERR_MASK	LOCK_ERR_MASK	Not Used	CS_ERR_MASK	Not Used	Not Used	Not Used	SAV_ERR_MASK	EAV_ERR_MASK
FF_LINE_END_F1	19h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1	18h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0	17h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0	16h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1	15h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1	14h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0	13h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0	12h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE4	11h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3	10h	Not Used	Not Used	Not Used	Not Used	Not Used	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2	0Fh	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1	0Eh	Not Used	Not Used	Not Used	Not Used	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B	0Dh	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A	0Ch	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Bh																
	0Ah																
ANC_TYPE5	09h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE4	08h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE3	07h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE2	06h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE1	05h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_STANDARD	04h	Not Used	VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0	INT_PROG	STD_LOCK	Not Used	Not Used	Not Used	Not Used	DF-b3	DF-b2	DF-b1	DF-b0
EDH_FLAG	03h	Not Used	ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	02h																
ERROR_STATUS	01h	Not Used	Not Used	Not Used	Not Used	Not Used	VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR	Not Used	CS_ERR	Not Used	Not Used	Not Used	SAV_ERR	EAV_ERR
IOPROC_DISABLE	00h	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	H_CONFIG	Not Used	Not Used	ILLEGAL_REMAP	EDH_CRC_INS	ANC_CSUM_INS	Not Used	Not Used	TRS_INS

2.5.1 Host Interface Map (R/W registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERROR_MASK	1Ah						VD_STD_ERR_MASK	FF_CRC_ERR_MASK	AP_CRC_ERR_MASK	LOCK_ERR_MASK	Not Used	CS_ERR_MASK	Not Used	Not Used	Not Used	SAV_ERR_MASK	EAV_ERR_MASK
FF_LINE_END_F1	19h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F1	18h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_END_F0	17h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
FF_LINE_START_F0	16h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F1	15h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F1	14h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_END_F0	13h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
AP_LINE_START_F0	12h							b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	11h																
	10h																
	0Fh																
	0Eh																
	0Dh																
	0Ch																
	0Bh																
	0Ah																
ANC_TYPE5	09h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE4	08h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE3	07h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE2	06h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
ANC_TYPE1	05h	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	04h																
	03h																
	02h																
	01h																
IOPROC_DISABLE	00h								H_CONFIG			ILLEGAL_REMAP	EDH_CRC_INS	ANC_CSUM_INS			TRS_INS

GS9060

2.5.2 Host Interface Map (Read only registers)

REGISTER NAME	ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1Ah																
	19h																
	18h																
	17h																
	16h																
	15h																
	14h																
	13h																
	12h																
RASTER_STRUCTURE4	11h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE3	10h						b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE2	0Fh					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
RASTER_STRUCTURE1	0Eh					b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
VIDEO_FORMAT_OUT_B	0Dh	VFO4-b7	VFO4-b6	VFO4-b5	VFO4-b4	VFO4-b3	VFO4-b2	VFO4-b1	VFO4-b0	VFO3-b7	VFO3-b6	VFO3-b5	VFO3-b4	VFO3-b3	VFO3-b2	VFO3-b1	VFO3-b0
VIDEO_FORMAT_OUT_A	0Ch	VFO2-b7	VFO2-b6	VFO2-b5	VFO2-b4	VFO2-b3	VFO2-b2	VFO2-b1	VFO2-b0	VFO1-b7	VFO1-b6	VFO1-b5	VFO1-b4	VFO1-b3	VFO1-b2	VFO1-b1	VFO1-b0
	0Bh																
	0Ah																
	09h																
	08h																
	07h																
	06h																
	05h																
VIDEO_STANDARD	04h		VDS-b4	VDS-b3	VDS-b2	VDS-b1	VDS-b0	INT_PROG	STD_LOCK					DF-b3	DF-b2	DF-b1	DF-b0
EDH_FLAG	03h		ANC-UES	ANC-IDA	ANC-IDH	ANC-EDA	ANC-EDH	FF-UES	FF-IDA	FF-IDH	FF-EDA	FF-EDH	AP-UES	AP-IDA	AP-IDH	AP-EDA	AP-EDH
	02h																
ERROR_STATUS	01h						VD_STD_ERR	FF_CRC_ERR	AP_CRC_ERR	LOCK_ERR		CS_ERR				SAV_ERR	EAV_ERR
	00h																

3. DETAILED DESCRIPTION

3.1 FUNCTIONAL OVERVIEW

The GS9060 is a dual-standard reclocking deserializer with an integrated serial digital loop-through output. When used in conjunction with any Gennum cable equalizer and the external GO1525 Voltage Controlled Oscillator, a receive solution at 270Mb/s is realized.

The application layer must set external device pins for the correct reception of either SMPTE or DVB-ASI data. The GS9060 also supports the reclocking and deserializing of data not conforming to SMPTE or DVB-ASI streams.

The provided serial loop-through outputs may be selected as either buffered or reclocked versions of the input signal and feature a high impedance mode, output mute on loss of signal and adjustable signal swing.

In the digital signal processing core, several data processing functions are implemented including error detection and correction and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GS9060 contains a JTAG interface for boundary scan test implementations.

3.2 SERIAL DIGITAL INPUT

The GS9060 contains two current mode differential serial digital input buffers, allowing the device to be connected to two SMPTE 259M-C compliant input signals.

Both input buffers have internal 50Ω termination resistors which are connected to ground via the TERM1 and TERM2 pins. The input common mode level is set by internal biasing resistors such that the serial digital input signals must be AC coupled into the device. Gennum recommends using a capacitor value of 4.7uF to accommodate pathological signals.

The input buffers use a separate power supply of +1.8V DC supplied via the BUFF_VDD and PDBUFF_GND pins.

3.2.1 Input Signal Selection

A 2x1 input multiplexer is provided to allow the application layer to select between the two serial digital input streams using a single external pin. When IP_SEL is set HIGH, serial digital input 1 (DDI1 / $\overline{DDI1}$) is selected as the input to the GS9060's reclocker stage. When IP_SEL is set LOW, serial digital input 2 (DDI2 / $\overline{DDI2}$) is selected.

3.2.2 Carrier Detect Input

For each of the differential inputs, an associated carrier detect input signal is included, ($\overline{CD1}$ and $\overline{CD2}$). These signals are generated by Gennum's family of automatic cable equalizers.

When LOW, $\overline{CDx}$ indicates that a valid serial digital data stream is being delivered to the GS9060 by the equalizer. When HIGH, the serial digital input to the device should be considered invalid. If no equalizer preceeds the device, the application layer should set $\overline{CD1}$ and $\overline{CD2}$ accordingly.

NOTE: If the GS9064 Automatic Cable Equalizer is used, the MUTE/$\overline{CD}$ output signal from that device must be translated to TTL levels before passing to the GS9060 $\overline{CDx}$ inputs. See Section 4.1 for a recommended transistor network that will set the correct voltage levels.

A 2x1 input multiplexer is also provided for these signals. The internal carrier_detect signal is determined by the setting of the IP_SEL pin and is used by the lock detect block of the GS9060 to determine the lock status of the device, (see Section 3.6).

3.2.3 Single Input Configuration

If the application requires a single differential input, the second set of inputs may be left unconnected. Tie the associated carrier detect pin HIGH, and leave the termination pin unconnected.

3.3 SERIAL DIGITAL RECLOCKER

The output of the 2x1 serial digital input multiplexer passes to the GS9060's internal reclocker stage. The function of this block is to lock to the input data stream, extract a clean clock, and retime the serial digital data to remove high frequency jitter.

The reclocker was designed with a 'hexabang' phase and frequency detector. That is, the PFD used can identify six 'degrees' of phase / frequency misalignment between the input data stream and the clock signal provided by the VCO, and correspondingly signal the charge pump to produce six different control voltages. This results in fast and accurate locking of the PLL to the data stream.

If lock is achieved, the reclocker provides an internal pll_lock signal to the lock detect block of the device.

3.3.1 External VCO

The GS9060 requires the external GO1525 Voltage Controlled Oscillator as part of the reclocker's phase-locked loop. This external VCO implementation was chosen to ensure high quality reclocking.

Power for the external VCO is generated entirely by the GS9060 from an integrated voltage regulator. The internal regulator uses +3.3V DC supplied via the CP_VDD / CP_GND pins to provide +2.5V DC on the VCO_VCC / VCO_GND pins.

The control voltage to the VCO is output from the GS9060 on the LF pin and requires 4.7kΩ pull-up and pull-down resistors to ensure correct operation.

The GO1525 produces a reference signal for the reclocker, input on the VCO pin of the GS9060. Both LF and VCO signals should be referenced to the supplied VCO_GND as shown in the recommended application circuit of Section 4.1.

3.3.2 Loop Bandwidth

The loop bandwidth of the integrated reclocker is nominally 1.4MHz, but may be increased or decreased via the LB_CONT pin. It is recommended that this pin be connected to VCO_GND through 39.2kΩ to maximize the input jitter tolerance of the device.

3.4 SERIAL DIGITAL LOOP-THROUGH OUTPUT

The GS9060 contains an integrated current mode differential serial digital cable driver with automatic slew rate control. When enabled, this serial digital output provides an active loop-through of the input signal.

To enable the loop-through output, SDO_EN/$\overline{\text{DIS}}$ must be set HIGH by the application layer. Setting the SDO_EN/$\overline{\text{DIS}}$ signal LOW will cause the SDO and $\overline{\text{SDO}}$ output pins to become high impedance, resulting in reduced device power consumption.

With suitable external return loss matching circuitry, the GS9060's loop-through outputs will provide a minimum output return loss of -15dB at 270Mb/s.

The integrated cable driver uses a separate power supply of +1.8V DC supplied via the CD_VDD and CD_GND pins.

3.4.1 Output Swing

Nominally, the voltage swing of the serial digital loop-through output is 800mV$_{p-p}$ single-ended into a 75Ω load. This is set externally by connecting the RSET pin to CD_VDD through 281Ω.

The loop-through output swing may be decreased by increasing the value of the RSET resistor. The relationship is approximated by the curve shown in Figure 7.

Alternatively, the serial digital output can drive 800mVp-p into a 50Ω load. Since the output swing is reduced by a factor of approximately one third when the smaller load is used, the RSET resistor must be 187Ω to obtain 800mVp-p.
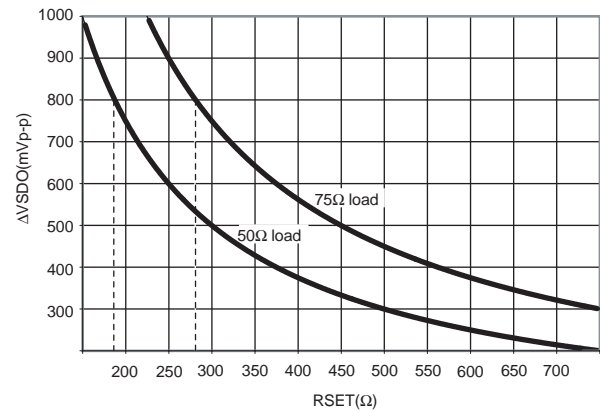

Figure 7 Serial Digital Loop-Through Output Swing

3.4.2 Reclocker Bypass Control

The serial digital loop-through output may be either a buffered version of the serial digital input signal, or a reclocked version of that signal.

The application layer may choose the reclocked output by setting $\overline{\text{RC\_BYP}}$ to logic HIGH. If $\overline{\text{RC\_BYP}}$ is set LOW, the data stream will bypass the internal reclocker and the serial digital output will be a buffered version of the input.

3.4.3 Serial Digital Output Mute

The GS9060 will automatically mute the serial digital loop-through output when the internal carrier_detect signal indicates an invalid serial input.

The loop-through output will also be muted when SDO/$\overline{\text{SDO}}$ is selected as reclocked, ($\overline{\text{RC\_BYP}}$ = HIGH), but the lock detect block has failed to lock to the data stream, (LOCKED = LOW).

Table 1 summarizes the possible states of the serial digital loop-through output data stream.

TABLE 1 SERIAL DIGITAL LOOP-THROUGH OUTPUT STATUS

SDO	$\overline{\text{CD}}$	LOCKED	$\overline{\text{RC\_BYP}}$
RECLOCKED	LOW	HIGH	HIGH
BUFFERED	LOW	X	LOW
MUTED	LOW	LOW	HIGH
MUTED	HIGH	LOW*	X

*NOTE: LOCKED = HIGH if and only if $\overline{\text{CD}}$ = LOW

GS9060

3.5 SERIAL-TO-PARALLEL CONVERSION

The retimed data and phase-locked clock signals from the reclocker are fed to the serial-to-parallel converter. The function of this block is to extract 10-bit data words from the reclocked serial data stream and present them to the SMPTE and DVB-ASI word alignment blocks simultaneously.

3.6 LOCK DETECT

The lock detect block controls the center frequency of the integrated reclocker to ensure lock to the received serial digital data stream is achieved, and indicates via the LOCKED output pin that the device has detected the appropriate sync words.

Lock detection is a continuous process, which begins at device power up or after a system reset, and continues until the device is powered down or held in reset.

The lock detection algorithm first determines if a valid serial digital input signal has been presented to the device by sampling the internal carrier_detect signal. As described in Section 3.2.2, this signal will be LOW when a good serial digital input signal has been detected.

If the carrier_detect signal is HIGH, the serial data into the device is considered invalid, and the VCO frequency will be set to the center of the pull range. The LOCKED pin will be LOW and all outputs of the device except for the PCLK output will be muted. Instead, the PCLK output frequency will operate within +/-3% of the rates shown in Table 15 of Section 3.11.5.

NOTE: When the device is operating in DVB-ASI mode, the parallel outputs will not mute when the carrier_detect signal is HIGH. The LOCKED signal will function normally.

If a valid input signal has been detected the lock algorithm will enter a hunt phase where four attempts are made to detect the presence of either SMPTE TRS sync words or DVB-ASI sync words. The center frequency of the reclocker will be 270Mb/s.

Assuming that a valid SMPTE or DVB-ASI signal has been applied to the device, asynchronous lock times will be as listed in AC Characteristics, (see Section 2.3)

NOTE: The PCLK output will continue to operate during the lock detection process. The frequency may toggle will be 27MHz when the 20bit/$\overline{10bit}$ pin is set LOW, and 13.5MHz when 20bit/$\overline{10bit}$ is set HIGH.

For SMPTE and DVB-ASI inputs, the lock detect block will only assert the LOCKED output signal HIGH if (1) the reclocker has locked to the input data stream as indicated by the internal pll_lock signal, and (2) TRS or DVB-ASI sync words have been correctly identified.

If after four attempts lock has not been achieved, the lock detection algorithm will enter into PLL lock mode. In this mode, the reclocker will attempt to lock to the input data stream without detecting SMPTE TRS or DVB-ASI sync words. This unassisted process can take up to 10ms to achieve lock.

When reclocker lock as indicated by the internal pll_lock signal is achieved in this mode, data will be passed directly to the parallel outputs without any further processing taking place and the LOCKED signal will be asserted HIGH if and only if the $\overline{SMPTE\_BYPASS}$ and DVB_ASI input pins are set LOW.

3.6.1 Input Control Signals

The GS9060 contains three input control signals which determine how the device locks to the input.

It is required that the application layer set the $\overline{SMPTE\_BYPASS}$ and DVB_ASI inputs to reflect the appropriate input data format. If either is configured incorrectly, the device will not lock to the input data stream, and the $\overline{DATA\_ERROR}$ pin will be set LOW.

The third input signal, $\overline{RC\_BYP}$, allows the application layer to determine whether the serial digital loop-through output will be a reclocked or buffered version of the input, (see Section 3.4.2). Table 2 shows the required settings for various input formats.

TABLE 2 INPUT CONTROL SIGNALS

FORMAT	PIN SETTINGS	
	$\overline{SMPTE\_BYPASS}$	DVB_ASI
SD SMPTE	HIGH	LOW
DVB-ASI	LOW	HIGH
NOT SMPTE OR DVB-ASI*	LOW	LOW

*NOTE: See Section 3.9 for a complete description of Data-Through mode.

3.7 SMPTE FUNCTIONALITY

The GS9060 is said to be in SMPTE mode once the device has detected SMPTE TRS sync words and locked to the input data stream as described in Section 3.6. The device will remain in SMPTE mode until such time that SMPTE TRS sync words fail to be detected.

The lock detect block may also drop out of SMPTE mode under the following conditions:

- $\overline{RESET\_TRST}$ is asserted LOW

- $\overline{CDx}$ is HIGH

- $\overline{SMPTE\_BYPASS}$ is asserted LOW

- DVB_ASI is asserted HIGH

TRS word detection is a continuous process and both 8-bit and 10-bit TRS words will be identified by the device.

The application layer must assert the DVB_ASI pin LOW and the $\overline{SMPTE\_BYPASS}$ pin HIGH in order to enable SMPTE operation.

3.7.1 SMPTE Descrambling and Word Alignment

After serial-to-parallel conversion, the internal 10-bit data bus is fed to the SMPTE descramble and word alignment block. The function of this block is to carry out NRZI-to-NRZ decoding, descrambling according to SMPTE 259M, and word alignment of the data to the TRS sync words.

Word alignment occurs when three consecutive valid TRS words (SAV and EAV inclusive) with the same bit alignment have been detected (1½ video lines).

In normal operation, re-synchronization of the word alignment process will only take place when two consecutive identical TRS word positions have been detected. When automatic or manual switch line lock handling is 'actioned', (see Section 3.7.3), word alignment re-synchronization will occur on the next received TRS code word.

3.7.2 Internal Flywheel

The GS9060 has an internal flywheel which is used in the generation of internal / external timing signals, in the detection and correction of certain error conditions and in automatic video standards detection. It is only operational in SMPTE mode.

The flywheel consists of a number of counters and comparators operating at video pixel and video line rates. These counters maintain information about the total line length, active line length, total number of lines per field / frame, and total active lines per field / frame for the received video stream.

The flywheel 'learns' the video standard by timing the horizontal and vertical reference information contained in the TRS ID words of the received video stream. Full synchronization of the flywheel to the received video standard therefore requires one complete video frame.

Once synchronization has been achieved, the flywheel will continue to monitor the received TRS timing information to maintain synchronization.

The FW_EN/$\overline{DIS}$ input pin controls the synchronization mechanism of the flywheel. When this input signal is LOW, the flywheel will re-synchronize all pixel and line based counters on every received TRS ID word.

When FW_EN/$\overline{DIS}$ is held HIGH, re-synchronization of the pixel and line based counters will only take place when a consistent synchronization error has been detected. Two consecutive video lines with identical TRS timing different to the current flywheel timing must occur to initiate re-synchronization of the counters. This provides a measure of noise immunity to internal and external timing signal generation.

The flywheel will be disabled should the LOCKED signal or the $\overline{RESET\_TRST}$ signal be LOW. A LOW to HIGH transistion on either signal will cause the flywheel to re-acquire synchronization on the next received TRS word, regardless of the setting of the FW_EN/$\overline{DIS}$ pin.

3.7.3 Switch Line Lock Handling

The principal of switch line lock handling is that the switching of synchronous video sources will only disturb the horizontal timing and alignment of the stream, whereas the vertical timing remains in synchronization.

To account for the horizontal disturbance caused by a synchronous switch, it is necessary to re-synchronize the flywheel immediately after the switch has taken place. Rapid re-synchronization of the GS9060 to the new video standard can be achieved by controlling the flywheel using the FW_EN/$\overline{DIS}$ pin.

At every PCLK cycle the device samples the FW_EN/$\overline{DIS}$ pin. When a logic LOW to HIGH transition at this pin is detected anywhere within the active line, the flywheel will re-synchronize immediately to the next TRS word. This is shown in Figure 8.

To ensure switch line lock handling, the FW_EN/$\overline{DIS}$ signal should be LOW for a minimum of one PCLK cycle (maximum one video line) anywhere within the active portion of the line on which the switch has taken place.
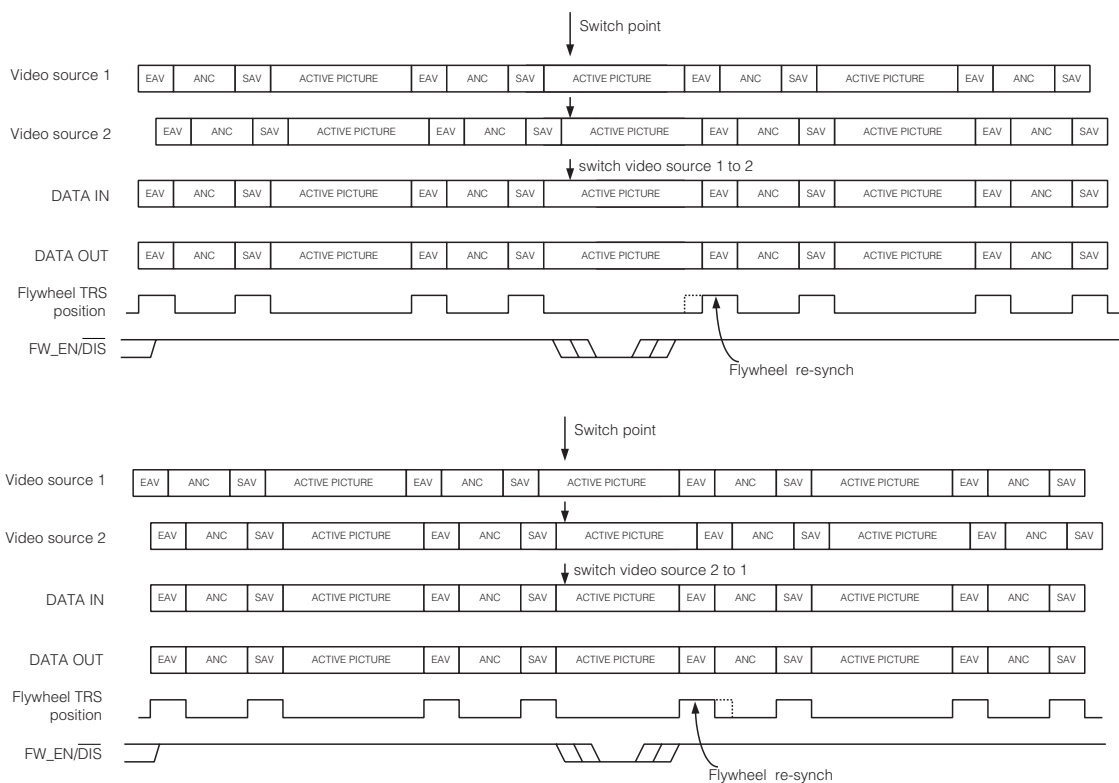
Figure 8   Switch Line Locking

The ability to manually re-synchronize the flywheel is also important when switching asynchronous sources or to implement other non-standardized video switching functions.

The GS9060 also implements automatic switch line lock handling. By utilizing the synchronous switch points defined by SMPTE RP168 for all major video standards with the automatic video standards detect function, the device automatically re-synchronizes the flywheel at the switch point.

This function will occur regardless of the setting of the FW_EN/$\overline{\text{DIS}}$ pin.

The switch line is defined as follows:

- For 525 line interlaced systems: re-sync takes place at the end of lines 10 & 273.

- For 525 line progressive systems: re-sync takes place at the end of line 10.

- For 625 line interlaced systems: re-sync takes place at the end of lines 6 & 319.

- For 625 line progressive systems: re-sync takes place at the end of line 6.

A full list of all major video standards and switching lines is shown in Table 3.

NOTE: The flywheel timing will define the line count such that the line numbers shown in Table 3 may not correspond directly to the digital line counts.

TABLE 3   SWITCH LINE POSITION FOR DIGITAL SYSTEMS

SYSTEM	VIDEO FORMAT	SAMPLING	SIGNAL STANDARD	PARALLEL INTERFACE	SERIAL INTERFACE	SWITCH LINE NO.
SDTI	720x576/50 (2:1)	4:2:2	BT.656	BT.656 + 305M	259M	6, 319
	720x483/59.94 (2:1)		125M	125M + 305M		10, 273
525	960x483/59.94 (2:1)	4:2:2	267M	267M	259M	10, 273
	720x483/59.94 (2:1)	4:4:4:4		347M	344M	
	720x483/59.94 (2:1)			RP174	344M	
	720x483/59.94 (2:1)			RP175	RP175	
	720x483/59.94 (2:1)	4:2:2	125M	125M	259M	
	720x483/59.94 (1:1)	4:2:2	293M	347M	344M	10
	720x483/59.94 (1:1)			293M	294M	
	720x483/59.94 (1:1)	4:2:0		293M	294M	
625	720x576/50 (1:1)	4:2:2	BT.1358	347M	344M	6
	720x576/50 (1:1)			BT.1358	BT.1362	
	720x576/50 (1:1)	4:2:0		BT.1358	BT.1362	
	960x576/50 (2:1)	4:2:2	BT.601	BT.656	259M	6, 319
	720x576/50 (2:1)	4:4:4:4	BT.799	347M	344M	
	720x576/50 (2:1)			BT.799	344M	
	720x576/50 (2:1)			BT.799	-	
	720x576/50 (2:1)	4:2:2	BT.601	125M	259M	

GS9060

22208 - 0

3.7.4 HVF Timing Signal Generation

The GS9060 extracts critical timing parameters from either the received TRS signals (FW_EN/$\overline{\text{DIS}}$ = LOW), or from the internal flywheel-timing generator (FW_EN/$\overline{\text{DIS}}$ = HIGH).

Horizontal blanking period (H), vertical blanking period (V), and even / odd field (F) timing are all extracted and presented to the application layer via the H:V:F status output pins.

The H signal timing is configurable via the H_CONFIG bit of the internal IOPROC_DISABLE register as either active line based blanking, or TRS based blanking, (see Section 3.10.6).

Active line based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H output is HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing used by the device.

When H_CONFIG is set HIGH, TRS based blanking is enabled. In this case, the H output will be HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words.

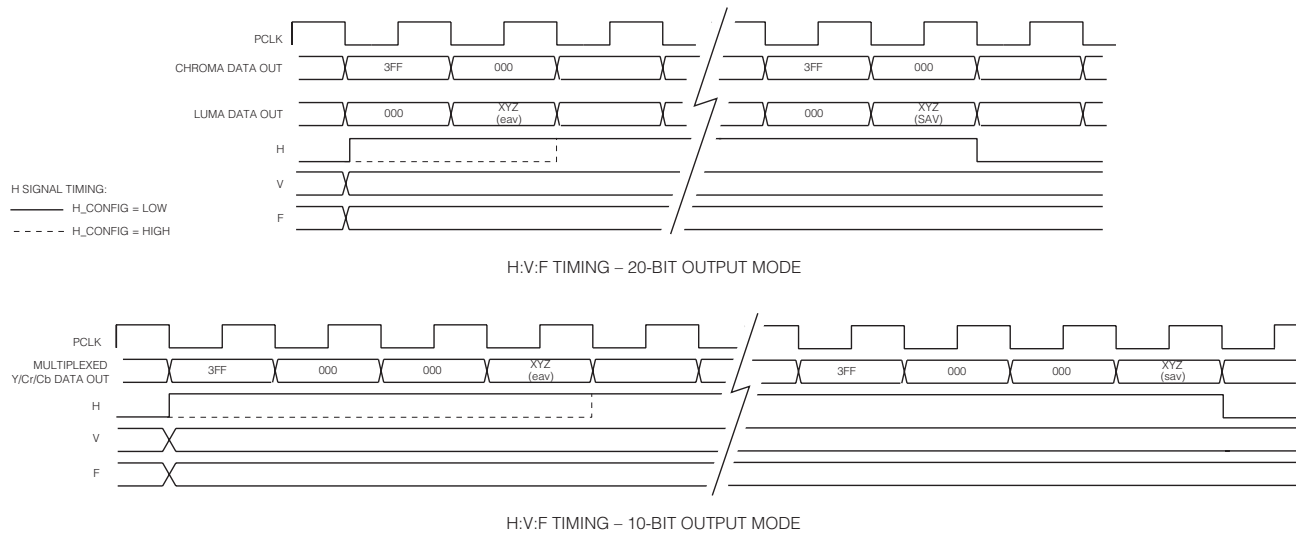The timing of these signals is shown in Figure 9.

H:V:F TIMING – 20-BIT OUTPUT MODE

H:V:F TIMING – 10-BIT OUTPUT MODE

Figure 9   H, V, F Timing

22208 - 0

3.8 DVB-ASI FUNCTIONALITY

The GS9060 is said to be in DVB-ASI mode once the device has detected 32 consecutive DVB-ASI words without a single word or disparity error being generated. The device will remain in DVB-ASI mode until 32 consecutive DVB-ASI word or disparity errors are detected, or until SMPTE TRS ID words have been detected.

The lock detect block may also drop out of DVB-ASI mode under the following conditions:

- $\overline{\text{RESET\_TRST}}$ is asserted LOW

- $\overline{\text{CDx}}$ is HIGH

- $\overline{\text{SMPTE\_BYPASS}}$ is asserted HIGH

- DVB_ASI is asserted LOW

K28.5 sync patterns in the received DVB-ASI data stream will be detected by the device in either inverted or non-inverted form.

The application layer must set $\overline{\text{SMPTE\_BYPASS}}$ LOW and DVB_ASI HIGH in order to enable DVB-ASI operation.

3.8.1 DVB-ASI 8b/10b Decoding and Word Alignment

After serial-to-parallel conversion, the internal 10-bit data bus is fed to the DVB-ASI 8b/10b decode and word alignment block. The function of this block is to word align the data to the K28.5 sync characters, and 8b/10b decode and bit-swap the data to achieve bit alignment with the data outputs.

The extracted 8-bit data will be presented to DOUT[17:10], bypassing all internal SMPTE mode data processing.

NOTE: When operating in DVB-ASI mode, DOUT[9:0] are forced LOW.

3.8.2 Status Signal Outputs

In DVB-ASI mode, the DOUT19 and DOUT18 pins will be configured as DVB-ASI status signals SYNCOUT and WORDERR respectively.

SYNCOUT will be HIGH whenever a K28.5 sync character is present on the output. This output may be used to drive the write enable signal of an external FIFO, thus providing a means of removing the K28.5 sync characters from the data stream. Parallel DVB-ASI data may then be clocked out of the FIFO at some rate less than 27MHz. See Figure 10.

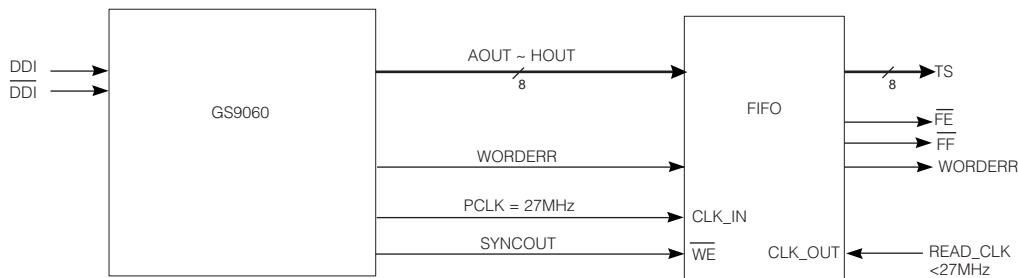WORDERR will be high whenever the device has detected an illegal code word.

Figure 10   DVB-ASI FIFO Implementation using the GS9060

3.9 DATA THROUGH MODE

The GS9060 may be configured by the application layer to operate as a simple serial-to-parallel converter. In this mode, the device presents data to the output data bus without performing any decoding, descrambling or word-alignment.

Data through mode is enabled only when the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI input pins are set LOW. Under these conditions, the lock detection algorithm enters PLL lock mode, (see Section 3.6), such that the device may reclock data not conforming to SMPTE or DVB-ASI streams.

3.10 ADDITIONAL PROCESSING FUNCTIONS

The GS9060 contains an additional data processing block which is available in SMPTE mode only, (see Section 3.7).

3.10.1 FIFO Load Pulse

To aid in the application-specific implementation of auto-phasing and line synchronization functions, the GS9060 will generate a FIFO load pulse to reset line-based FIFO storage.

The $\overline{\text{FIFO\_LD}}$ output pin will normally be HIGH but will go LOW for one PCLK period, thereby generating a FIFO write reset signal.

The FIFO load pulse will be generated such that it is co-timed to the SAV XYZ code word presented to the output data bus. This ensures that the next PCLK cycle will correspond to the first active sample of the video line.

Figure 11 shows the timing relationship between the $\overline{\text{FIFO\_LD}}$ signal and the output video data.
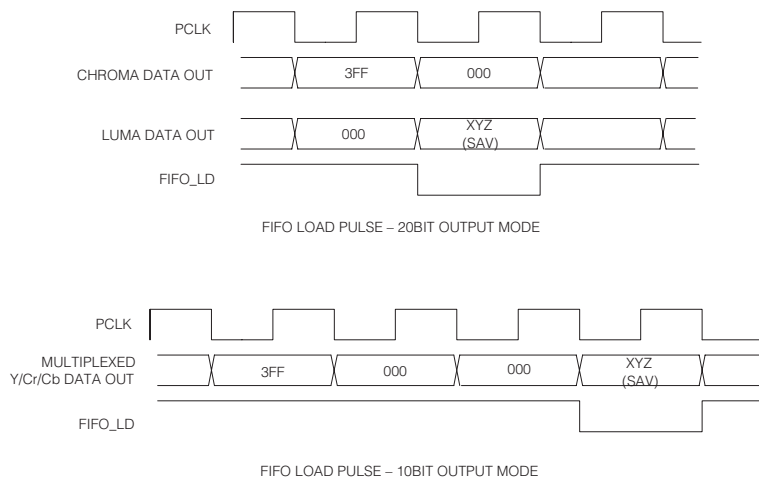
22208 - 0

FIFO LOAD PULSE – 20BIT OUTPUT MODE

FIFO LOAD PULSE – 10BIT OUTPUT MODE

Figure 11 $\overline{\text{FIFO\_LD}}$ Pulse Timing

3.10.2   Ancillary Data Detection and Indication

The GS9060 will detect all types of ancillary data in either the vertical or horizontal blanking spaces and indicate via the status signal output pins YANC and CANC the position of ancillary data in the output data stream. These status signal outputs are synchronous with PCLK and can be used as clock enables to external logic, or as write enables to an external FIFO or other memory device.

The YANC and CANC signal operation will depend on the output data format. For 20-bit demultiplexed data, (see Section 3.11), the YANC and CANC signals will operate independently. However, for 10-bit multiplexed data, the YANC and CANC signals will both be HIGH whenever ancillary data is detected.

The signals will be HIGH from the start of the ancillary data preamble and will remain HIGH until after the ancillary data checksum.

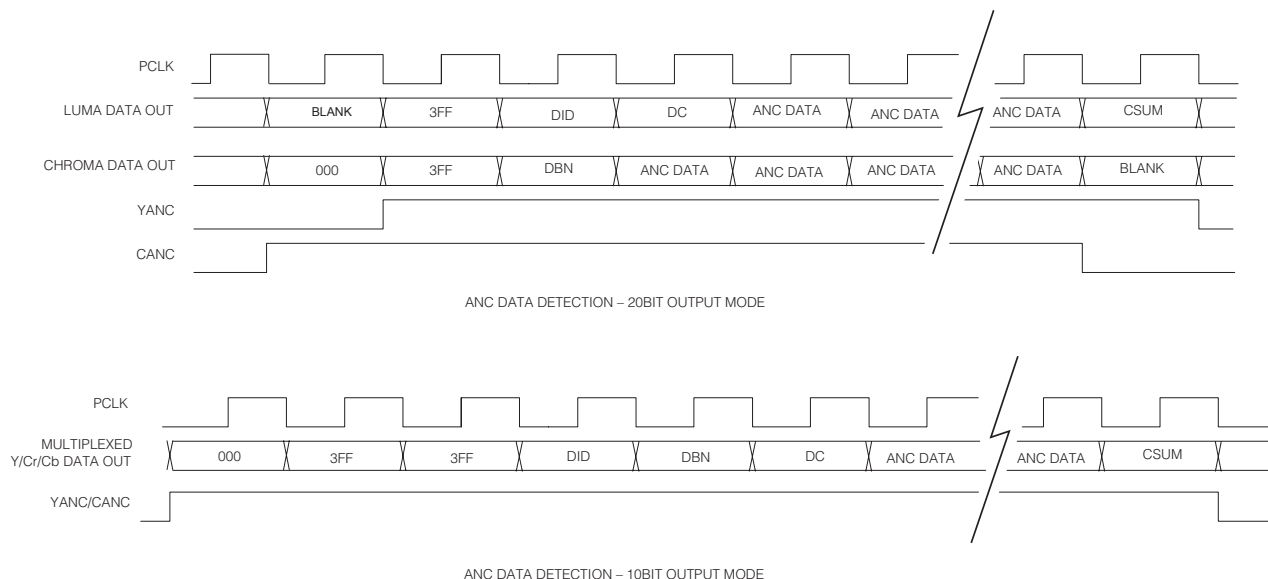The operation of the YANC and CANC signals is shown in Figure 12.

ANC DATA DETECTION – 20BIT OUTPUT MODE

ANC DATA DETECTION – 10BIT OUTPUT MODE

Figure 12   YANC and CANC Output Signal Timing

3.10.2.1 Programmable Ancillary Data Detection

Although the GS9060 will detect all types of ancillary data by default, it also allows the host interface to specifically program up to five different ancillary data types for detection. This is accomplished via the ANC_TYPE register (Table 4).

For each data type to be detected, the host interface must program the DID and/or SDID of the ancillary data type of interest. The GS9060 will compare the received DID and/or SDID with the programmed values and assert YANC and CANC only if an exact match is found.

If any DID or SDID value is set to zero in the ANC_TYPE register, no comparison or match will be made for that value. For example, if the DID is programmed but the SDID is set to zero, the device will detect all ancillary data types matching the DID value, regardless of the SDID.

In the case where all five DID and SDID values are set to zero, the GS9060 will detect all ancillary data types. This is the default setting after device reset.

Where one or more, but less than five, DID and/or SDID values have been programmed, then only those matching ancillary data types will be detected and indicated.

NOTE 1: The GS9060 will always detect EDH ancillary data packets for EDH error detection purposes, regardless of which DID/SDID values have been programmed for ancillary data indication, (see Section 3.10.5.2).

NOTE 2: See SMPTE 291M for a definition of ancillary data terms.

TABLE 4 HOST INTERFACE DESCRIPTION FOR PROGRAMMABLE ANCILLARY DATA TYPE REGISTERS

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
ANC_TYPE1 Address: 05h	15-8	ANC_TYPE1[15:8]	Used to program the DID for ancillary data detection at the YANC and CANC output	R/W	0
	7-0	ANC_TYPE1[7:0]	Used to program the SDID for ancillary data detection at the YANC and CANC output. Should be set to zero if no SDID is present in the ancillary data product to be detected.	R/W	0
ANC_TYPE2 Address: 06h	15-8	ANC_TYPE2[15:8]	Used to program the DID for ancillary data detection at the YANC and CANC output	R/W	0
	7-0	ANC_TYPE2[7:0]	Used to program the SDID for ancillary data detection at the YANC and CANC output. Should be set to zero if no SDID is present in the ancillary data product to be detected.	R/W	0
ANC_TYPE3 Address: 07h	15-8	ANC_TYPE3[15:8]	Used to program the DID for ancillary data detection at the YANC and CANC output	R/W	0
	7-0	ANC_TYPE3[7:0]	Used to program the SDID for ancillary data detection at the YANC and CANC output. Should be set to zero if no SDID is present in the ancillary data product to be detected.	R/W	0
ANC_TYPE4 Address: 08h	15-8	ANC_TYPE4[15:8]	Used to program the DID for ancillary data detection at the YANC and CANC output	R/W	0
	7-0	ANC_TYPE4[7:0]	Used to program the SDID for ancillary data detection at the YANC and CANC output. Should be set to zero if no SDID is present in the ancillary data product to be detected.	R/W	0
ANC_TYPE5 Address: 09h	15-8	ANC_TYPE5[15:8]	Used to program the DID for ancillary data detection at the YANC and CANC output	R/W	0
	7-0	ANC_TYPE5[7:0]	Used to program the SDID for ancillary data detection at the YANC and CANC output. Should be set to zero if no SDID is present in the ancillary data product to be detected.	R/W	0

3.10.3 SMPTE 352M Payload Identifier

The GS9060 can receive and detect the presence of the SMPTE 352M payload identifier ancillary data packet. This four word payload identifier packet may be used to indicate the transport mechanism, frame rate and line scanning / sampling structure.

Upon reception of this packet, the device will extract the four words describing the video format being transported and make this information available to the host interface via the four VIDEO_FORMAT_OUT registers (Table 5).

The VIDEO_FORMAT_OUT registers will only be updated if the received checksum is the same as the locally calculated checksum.

These registers will be cleared to zero, indicating an undefined format, if the device loses lock to the input data stream (LOCKED = LOW), or if the $\overline{\text{SMPTE\_BYPASS}}$ pin is asserted LOW. This is also the default setting after device reset.

The SMPTE 352M packet should be received once per field for interlaced systems and once per frame for progressive systems. If the packet is not received for two complete video frames, the VIDEO_FORMAT_OUT registers will be cleared to zero.

TABLE 5   HOST INTERFACE DESCRIPTION FOR SMPTE 352M PAYLOAD IDENTIFIER REGISTERS

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
VIDEO_FORMAT_OUT_B Address: 0Dh	15-8	SMPTE352M Byte 4	Data will be available in this register when Video Payload Indentification Packets are detected in the data stream.	R	0
	7-0	SMPTE352M Byte 3	Data will be available in this register when Video Payload Indentification Packets are detected in the data stream.	R	0
VIDEO_FORMAT_OUT_A Address: 0Ch	15-8	SMPTE352M Byte 2	Data will be available in this register when Video Payload Indentification Packets are detected in the data stream.	R	0
	7-0	SMPTE352M Byte 1	Data will be available in this register when Video Payload Indentification Packets are detected in the data stream.	R	0

3.10.4 Automatic Video Standard and Data Format Detection

The GS9060 can independently detect the input video standard and data format by using the timing parameters extracted from the received TRS ID words. This information is presented to the host interface via the VIDEO_STANDARD register (Table 6).

Total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are also calculated and presented to the host interface via the RASTER_STRUCTURE registers (Table 7). These line and sample count registers are updated once per frame at the end of line 12. This is in addition to the information contained in the VIDEO_STANDARD register.

After device reset, the four RASTER_STRUCTURE registers default to zero.

3.10.4.1 Video Standard Indication

The video standard codes reported in the VD_STD[4:0] bits of the VIDEO_STANDARD register represent the SMPTE standards as shown in Table 8.

In addition to the 5-bit video standard code word, the VIDEO_STANDARD register also contains an additional status bit. The STD_LOCK bit will be set HIGH whenever the flywheel has achieved full synchronization.

The VD_STD[4:0], and STD_LOCK bits of the VIDEO_STANDARD register will default to zero after device reset. These bits will also default to zero if the device loses lock to the input data stream, (LOCKED = LOW), or if the $\overline{\text{SMPTE\_BYPASS}}$ pin is asserted LOW.

TABLE 6   HOST INTERFACE DESCRIPTION FOR VIDEO STANDARD AND DATA FORMAT REGISTER

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
VIDEO_STANDARD Address: 04h	15	Not Used			
	14-10	VD_STD[4:0]	Video Data Standard (see Table 8)	R	0
	9	Not Used			
	8	STD_LOCK	Standard Lock: Set HIGH when flywheel has achieved full synchronization.	R	0
	7-4	Not Used			
	3-0	DATA_FORMAT[3:0]	Data Format (see Table 9).	R	F_h

TABLE 7   HOST INTERFACE DESCRIPTION FOR RASTER STRUCTURE REGISTERS

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
RASTER_STRUCTURE1 Address: 0Eh	15-12	Not Used			
	11-0	RASTER_STRUCTURE1[11:0]	Words Per Active Line.	R	0
RASTER_STRUCTURE2 Address: 0Fh	15-12	Not Used			
	11-0	RASTER_STRUCTURE2[11:0]	Words Per Total Line.	R	0
RASTER_STRUCTURE3 Address: 10h	15-11	Not Used			
	10-0	RASTER_STRUCTURE3[10:0]	Total Lines Per Frame.	R	0
RASTER_STRUCTURE4 Address: 11h	15-11	Not Used			
	10-0	RASTER_STRUCTURE4[10:0]	Active Lines Per Field.	R	0

TABLE 8   SUPPORTED VIDEO STANDARDS

VD_STD[4:0]	SMPTE STANDARD	VIDEO FORMAT	LENGTH OF HANC	LENGTH OF ACTIVE VIDEO	TOTAL SAMPLES	SMPTE352M LINES
16h	125M	1440x487/60 (2:1) (Or dual link progressive)	268	1440	1716	3, 276
17h		1440x507/60 (2:1)	268	1440	1716	3, 276
19h		525-line 487 generic	-	-	1716	3, 276
1Bh		525-line 507 generic	-	-	1716	3, 276
18h	ITU-R BT.656	1440x576/50 (2:1) (Or dual link progressive)	280	1440	1728	9, 322
1Ah		625-line generic (EM)	-	-	1728	9, 322
1Eh	Unknown SD	-	-	-	-	-
00h-15h, 1Ch, 1Fh	Reserved					

GS9060

3.10.4.2 Data Format Indication

The data format codes will be reported in the DATA_FORMAT[3:0] bits of the VIDEO_STANDARD register. These codes represent the data formats listed in Table 9.

The DATA_FORMAT[3:0] bits of the VIDEO_STANDARD register will default to 'F$_h$' after device reset. These bits will also default to 'F$_h$' if the device loses lock to the input data stream, (LOCKED = LOW), or if Data-Through mode is enabled, (see Section 3.9).

TABLE 9 DATA FORMAT CODES

DATA_FORMAT[3:0]	DATA FORMAT	APPLICABLE STANDARDS
0h	SDTI DVCPRO - No ECC	SMPTE 321M
1h	SDTI DVCPRO - ECC	SMPTE 321M
2h	SDTI DVCAM	SMPTE 322M
3h	SDTI CP	SMPTE 326M
4h	Other SDTI fixed block size	-
5h	Other SDTI variable block size	-
6h	SDI	-
7h	DVB-ASI	-
8h ~ Eh	Reserved	
Fh	Unknown data format	-

3.10.5 Error Detection and Indication

The GS9060 contains a number of error detection functions to enhance operation of the device when operating in SMPTE mode. These functions, (except lock error detection), will not be available in either DVB-ASI or Data-Through operating modes. See Section 3.8 and Section 3.9.

The device maintains an error status register at address 01$_h$ called ERROR_STATUS (Table 10). Each type of error has a specific flag or bit in this register which is set HIGH whenever that error is detected.

The ERROR_STATUS register will be cleared at the start of each video field or when read by the host interface, which ever condition occurs first.

All bits of the ERROR_STATUS register except the LOCK_ERR bit will also be cleared if a change in the video standard is detected, or under the following conditions:

- $\overline{\text{RESET\_TRST}}$ is held LOW

- LOCKED is asserted LOW

- $\overline{\text{SMPTE\_BYPASS}}$ is asserted LOW

In addition to the ERROR_STATUS register, a register called ERROR_MASK (Table 11) is included which allows the host interface to select the specific error conditions that will be detected. There is one bit in the ERROR_MASK register for each type of error represented in the ERROR_STATUS register.

The bits of the ERROR_MASK register will default to '0' after device reset, thus enabling all error types to be detected. The host interface may disable individual error detection by setting the corresponding bit HIGH in this register.

Error conditions are also indicated to the application layer via the status signal pin $\overline{\text{DATA\_ERROR}}$. This output pin is a logical 'OR'ing of each error status flag stored in the ERROR_STATUS register. $\overline{\text{DATA\_ERROR}}$ is normally HIGH, but will be set LOW by the device when an error condition that has not been masked is detected.

TABLE 10   HOST INTERFACE DESCRIPTION FOR ERROR STATUS REGISTER

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
ERROR_STATUS Address: 01h	15-11		Not Used		
	10	VD_STD_ERR	Video Standard Error Flag. Set HIGH when a mismatch between the received SMPTE352M packets and the calculated video standard occurs.	R	0
	9	FF_CRC_ERR	Full Field CRC Error Flag. Set HIGH in SD mode when a Full Field (FF) CRC mismatch has been detected in Field 1 or 2.	R	0
	8	AP_CRC_ERR	Active Picture CRC Error Flag. Set HIGH in SD mode when an Active Picture (AP) CRC mismatch has been detected in Field 1 or 2.	R	0
	7	LOCK_ERR	Lock Error Flag. Set HIGH whenever the LOCK pin is LOW (indicating the device not correctly locked).	R	0
	6		Not Used		
	5	CS_ERR	Luma Checksum Error Flag. Set HIGH when ancillary data packet checksum error has been detected in the Y channel.	R	0
	4-2		Not Used		
	1	SAV_ERR	Start of Active Video Error Flag. Set HIGH when TRS errors are detected in either 8-bit or 10-bit TRS words. FW_EN/$\overline{\text{DIS}}$ must be set HIGH.	R	0
	0	EAV_ERR	End of Active Video Error Flag. Set HIGH when TRS errors are detected in either 8-bit or 10-bit TRS words. FW_EN/$\overline{\text{DIS}}$ must be set HIGH.	R	0

TABLE 11   HOST INTERFACE DESCRIPTION FOR ERROR MASK REGISTER

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
ERROR_MASK Address: 1Ah	15-11		Not Used		
	10	VD_STD_ERR_MASK	Video Standard Error Flag Mask bit.	R/W	0
	9	FF_CRC_ERR_MASK	Full Field CRC Error Flag Mask bit.	R/W	0
	8	AP_CRC_ERR_MASK	Active Picture CRC Error Flag Mask bit.	R/W	0
	7	LOCK_ERR_MASK	Lock Error Flag Mask bit.	R/W	0
	6		Not Used		
	5	CS_ERR_MASK	Checksum Error Flag Mask bit.	R/W	0
	4-2		Not Used		
	1	SAV_ERR_MASK	Start of Active Video Error Flag Mask bit.	R/W	0
	0	EAV_ERR_MASK	End of Active Video Error Flag Mask bit.	R/W	0

GS9060

22208 - 0

3.10.5.1 Video Standard Error Detection

If a mismatch between the received SMPTE 352M packets and the calculated video standard occurs, the GS9060 will indicate a video standard error by setting the VD_STD_ERR bit of the ERROR_STATUS register HIGH.

3.10.5.2 EDH CRC Error Detection

The GS9060 calculates Full Field (FF) and Active Picture (AP) CRC words according to SMPTE RP165 in support of Error Detection and Handling packets in SD signals.

These calculated CRC values are compared with the received CRC values. If a mismatch is detected, the error is flagged in the AP_CRC_ERR and/or FF_CRC_ERR bits of the ERROR_STATUS register. These two flags are shared between fields 1 and 2.

The AP_CRC_ERR bit will be set HIGH when an active picture CRC mismatch has been detected in field 1 or 2. The FF_CRC_ERR bit will be set HIGH when a full field CRC mismatch has been detected in field 1 or 2.

EDH CRC errors will only be indicated when the device is operating in SMPTE mode, and when the device has correctly received EDH packets.

SMPTE RP165 specifies the calculation ranges and scope of EDH data for standard 525 and 625 component digital interfaces. The GS9060 will utilize these standard ranges by default.

If the received video format does not correspond to 525 or 625 digital component video standards as determined by the flywheel pixel and line counters, then one of two schemes for determining the EDH calculation ranges will be employed:

1. Ranges will be based on the line and pixel ranges programmed by the host interface; or

2. In the absence of user-programmed calculation ranges, ranges will be determined from the received TRS timing information.

The registers available to the host interface for programming EDH calculation ranges include active picture and full field line start and end positions for both fields. Table 12 shows the relevant registers, which default to '0' after device reset.

If any or all of these register values are zero, then the EDH CRC calculation ranges will be determined from the flywheel generated H signal. The first active and full field pixel will always be the first pixel after the SAV TRS code word. The last active and full field pixel will always be the last pixel before the start of the EAV TRS code words.

TABLE 12   HOST INTERFACE DESCRIPTION FOR EDH CALCULATION RANGE REGISTERS

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
AP_LINE_START_F0 Address: 12h	15-10	Not Used			
	9-0	AP_LINE_START_F0[9:0]	Field 0 Active Picture start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_END_F0 Address: 13h	15-10	Not Used			
	9-0	AP_LINE_END_F0[9:0]	Field 0 Active Picture end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_START_F1 Address: 14h	15-10	Not Used			
	9-0	AP_LINE_START_F1[9:0]	Field 1 Active Picture end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
AP_LINE_END_F1 Address: 15h	15-10	Not Used			
	9-0	AP_LINE_END_F1[9:0]	Field 1 Active Picture end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_START_F0 Address: 16h	15-10	Not Used			
	9-0	FF_LINE_START_F0[9:0]	Field 0 Full Field start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_END_F0 Address: 17h	15-10	Not Used			
	9-0	FF_LINE_END_F0[9:0]	Field 0 Full Field start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_START_F1 Address: 18h	15-10	Not Used			
	9-0	FF_LINE_START_F1[9:0]	Field 1 Full Field start line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0
FF_LINE_END_F1 Address: 19h	15-10	Not Used			
	9-0	FF_LINE_END_F1[9:0]	Field 1 Full Field end line data used to set EDH calculation range outside of SMPTE RP 165 values.	R/W	0

GS9060

3.10.5.3 Lock Error Detection

The LOCKED pin of the GS9060 indicates the lock status of the reclocker and lock detect blocks of the device. Only when the LOCKED pin is asserted HIGH has the device correctly locked to the received data stream, (see Section 3.6).

The GS9060 will also indicate lock error to the host interface when LOCKED = LOW by setting the LOCK_ERR bit in the ERROR_STATUS register HIGH.

3.10.5.4 Ancillary Data Checksum Error Detection

The GS9060 will calculate checksums for all received ancillary data and compare the calculated values to the received checksum words. If a mismatch is detected, the error is flagged in the CS_ERR bits of the ERROR_STATUS register.

Although the GS9060 will calculate and compare checksum values for all ancillary data types by default, the host interface may program the device to check only certain types of ancillary data checksums.

This is accomplished via the ANC_TYPE register as described in Section 3.10.2.1.

3.10.5.5 TRS Error Detection

TRS errors flags are generated by the GS9060 when:

1. The received TRS timing does not correspond to the internal flywheel timing; or

2. The received TRS hamming codes are incorrect.

Both 8-bit and 10-bit SAV and EAV TRS words are checked for timing and data integrity errors. These are flagged via the SAV_ERR and/or EAV_ERR bits of the ERROR_STATUS register.

Timing-based TRS errors will only be generated if the FW_EN/$\overline{\text{DIS}}$ pin is set HIGH.

3.10.6 Error Correction and Insertion

In addition to signal error detection and indication, the GS9060 may also correct certain types of errors by inserting corrected code words and checksums into the data stream. These features are only available in SMPTE mode and IOPROC_EN/$\overline{\text{DIS}}$ must be set HIGH. Individual correction features may be enabled or disabled via the IOPROC_DISABLE register (Table 13).

All of the IOPROC_DISABLE register bits default to '0' after device reset, enabling all of the processing features. To disable any individual error correction feature, the host interface must set the corresponding bit HIGH in the IOPROC_DISABLE register.

TABLE 13 HOST INTERFACE DESCRIPTION FOR INTERNAL PROCESSING DISABLE REGISTER

REGISTER NAME	BIT	BIT NAME	DESCRIPTION	R/W	DEFAULT
IOPROC_DISABLE Address: 00h	15-9		Not Used		
	8	H_CONFIG	Horizontal sync timing output configuration. Set LOW for active line blanking timing. Set HIGH for H blanking based on the H bit setting of the TRS words. See Figure 9.		0
	7		Not Used		
	6		Not Used		
	5	ILLEGAL_REMAP	Illegal Code re-mapping. Correction of illegal code words within the active picture. Set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin must be set HIGH.	R/W	0
	4	EDH_CRC_INS	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction insertion. Set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin must be set HIGH.	R/W	0
	3	ANC_CSUM_INS	Ancillary Data Check-sum insertion. Set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin must be set HIGH.	R/W	0
	2-1		Not Used		
	0	TRS_INS	Timing Reference Signal Insertion. Set HIGH to disable. The IOPROC_EN/$\overline{\text{DIS}}$ pin must be set HIGH.	R/W	0

3.10.6.1 Illegal Code Remapping

If the ILLEGAL_REMAP bit of the IOPROC_DISABLE register is set LOW, the GS9060 will remap all codes within the active picture between the values of 3FCh and 3FFh to 3FBh. All codes within the active picture area between the values of 000h and 003h will be re-mapped to 004h.

In addition, 8-bit TRS and ancillary data preambles will be remapped to 10-bit values if this feature is enabled.

3.10.6.2 EDH CRC Error Correction

The GS9060 will generate and insert active picture and full field CRC words into the EDH data packets received by the device. This feature is only available in SD mode and is enabled by setting the EDH_CRC_INS bit of the IOPROC_DISABLE register LOW.

EDH CRC calculation ranges are described in Section 3.10.5.2.

NOTE: Although the GS9060 will modify and insert EDH CRC words and EDH packet checksums, EDH error flags will not be updated by the device.

3.10.6.3 Ancillary Data Checksum Error Correction

When ancillary data checksum error correction and insertion is enabled, the GS9060 will generate and insert ancillary data checksums for all ancillary data words by default. Where user specified ancillary data has been programmed into the device (see Section 3.10.2.1), only the checksums for the programmed ancillary data types will be corrected.

This feature is enabled when the ANC_CSUM_INS bit of the IOPROC_DISABLE register is set LOW.

3.10.6.4 TRS Error Correction

When TRS error correction and insertion is enabled, the GS9060 will generate and insert 10-bit TRS code words as required.

TRS word generation will be performed in accordance with the timing parameters generated by the flywheel to provide an element of noise immunity. As a result, TRS correction will only take place if the flywheel is enabled, (FW_EN/$\overline{\text{DIS}}$ = HIGH).

In addition, the TRS_INS bit of the IOPROC_DISABLE register must be set LOW.

3.10.7 EDH Flag Detection

As described in Section 3.10.5.2, the GS9060 can detect EDH packets in the received data stream. The EDH flags for ancillary data, active picture and full field areas are extracted from the detected EDH packets and placed in the EDH_FLAG register of the device (Table 14).

One set of flags is provided for both fields 1 and 2. Field 1 flag data will be overwritten by field 2 flag data.

The EDH_FLAG register may be read by the host interface at any time during the received frame except on the lines defined in SMPTE RP165 where these flags are updated.

NOTE 1: By programming the ANC_TYPE1 register (005h) with the DID word for EDH ancillary packets, the application layer may detect a high-to-low transition on either the YANC or CANC output pin of the GS9060 to determine (a) when EDH packets have been received by the device, and (b) when the EDH_FLAG register can be read by the host interface. See Section 3.10.2 for more information on ancillary data detection and indication.

NOTE 2: The bits of the EDH_FLAG register are sticky and will not be cleared by a read operation. If the GS9060 is decoding a source containing EDH packets, where EDH flags may be set, and the source is replaced by one without EDH packets, the EDH_FLAG register will not be cleared.

NOTE 3: The GS9060 will detect EDH flags, but will not update the flags if an EDH CRC error is detected. Gennum's GS9062 Serializer allows the host to individually set EDH flags.

TABLE 14   HOST INTERFACE DESCRIPTION FOR EDH FLAG REGISTER

REGISTER NAME	BIT	NAME	DESCRIPTION	R/W	DEFAULT
EDH_FLAG Address: 03h	15		Not Used		
	14	ANC-UES out	Ancillary Unknown Error Status Flag.	R	0
	13	ANC-IDA out	Ancillary Internal device error Detected Already Flag.	R	0
	12	ANC-IDH out	Ancillary Internal device error Detected Here Flag.	R	0
	11	ANC-EDA out	Ancillary Error Detected Already Flag.	R	0
	10	ANC-EDH out	Ancillary Error Detected Here Flag.	R	0
	9	FF-UES out	Full Field Unknown Error Status Flag.	R	0
	8	FF-IDA out	Full Field Internal device error Detected Already Flag.	R	0
	7	FF-IDH out	Full Field Internal device error Detected Here Flag.	R	0
	6	FF-EDA out	Full Field Error Detected Already Flag.	R	0
	5	FF-EDH out	Full Field Error Detected Here Flag.	R	0
	4	AP-UES out	Active Picture Unknown Error Status Flag.	R	0
	3	AP-IDA out	Active Picture Internal device error Detected Already Flag.	R	0
	2	AP-IDH out	Active Picture Internal device error Detected Here Flag.	R	0
	1	AP-EDA out	Active Picture Error Detected Already Flag.	R	0
	0	AP-EDH out	Active Picture Error Detected Here Flag.	R	0

3.11   PARALLEL DATA OUTPUTS

Data outputs leave the device on the rising edge of PCLK as shown in Figure 13.

The data may be scrambled or unscrambled, framed or unframed, and may be presented in 10-bit or 20-bit format. The output data bus width is controlled independently from the internal data bus width by the 20bit/$\overline{10bit}$ input pin.

Likewise, the output data format is defined by the setting of the external $\overline{SMPTE\_BYPASS}$ and DVB_ASI pins. Recall that these pins are set by the application layer as inputs to the device.

3.11.1 Parallel Data Bus Buffers

The parallel data outputs of the GS9060 are driven by high-impedance buffers which support both LVTTL and LVCMOS levels. These buffers use a separate power supply of +3.3V DC supplied via the IO_VDD and IO_GND pins.

All output buffers, including the PCLK output, may be driven to a high-impedance state if the $\overline{RESET\_TRST}$ signal is asserted LOW.
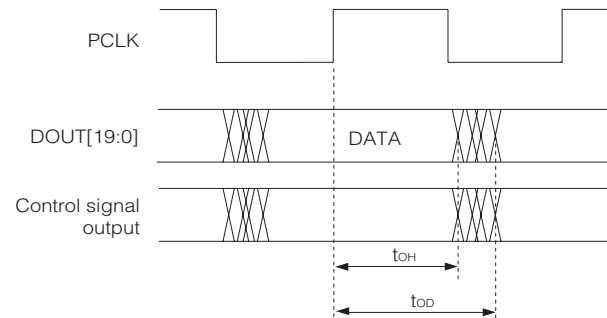
Figure 13   PCLK to Data Timing

3.11.2 Parallel Output in SMPTE Mode

When the device is operating in SMPTE mode, (see Section 3.7), data may be presented to the output bus in either multiplexed or demultiplexed form depending on the setting of the 20bit/10bit input pin.

In 20-bit mode, (20bit/10bit = HIGH), the output data will be word aligned, demultiplexed luma and chroma data. Luma words will always appear on DOUT[19:10] while chroma words will occupy DOUT[9:0].

In 10-bit mode, (20bit/10bit = LOW), the output data will be word aligned, multiplexed luma and chroma data. The data will be presented on DOUT[19:10], and the device will force DOUT[9:0] LOW.

3.11.3 Parallel Output in DVB-ASI Mode

When operating in DVB-ASI mode, (see Section 3.8), the GS9060 automatically configures the output port for 10-bit operation regardless of the setting of the 20bit/10bit pin.

The extracted 8-bit data words will be presented on DOUT[17:10] such that DOUT17 = HOUT is the most significant bit of the decoded transport stream data and DOUT10 = AOUT is the least significant bit.

In addition, DOUT19 and DOUT18 will be configured as the DVB-ASI status signals SYNCOUT and WORDERR respectively. See Section 3.8.2 for a description of these DVB-ASI specific output signals.

DOUT[9:0] will be forced LOW when the GS9060 is operating in DVB-ASI mode.

3.11.4 Parallel Output in Data-Through Mode

When operating in Data-Through mode, (see Section 3.9), the GS9060 presents data to the output data bus without performing any decoding, descrambling or word-alignment.

3.11.5 Parallel Output Clock (PCLK)

The frequency of the PCLK output signal of the GS9060 is determined by the output data format. Table 15 below lists the possible output signal formats and their corresponding parallel clock rates. Note that DVB-ASI output will always be in 10-bit format, regardless of the setting of the 20bit/10bit pin.

TABLE 15 PARALLEL DATA OUTPUT FORMAT

OUTPUT DATA FORMAT	INPUT CONTROL SIGNALS			DOUT [19:10]	DOUT [9:0]	PCLK
	20bit/10bit	SMPTE_BYPASS	DVB_ASI			
SMPTE MODE						
20bit DEMULTIPLEXED	HIGH	HIGH	LOW	LUMA	CHROMA	13.5MHz
10bit MULTIPLEXED	LOW			LUMA / CHROMA	FORCED LOW	27MHz
DVB-ASI MODE						
10bit DVB-ASI	HIGH	LOW	HIGH	DVB-ASI DATA	FORCED LOW	27MHz
	LOW					
DATA-THROUGH MODE						
20bit DEMULTIPLEXED	HIGH	LOW	LOW	DATA	DATA	13.5MHz
10bit MULTIPLEXED	LOW			DATA	FORCED LOW	27MHz

3.12 GSPI HOST INTERFACE

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the host to enable additional features of the device and /or to provide additional status information through configuration registers in the GS9060.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the host interface. The SDOUT pin is a high-impedance output allowing multiple devices to be connected in parallel and selected via the $\overline{CS}$ input. The interface is illustrated in Figure 14.

All read or write access to the GS9060 is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.
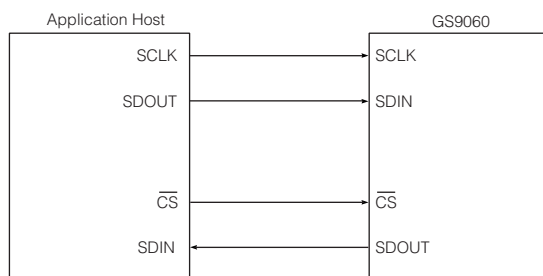
Figure 14   Gennum Serial Peripheral Interface (GSPI)

3.12.1 Command Word Description

The command word is transmitted MSB first and contains a read/write bit, nine reserved bits and a 6-bit register address. Set R/W = '1' to read and R/W = '0' to write from the GSPI.

Command words are clocked into the GS9060 on the rising edge of the serial clock SCLK. The appropriate chip select, $\overline{CS}$, signal must be asserted low a minimum of 1.5ns (t_0 in Figure 17 and Figure 18) before the first clock edge to ensure proper operation.

Each command word must be followed by only one data word to ensure proper operation.

MSB   LSB

| R/W | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV | RSV | A5 | A4 | A3 | A2 | A1 | A0 |

Figure 15   Command Word

MSB   LSB

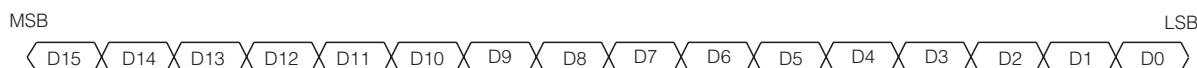| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Figure 16   Data Word

41 of 47

3.12.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 17 and Figure 18 respectively. The maximum SCLK frequency allowed is 6.6MHz.

When writing to the registers via the GSPI, the MSB of the data word may be presented to SDIN immediately following the falling edge of the LSB of the command word. All SDIN data is sampled on the rising edge of SCLK.

When reading from the registers via the GSPI, the MSB of the data word will be available on SDOUT 12ns (t_5 in Figure 17) following the falling edge of the LSB of the command word, and thus may be read by the host on the very next rising edge of the clock. The remaining bits are clocked out by the GS9060 on the negative edges of SCLK.
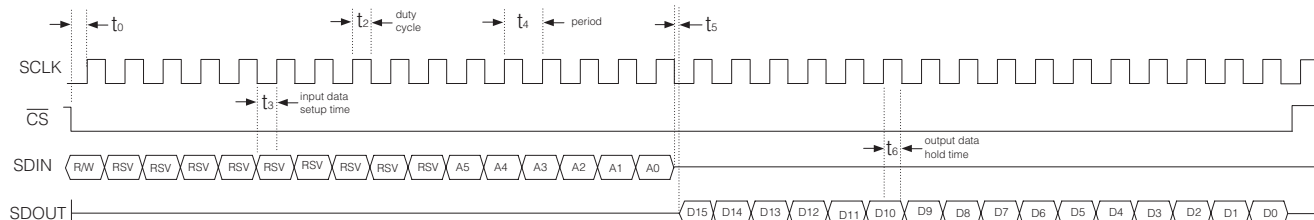

Figure 17 GSPI Read Mode Timing

Figure 18 GSPI Write Mode Timing

3.12.3 Configuration and Status Registers

Table 16 summarizes the GS9060's internal status and configuration registers.

All of these registers are available to the host via the GSPI and are all individually addressable.

Where status registers contain less than the full 16 bits of information however, two or more registers may be combined at a single logical address.

TABLE 16 GS9060 INTERNAL REGISTERS

ADDRESS	REGISTER NAME	SEE SECTION
00h	IOPROC_DISABLE	Section 3.10.6
01h	ERROR_STATUS	Section 3.10.5
03h	EDH_FLAG	Section 3.10.7
04h	VIDEO_STANDARD	Section 3.10.4
05h - 09h	ANC_TYPE	Section 3.10.2.1
0Ch - 0Dh	VIDEO_FORMAT	Section 3.10.3
0Eh - 11h	RASTER_STRUCTURE	Section 3.10.4
12h - 19h	EDH_CALC_RANGES	Section 3.10.5.2
1Ah	ERROR_MASK	Section 3.10.5

3.13 JTAG

When the JTAG/$\overline{\text{HOST}}$ input pin of the GS9060 is set HIGH, the host interface port will be configured for JTAG test operation. In this mode, pins 27 through 30 become TMS, TDO, TDI, and TCK. In addition, the $\overline{\text{RESET\_TRST}}$ pin will operate as the test reset pin.

Boundary scan testing using the JTAG interface will be enabled in this mode.

There are two methods in which JTAG can be used on the GS9060:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly; or

2. Under control of the host for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 19.
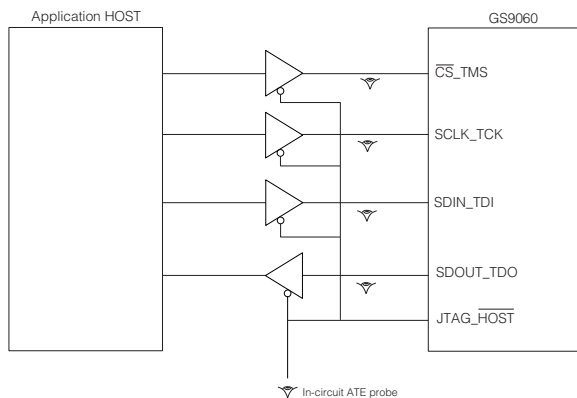

Figure 19   In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the host may still cntrol the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 20.

Figure 20   System JTAG

Please contact your Gennum representative to obtain the BSDL model for the GS9060.

3.14 DEVICE POWER UP

Because the GS9060 is designed to operate in a multi-volt environment, any power up sequence is allowed. The charge pump, phase detector, core logic, serial digital input/output buffers and digital I/O buffers should all be powered up within 1ms of one another.

Device pins may also be driven prior to power up without causing damage.

To ensure that all internal registers are cleared upon power-up, the application layer must hold the $\overline{\text{RESET\_TRST}}$ signal LOW for a minimum of 1ms after the core power supply has reached the minimum level specified in the DC Electrical Characteristics Table (see Section 2.2). See Figure 21.

3.15 DEVICE RESET

In order to initialize all internal operating conditions to their default states the application layer must hold the $\overline{\text{RESET\_TRST}}$ signal LOW for a minimum of t_{reset} = 1ms.

When held in reset, all device outputs will be driven to a high-impedance state.

Figure 21   Reset Pulse

4. APPLICATION REFERENCE DESIGN

4.1 TYPICAL APPLICATION CIRCUIT (PART A)

4.2 TYPICAL APPLICATION CIRCUIT (PART B)

5. REFERENCES & RELEVANT STANDARDS

SMPTE 125M   Component video signal 4:2:2 – bit parallel interface

SMPTE 291M   Ancillary Data Packet and Space Formatting
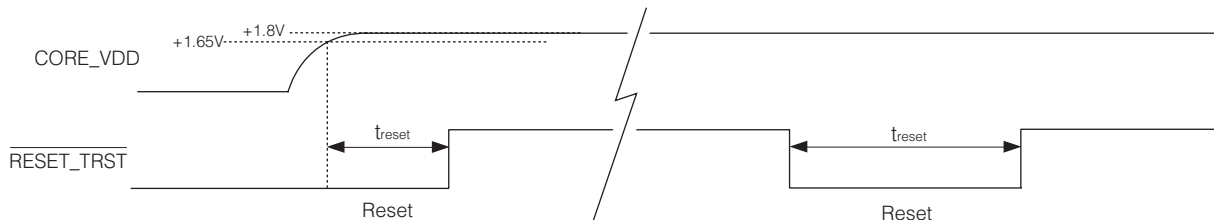
SMPTE 293M   720 x 483 active line at 59.94 Hz progressive scan production – digital representation

SMPTE 352M   Video Payload Identification for Digital Television Interfaces

SMPTE RP165   Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television

SMPTE RP168   Definition of Vertical Interval Switching Point for Synchronous Video Switching

6. PACKAGE & ORDERING INFORMATION

6.1 PACKAGE DIMENSIONS

Table X

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A$_1$	0.05	—	0.15	0.002	—	0.006
A$_2$	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D$_1$	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E$_1$	14.00 BSC.			0.551 BSC.		
R$_2$	0.08	—	0.20	0.003	—	0.008
R$_1$	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ$_1$	0°	—	—	0°	—	—
θ$_2$	11°	12°	13°	11°	12°	13°
θ$_3$	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L$_1$	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

CONTROL DIMENSIONS ARE IN MILLIMETERS.

Table Y

SYMBOL	80L					
	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
b	0.22	0.30	0.38	0.009	0.012	0.015
e	0.65 BSC			0.026 BSC		
D2	12.35			0.486		
E2	12.35			0.486		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.13			0.005		

NOTES:
Diagram shown is representative only. Table X is fixed for all pin sizes, and Table Y is specific to the 80-pin package.

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.

6.2 ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE
GS9060-CF	80-pin LQFP	0°C to 70°C

7. REVISION HISTORY

VERSION	ECR	DATE	CHANGES AND/OR MODIFICATIONS
A	120602	July 2002	New Document
B	126379	August 2002	Update AC/DC parameters. Correct pin descriptions. Add reflow profile. Insert I/O diagrams. Add JTAG information.
C	127430	November 2002	Change typical application circuit.
0	130131	July 2003	Upgrade to preliminary data sheet. Reformat detailed description and expand information. AC/DC parameters updated. Reset Operation clarified. Edit pin descriptions. Correct register addresses.

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION