ST-NXP Wireless

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- **Company name - Philips Semiconductors** is replaced with **ST-NXP Wireless**.

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- **Web site** - http://www.semiconductors.philips.com is replaced with http://www.stnwireless.com

- **Contact information** - the list of sales offices previously obtained by sending an email to sales.addresses@www.semiconductors.philips.com, is now found at http://www.stnwireless.com under Contacts.

If you have any questions related to the document, please contact our nearest sales office. Thank you for your cooperation and understanding.

ST-NXP Wireless

ISP1109

Universal Serial Bus transceiver with carkit support

Rev. 01 — 14 July 2005 Product data sheet

1. General description

The ISP1109 is a Universal Serial Bus (USB) transceiver device that supports *CEA–936–A, Mini-USB Analog Carkit Interface*. It is fully compliant with *Universal Serial Bus Specification Rev. 2.0*. The ISP1109 can transmit and receive serial data at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates.

The ISP1109 is available in HVQFN32 package.

2. Features

- Fully complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports *CEA–936–A, Mini-USB Analog Carkit Interface*
- Can transmit and receive serial data at full-speed (12 Mbit/s) and low-speed (1.5 Mbit/s) data rates
- Supports Serial Parallel Interface (SPI) (up to 26 MHz) and I^{2}C-bus (up to 400 kHz) serial interface to access control and status registers
- Supports Universal Asynchronous Receiver-Transmitter (UART) pass-through on the DP and DM lines
- Built-in analog switches to support analog audio signals multiplexed on the DP and DM lines
- Supports On-The-Go (OTG) Session Request Protocol (SRP)
- Supports Power-down mode, in which the whole chip consumes less than 20 µA power current
- 3.0 V to 5.25 V power supply input range (V_{CC})
- Supports wide range digital interfacing I/O voltage ($V_{CC(I/O)}$) of 1.65 V to 3.6 V
- ±12 kV ESD protection at pins DP, DM, ID, V_{BUS}, V_{CC}, GNDA and GNDD
- Supports charger current switching (ISET) detection
- Full industrial grade operation from –40 °C to +85 °C
- Available in a small HVQFN32 (5 x 5 mm^2) halogen-free and lead-free package.

3. Applications

- Mobile phones.

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4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1109BS	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm	SOT617-1

5. Block diagram

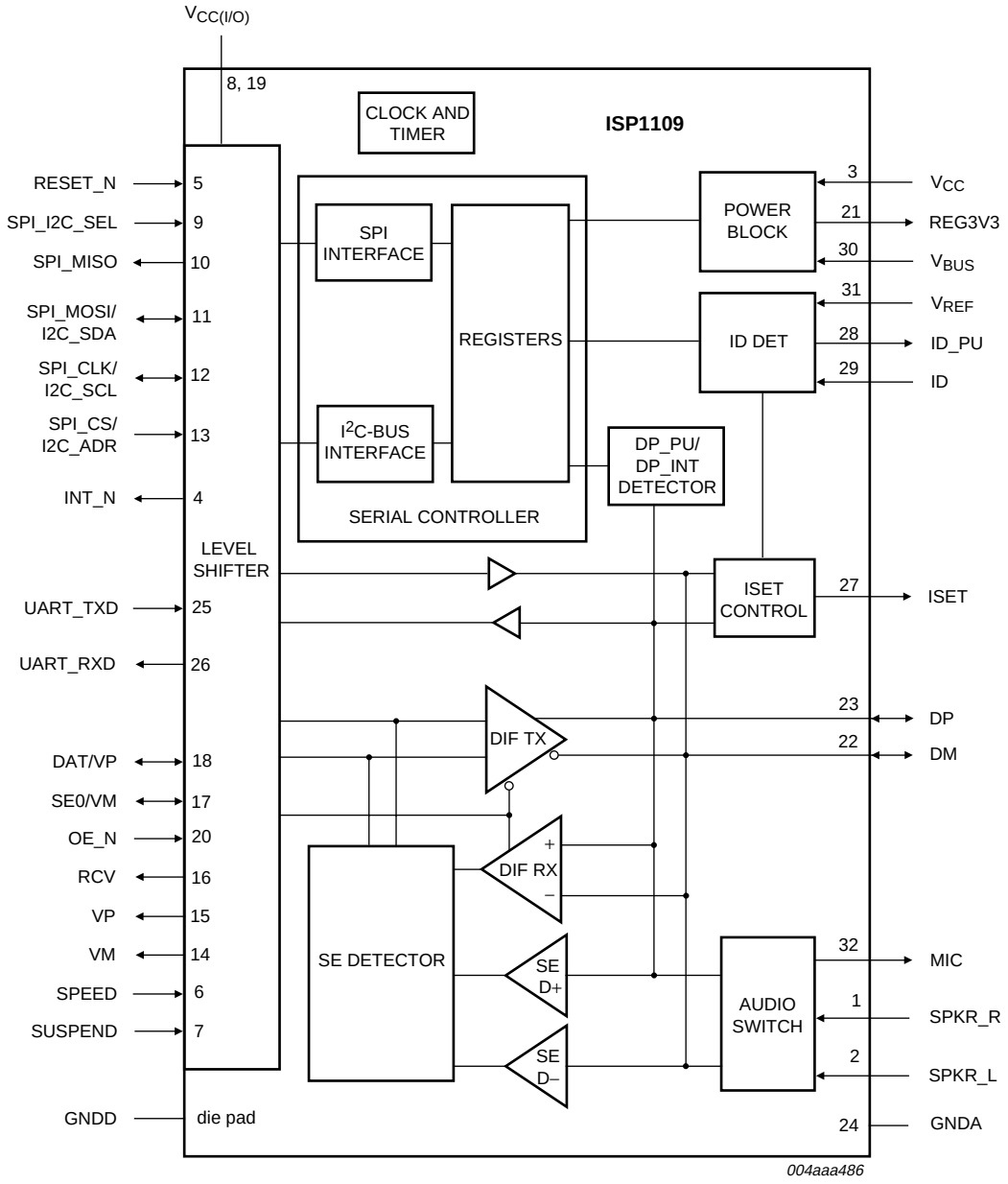


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

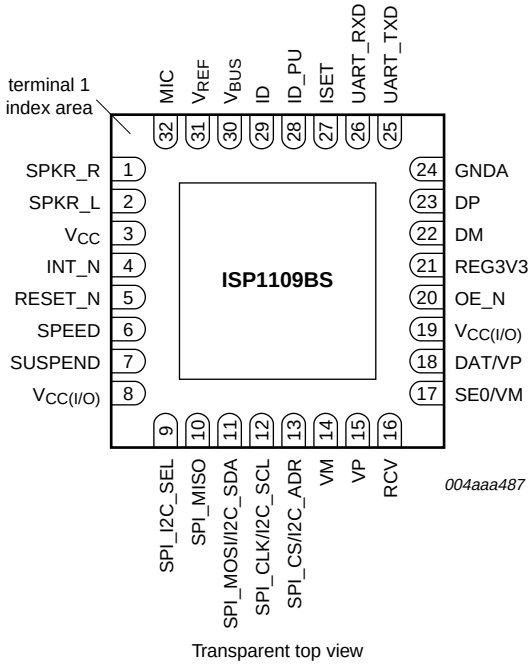


Fig 2. Pin configuration HVQFN32; top view.

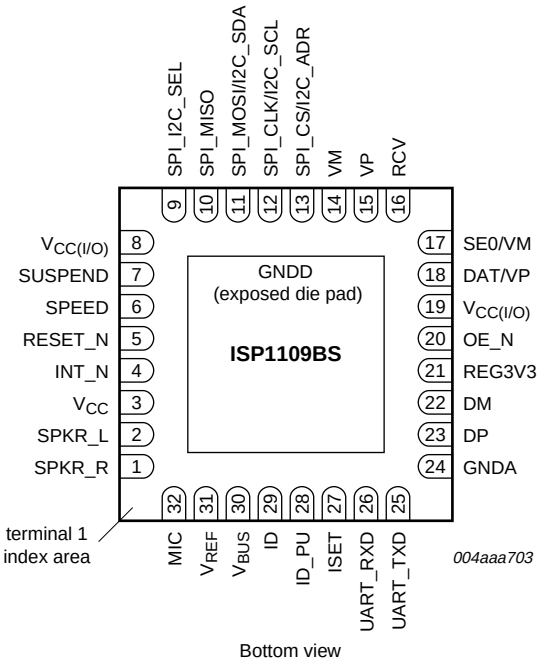


Fig 3. Pin configuration HVQFN32; bottom view.

6.2 Pin description

Table 2: Pin description

Symbol [1] [2]	Pin	Type [3]	Reset state	Description
SPKR_R	1	AI	-	analog audio input signal for the right speaker channel
SPKR_L	2	AI	-	analog audio input signal for the left speaker channel
V_{CC}	3	P	-	supply voltage; operates when $3.0\ V < V_{CC} < 5.25\ V$
INT_N	4	OD	high-Z	interrupt output; active LOW; connect to $V_{CC(I/O)}$ through a 3.3 kΩ resistor open-drain output
RESET_N	5	I	-	asynchronous reset input, active LOW input
SPEED	6	I	-	speed selection input for the USB transceiver: • LOW: USB low-speed • HIGH: USB full-speed. when not in use, connect to $V_{CC(I/O)}$ through a 10 kΩ resistor input
SUSPEND	7	I	-	suspend selection input for the USB transceiver: • LOW: normal operation • HIGH: suspend mode. when not in use, connect to ground through a 10 kΩ resistor input
$V_{CC(I/O)}$	8	P	-	supply voltage for I/O interface logic signals (1.65 V to 3.6 V)
SPI_I2C_SEL	9	I	-	selection of SPI or I^2C-bus serial interface to access internal registers: • LOW: SPI slave interface is selected • HIGH: I^2C-bus slave interface is selected. The I^2C-bus device address is 010 110Xb; here X is determined by pin 13 (I2C_ADR). input
SPI_MISO	10	O	-	SPI slave data output; leave this pin open when I^2C-bus is selected push-pull output
SPI_MOSI/ I2C_SDA	11	I/OD	high-Z	**SPI_MOSI input —** SPI slave data input **I2C_SDA input and output —** serial I^2C-bus data; when used as an I^2C-bus data, the pad is open-drain; connect to $V_{CC(I/O)}$ through a 3.3 kΩ resistor.

Table 2: Pin description...*continued*

Symbol [1] [2]	Pin	Type [3]	Reset state	Description
SPI_CLK/ I2C_SCL	12	I/OD	high-Z	**SPI_CLK input —** SPI clock input **I2C_SCL input and output —** serial I^2C-bus clock; when used as an I^2C-bus clock, the pad is open-drain; connect to $V_{CC(I/O)}$ through a 3.3 kΩ resistor.
SPI_CS/ I2C_ADR	13	I	-	**SPI_CS input —** SPI chip select input **I2C_ADR input —** LSB address offset of the I^2C-bus slave address. input
VM	14	O	-	single-ended DM receiver output; leave this pin open when not in use push-pull output
VP	15	O	-	single-ended DP receiver output; leave this pin open when not in use push-pull output
RCV	16	O	0	differential receiver output; leave this pin open when not in use push-pull output
SE0/VM	17	I/O	high-Z	**SE0 input and output —** SE0 functions in DAT_SE0 USB mode **VM input and output —** VM functions in VP_VM USB mode. bidirectional pad
DAT/VP	18	I/O	high-Z	**DAT input and output —** DAT functions in DAT_SE0 USB mode **VP input and output —** VP functions in VP_VM USB mode. bidirectional pad
$V_{CC(I/O)}$	19	P	-	supply voltage for the I/O interface logic signals (1.65 V to 3.6 V)
OE_N	20	I	-	enable differential transmitter input input
REG3V3	21	P	-	regulated output voltage 3.3 V; a 0.1 µF external capacitor is required
DM	22	AI/O	high-Z	this pin can be programmed as: • USB D– (data minus pin) • transparent UART RxD or • transparent audio SPKR_L.
DP	23	AI/O	high-Z	this pin can be programmed as: • USB D+ (data plus pin) • transparent UART TxD or • transparent audio SPKR_R or MIC.
GNDA	24	P	-	analog ground

Table 2: Pin description *…continued*

Symbol [1] [2]	Pin	Type [3]	Reset state	Description
UART_TXD	25	I	-	connect to TxD of the UART controller; when not in use, connect to $V_{CC(I/O)}$ through a 10 kΩ resistor input
UART_RXD	26	O	-	connect to RxD of the UART controller; leave this pin open when not in use push-pull output
ISET	27	O [4]	-	output indicating detection of the carkit, charger or factory mode to enable high current mode of the phone charger; leave this pin open when not in use push-pull output
ID_PU	28	AI	-	an external resistor is connected between the ID and ID_PU pins
ID	29	AI	-	identification detector input of the USB mini connector
V_{BUS}	30	AI	-	V_{BUS} line input supply voltage of the USB connector [5]
V_{REF}	31	P	-	supply voltage for audio circuits; 2.775 V ± 0.1 V
MIC	32	AO	-	audio output signal for the microphone channel
GNDD	exposed die pad	P	-	digital ground

[1] Symbol names ending with underscore N—for example, NAME_N—indicate active LOW signals.

[2] Use a decoupling capacitor of 0.1 µF on all $V_{CC(I/O)}$, V_{REF} and V_{CC} pins.

[3] I = input; O = output; I/O = digital input/output; OD = open-drain output; AI/O = analog input/output; P = power or ground.

[4] The ISET pin is powered by REG3V3. All other digital pins are powered by $V_{CC(I/O)}$.

[5] For the decoupling capacitor requirement, refer to Table 7-7 of *Universal Serial Bus Specification Rev. 2.0*.

7. Functional description

7.1 Serial controller

The serial controller includes the following functions:

- Serial Controller interface (SPI or I^2C-bus)
- Device Identification registers
- Control registers
- Interrupt registers
- Interrupt generator.

The serial controller acts as an SPI slave or I^2C-bus slave.

All the registers are the same as that in SPI or I^2C-bus mode. In I^2C-bus mode, the registers are accessed in 8-bit width (bits 0 to 7) for each address. In SPI mode, there are 25 bits for each address, only bits 0 to 7 are useful while bits 8 to 24 are don't cares.

At hardware reset including power-on reset, the level on pin SPI_I2C_SEL will determine whether the SPI or I^2C-bus interface is active. If SPI_I2C_SEL = LOW, the SPI interface is selected. If SPI_I2C_SEL = HIGH, the I^2C-bus interface is selected.

7.2 V_{BUS} detector

The V_{BUS} detector provides voltage level detection on V_{BUS}. If V_{BUS} is above the V_{BUS} session valid comparator threshold voltage ($V_{th(svc)}$), logic 1 will be stored in bit VBUS_DET of the Interrupt Source register. If V_{BUS} is below $V_{th(svc)}$, logic 0 will be stored.

7.3 ID detector

In normal power mode, that is, when both V_{CC} and $V_{CC(I/O)}$ are present, the ID detector senses the condition of the ID line and can differentiate between the following three conditions:

- ID pin is floating (bit ID_FLOAT = 1)
- ID pin is shorted to ground (bit ID_GND = 1)
- ID pin is connected to ground through resistor $R_{DN(ID)}$ (bits ID_FLOAT and ID_GND are logic 0).

The recommended procedure to detect the status of ID using software is:

1. When nothing is connected, ID is in the ID_FLOAT state. Enable the ID_FLOAT interrupt (falling edge).
2. If an interrupt occurs, read the Interrupt Latch register. If ID changes, bit ID_FLOAT is set.
3. The software waits for sometime, for example: 100 ms, to allow mechanical debounce.
4. The software reads the Interrupt Source register, and checks bits ID_FLOAT and ID_GND.

The ID detector has a switch that can be used to ground pin ID. This switch is controlled by bit ID_PULLDN of the Resistor Control register, and bits PH_ID_INT and PH_ID_ACK of the Audio Control register. See Table 3.

Table 3: ID pull-down control

ID_PULLDN	PH_ID_ACK	PH_ID_INT	Switch between ID and GND
0	0	0	off
0	0	1	on for time $t_{Wint(ID)}$ then off; bit PH_ID_INT auto-clears to 0
0	1	0	wait for time $t_{int(ID)}$, turn on the switch for $t_{Wint(ID)}$ then off; bit PH_ID_ACK auto-clears to 0
0	1	1	not defined
1	X	X	on

The ID detector also has a switch that is connected between the ID_PU and V_{REF} pins. If the voltage on the ID pin is higher than the voltage on the V_{REF} pin, the switch will be turned off. Otherwise, the switch will remain on.

7.4 Pull-up and pull-down resistors

The DP pull-up resistor can be enabled or disabled (default enabled) using register bit DP_PULLUP, if V_{BUS} is above $V_{th(svc)}$. The pull-up resistance on pin DP ($R_{UP(DP)}$) must be enabled, if $V_{CC} > V_{th(ISET)}$ and $V_{BUS} > V_{th(svc)}$.

To support DP Session Request Protocol (SRP), it is required that a B-device can perform DP pulsing when V_{BUS} is below the session end threshold (0.2 V to 0.8 V). If register bit DP_SRP_EN is set, the DP pull-up resistor will be enabled irrespective of the status of V_{BUS}.

Table 4: DP pull-up resistor ($R_{UP(DP)}$) control

Bit		$V_{BUS} > V_{th(svc)}$	Pin		DP pull-up resistor (SW1)
DP_SRP_EN	DP_PULLUP		$V_{CC(I/O)}$ HIGH	RESET_N	
0	0	X	X	X	off
0	1	no	X	X	off
0	1	X	LOW	X	off
0	1	X	X	LOW	off
0	1	yes	HIGH	HIGH	on
1	X	X	X	HIGH	on

The pull-up resistor is context variable, as described in document *ECN_27%_Resistor*. The value of the pull-up resistor depends on the condition of the USB bus:

- When the bus is idle, the value of the resistor is 900 Ω to 1575 Ω (SW2 = on).
- When the bus is transmitting or receiving, the value of the resistor is 1425 Ω to 3090 Ω (SW2 = off).

DP also implements a weak pull-up resistor ($R_{weakUP(DP)}$) that is controlled by bit DP_WKPU_EN of the Resistor Control register; see Figure 4. $R_{weakUP(DP)}$ will be connected to the DP pin (SW3 = on), if bit DP_WKPU_EN = 1 and the voltage on V_{BUS} is greater than $V_{th(svc)}$.

The DP pull-down resistor ($R_{DN(DP)}$) is connected to the DP line, if bit DP_PULLDOWN in the Resistor Control register is set.

The DM pull-down resistor ($R_{DN(DM)}$) is connected to the DM line, if bit DM_PULLDOWN in the Resistor Control register is set.

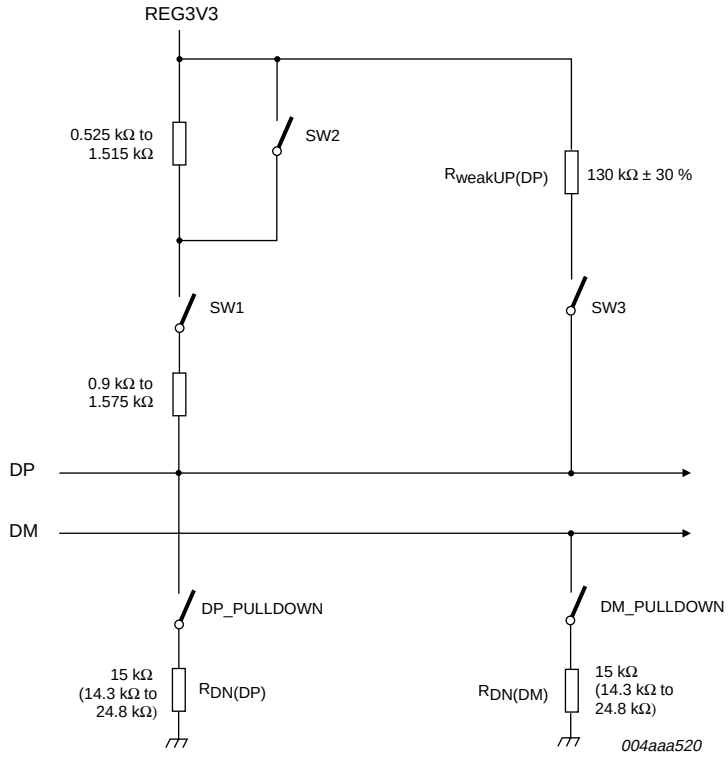


Fig 4. DP and DM pull-up and pull-down resistors.

7.5 Power block

The built-in DC-DC regulator conditions the input power supply (V_{CC}) for use in the core of the ISP1109.

When V_{CC} is greater than 3.6 V, the regulator will output 3.3 V ± 10 %. When V_{CC} is less than 3.6 V, the regulator will be bypassed and pin REG3V3 will be shorted to pin V_{CC}.

The output of the regulator can be monitored on pin REG3V3. A capacitor (0.1 µF) will be connected to pin REG3V3.

7.6 Carkit DP interrupt detector

The carkit DP interrupt detector is a comparator that detects the carkit interrupt signal on the DP line in analog audio mode. Bit DP_INT will be cleared (set to logic 0), if the voltage level on the DP line is below the carkit interrupt threshold $V_{thPH(DP)L}$ (0.4 V to 0.6 V).

The carkit interrupt detector is enabled in audio mode only (bit AUDIO_EN = 1).

7.7 Audio switches

The audio switches provide low impedance path for analog audio signals to be multiplexed on the DP and DM lines, or loopback between the MIC and SPKR lines.

There are five analog switches that are controlled by register bits. The impedance of the switches will be between 50 Ω and 150 Ω. Table 5 shows the relation between the control bits and the switches. Figure 5 shows the audio switches.

Table 5: Audio switch control

AUDIO_EN	AUDIO_MONO	S1	S2	S3
0	X	off	off	off
1	0	on	off	on
1	1	off	on	off

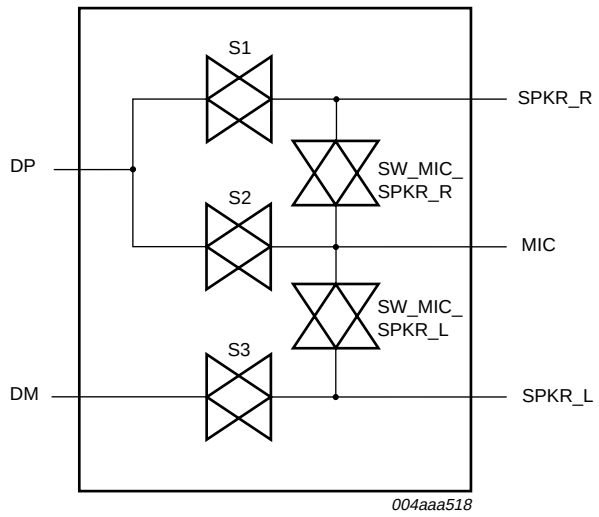


Fig 5. Audio switches.

7.8 ISET detector

The ISET detector will set the ISET pin HIGH when either of the following conditions is met:

- ID > $V_{th(ID\_FM)}$, V_{CC} > $V_{th(ISET)}$ and V_{BUS} > $V_{th(svc)}$
- DP and DM SE1 detected, V_{CC} > $V_{th(ISET)}$ and V_{BUS} > $V_{th(svc)}$.

The DP and DM SE1 detector will time the length of the SE1 condition. The timer value is programmable using register bit TMR_SE1. The timer ranges from 0 ms to 15 ms, with 1 ms interval.

The ID > $V_{th(ID\_FM)}$ detector, and the SE1 detector (with timer) requires bias current. In Power-down mode, the bias current is turned off to minimize current I_{CC}. The bias current needs to be enabled so that the ISET detector can function as described earlier.

- If the Power-down is because $V_{CC(I/O)}$ is disconnected, the bias will be enabled if the V_{BUS} voltage goes above the SESS_VLD threshold.

- If the Power-down is because of the setting of register bit PWR_DN in the Mode Control register, the bias will be enabled if the V_{BUS} voltage goes above the SESS_VLD threshold. Note: In this case, make sure bit SESS_VLD_IEH in the Interrupt Enable High register is set to logic 1 before the PWR_DN bit is set. The recommended sequences for software is:
  a. Set bit SESS_VLD_IEH to logic 1
  b. Set bit PWR_DN to logic 1
  c. Wait for interrupt from the ISP1109
  d. If INT_N is asserted, read the Interrupt Latch register
  e. If bit SESS_VLD_INT is logic 1, clear bit PWR_DN (Note: Software must clear bit PWR_DN within 5 ms from the time pin INT_N is asserted. For details, see Section 10).

Pin ISET will remain LOW when V_{CC} is below $V_{th(ISET)}$. Pin ISET can also be controlled by software through register bits. If bit ISET_DRV_EN is set to logic 1, the status of the ISET pin will be determined by bit ISET_STATE.

7.9 USB transceiver

7.9.1 Differential driver

The operation of the driver is described in Table 6.

Table 6: Transceiver driver operating setting

Pin		Pin or bit SUSPEND	Bit DAT_SE0	Differential driver
RESET_N [1]	OE_N			
HIGH	LOW	0	0	output value from DAT/VP to DP and SE0/VM to DM
HIGH	LOW	0	1	output value from DAT/VP to DP and DM, if SE0/VM is LOW; otherwise, drive both DP and DM LOW
HIGH	LOW	1	X	output value from DAT/VP to DP and DM
HIGH	HIGH	X	X	high-Z
LOW	X	X	X	high-Z

[1] Include the internal power-on-reset pulse (active HIGH).

Table 7 shows the behavior of the transmit operation in detail.

Table 7: USB functional mode: transmit operation

USB mode	Inputs		Outputs	
	DAT/VP	SE0/VM	DP	DM
DAT_SE0	LOW	LOW	LOW	HIGH
DAT_SE0	HIGH	LOW	HIGH	LOW
DAT_SE0	LOW	HIGH	LOW	LOW
DAT_SE0	HIGH	HIGH	LOW	LOW
VP_VM	LOW	LOW	LOW	LOW

Table 7: USB functional mode: transmit operation…*continued*

USB mode	Inputs		Outputs	
	DAT/VP	SE0/VM	DP	DM
VP_VM	HIGH	LOW	HIGH	LOW
VP_VM	LOW	HIGH	LOW	HIGH
VP_VM	HIGH	HIGH	HIGH	HIGH

7.9.2 Differential receiver

The operation of the differential receiver is described in Table 8.

Table 8: Differential receiver operation settings

Pin or bit SUSPEND	Pin OE_N	Bit		Differential receiver
		DAT_SE0	BI_DI	
0	HIGH	1	0	output differential value from DP and DM to RCV
0	HIGH	1	1	output differential value from DP and DM to DAT/VP and RCV
0	HIGH	0	X	output differential value from DP and DM to RCV
X	LOW	X	X	0
1	X	X	X	X

The detailed behavior of the receive transceiver operation is shown in Table 9.

Table 9: USB functional mode: receive operation

USB mode	Pin or bit SUSPEND	Inputs		Outputs		
		DP	DM	DAT/VP [1]	SE0/VM [1]	RCV
DAT_SE0	0	LOW	LOW	RCV	HIGH	last value of RCV
DAT_SE0	0	HIGH	LOW	HIGH	LOW	HIGH
DAT_SE0	0	LOW	HIGH	LOW	LOW	LOW
DAT_SE0	0	HIGH	HIGH	RCV	LOW	last value of RCV
DAT_SE0	1	LOW	LOW	LOW	HIGH	X
DAT_SE0	1	HIGH	LOW	HIGH	LOW	X
DAT_SE0	1	LOW	HIGH	LOW	LOW	X
DAT_SE0	1	HIGH	HIGH	HIGH	LOW	X
VP_VM	0	LOW	LOW	LOW	LOW	last value of RCV
VP_VM	0	HIGH	LOW	HIGH	LOW	HIGH
VP_VM	0	LOW	HIGH	LOW	HIGH	LOW
VP_VM	0	HIGH	HIGH	HIGH	HIGH	last value of RCV
VP_VM	1	LOW	LOW	LOW	LOW	X
VP_VM	1	HIGH	LOW	HIGH	LOW	X
VP_VM	1	LOW	HIGH	LOW	HIGH	X
VP_VM	1	HIGH	HIGH	HIGH	HIGH	X

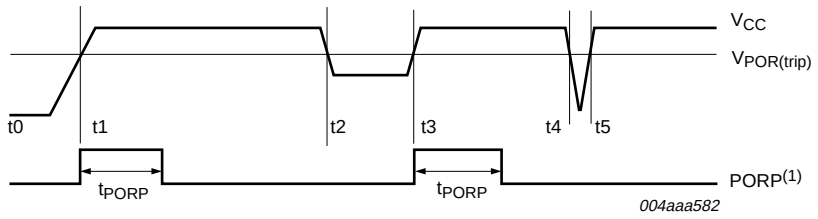
[1] Applies only to bidirectional mode (bit BI_DI = 1). For unidirectional mode (bit BI_DI = 0), DAT/VP and SE0/VM are input-only pins.

7.10 Power-On Reset (POR)

When $V_{CC(I/O)}$ is directly connected to the RESET_N pin, the internal POR pulse width (t_{PORP}) will be typically 800 ns. The pulse is started when V_{CC} rises above $V_{POR(trip)}$ (1.5 V to 2.5 V).

To give a better view of the functionality, Figure 6 shows a possible curve of V_{CC} with dips at t2 to t3 and t4 to t5. If the dip at t4 to t5 is too short (that is, < 11 µs), the internal POR pulse will not react and will remain LOW. The internal POR starts with a 1 at t0. At t1, the detector will see the passing of the trip level and a delay element will add another t_{PORP} before it drops to 0.

The internal POR pulse will be generated whenever V_{CC} drops below $V_{POR(trip)}$ for more than 11 µs.



(1) PORP = Power-On Reset Pulse.

Fig 6. Internal power-on reset timing.

8. Modes of operation

The ISP1109 supports four types of modes:

- Power modes
- Serial control modes
- USB modes
- Transparent modes.

8.1 Power modes

8.1.1 Normal mode

In this mode, both V_{CC} and $V_{CC(I/O)}$ are connected and their voltage levels are within the operation range ($V_{CC} \geq 3.0$ V, $V_{CC(I/O)} \geq 1.65$ V, $V_{CC(I/O)} \leq V_{CC}$).

There are three levels of power saving schemes in the ISP1109:

- Active power mode: Power is on; all circuits are active.
- USB suspend mode: To reduce power consumption, the USB differential receiver is powered off.
- Power-down mode: Set by writing logic 1 to bit PWR_DN of the Mode Control 2 register. The clock generator and all biasing circuits are turned off to reduce power consumption to the minimum possible; typically I_{CC} is less than 20 μA. For details on waking up the clock, see Section 10.

8.1.2 Disable mode

In disable mode, $V_{CC(I/O)}$ is cut-off and V_{CC} is powered. In this mode, the ISP1109 is in Power-down state, if V_{BUS} is below SESS_VLD threshold (0.8 V to 2.0 V).

When V_{CC} is below threshold $V_{th(ISET)}$, pin ISET will remain at the LOW level.

When $V_{BUS} > V_{th(svc)}$ and V_{CC} rises above $V_{th(ISET)}$, the ISP1109 will output HIGH on pin ISET, if any of the following conditions is detected:

- Voltage on pin ID is greater than $V_{th(ID\_FM)}$
- DP and DM are single-ended one (SE1).

If the preceding condition is detected, pin ISET will be asserted within 1.5 ms when V_{CC} rises above $V_{th(ISET)}$.

The USB differential driver will be set in three-state as long as $V_{CC(I/O)}$ is lost. The DP pull-up resistor ($R_{UP(DP)}$) will be disconnected from the DP line. The DP weak pull-up resistor ($R_{weakUP(DP)}$) will be connected if the V_{BUS} voltage is above $V_{th(svc)}$.

8.1.3 Isolate mode

In isolate mode, V_{CC} is cut-off and $V_{CC(I/O)}$ is powered. In this mode, the ISP1109 will drive stable level to all digital output pins, and all bidirectional digital pins will be set in three-state.

Table 10 shows a summary of power modes.

Table 10: ISP1109 power modes: summary

V_{CC}	$V_{CC(I/O)}$	V_{BUS}	PWR_DN (bit)	I_{CC} < 20 μA	ISET (pin)	Comment
off	off	X	X	yes	high-Z	power off
off	on	X	X	yes	high-Z	isolate mode
on	off	$<V_{th(svc)}$	X	yes	LOW	disable mode (Power-down)
on	off	$>V_{th(svc)}$	X	no	LOW or HIGH	disable mode (ISET operation)
on	on	X	0	no	LOW or HIGH	normal mode (full operation)
on	on	X	1	yes	LOW or HIGH	normal mode (Power-down)

Table 11 shows the pin states in disable or isolate mode.

Table 11: ISP1109 pin states in disable or isolate mode

Pin name	Disable mode (V_{CC} = on, $V_{CC(I/O)}$ = off)	Isolate mode (V_{CC} = off, $V_{CC(I/O)}$ = on)
V_{CC}, REG3V3	powered	not present
$V_{CC(I/O)}$, V_{REF}	not present	powered
ISET	drive HIGH or LOW	high-Z
DP	high-Z	high-Z
DM	15 kΩ pull-down enabled	high-Z
RCV	high-Z	drive LOW
VP, VM, SPI_MISO, UART_RXD	high-Z	drive HIGH
RESET_N, SPEED, SUSPEND, SPI_I2C_SEL, SPI_MOSI/I2C_SDA, SPI_CLK/I2C_CLK, SPI_CS/I2C_ADR, SE0/VM, DAT/VP, UART_TXD, INT_N	high-Z	high-Z
MIC, SPKR_R, SPKR_L, ID, V_{BUS}	high-Z	high-Z
ID_PU	V_{REF} (high-Z, if voltage on pin ID > V_{REF})	V_{REF} (high-Z, if voltage on pin ID > V_{REF})

8.2 Serial control modes

8.2.1 I²C-bus mode

In I²C-bus mode, an external System-on-a-Chip (SoC) directly communicates with the serial controller through the SCL and SDA lines. The serial controller has a built-in I²C-bus slave function. An external I²C-bus master can access the internal registers of the ISP1109 through the I²C-bus interface.

The supported I²C-bus bit rate is up to 400 kbit/s. The I²C-bus device address is 010 110Xb, where X is determined by pin 13.

8.2.2 SPI mode

In this mode, an external SoC directly communicates with the serial controller through the SPI interface: SPI_MOSI, SPI_MISO, SPI_CLK, SPI_CS. The serial controller has a built-in SPI slave function. An external SPI master can access the internal registers of the ISP1109 through the SPI interface. The maximum SPI clock rate is 26 MHz.

8.3 USB modes

The four USB modes of the ISP1109 are:

- VP_VM unidirectional mode
- VP_VM bidirectional mode
- DAT_SE0 unidirectional mode (default)
- DAT_SE0 bidirectional mode.

In VP_VM USB mode, pin DAT/VP is used for the VP function, pin SE0/VM is used for the VM function, and pin RCV is used for the RCV function.

In DAT_SE0 USB mode, pin DAT/VP is used for the DAT function, pin SE0/VM is used for the SE0 function, and pin RCV is not used.

In unidirectional mode, pins DAT/VP and SE0/VM are always input. In bidirectional mode, the direction of these signals depends on input OE_N.

Table 12 specifies the functionality of the device during the four USB modes.

Table 12: USB functional modes: I/O values

USB mode [1]		Bit		Pin					
		DAT_SE0	BI_DI	OE_N	DAT/VP	SE0/VM	VP	VM	RCV
VP_VM	unidirectional	0	0	X	TxD+ [2]	TxD– [2]	RxD+ [6]	RxD– [6]	RxD [6]
	bidirectional		1	LOW	TxD+ [2]	TxD– [2]			
				HIGH	RxD+ [3]	RxD– [3]			
DAT_SE0	unidirectional	1	0	X	TxD [4]	FSE0 [5]			
	bidirectional		1	LOW	TxD [4]	FSE0 [5]			
				HIGH	RxD [6]	RSE0 [7]			

[1] Some of the modes and signals are provided to achieve backward compatibility with IP cores.

[2] TxD+ and TxD– are single-ended inputs to drive the DP and DM outputs, respectively, in single-ended mode.

[3] RxD+ and RxD– are the outputs of the single-ended receivers connected to DP and DM, respectively.

[4] TxD is the input to drive DP and DM in DAT_SE0 mode.

[5] FSE0 is to force an SE0 on the DP and DM lines in DAT_SE0 mode.

[6] RxD is the output of the differential receiver.

[7] RSE0 is an output, indicating that an SE0 is received on the DP and DM lines.

8.4 Transparent modes

8.4.1 Transparent UART mode

When in transparent UART mode, an SoC (with the UART controller) communicates through the ISP1109 to another UART device that is connected to its DP and DM lines. The ISP1109 operates as logic level translator between the following pins, depending on the setting of register bit UART_PIN_SEL.

- If UART_PIN_SEL = 0 (default):
  - For the TxD signal: From UART_TXD ($V_{CC(I/O)}$ level) to DM (REG3V3 level)
  - For the RxD signal: From DP (REG3V3 level) to UART_RXD (REG3V3 level).

- If UART_PIN_SEL = 1:
  - For the TxD signal: From SE0/VM ($V_{CC(I/O)}$ level) to DM (REG3V3 level)
  - For the RxD signal: From DP (REG3V3 level) to DAT/VP (REG3V3 level).

The ISP1109 is in transparent UART mode, if bit UART_EN of the Mode Control 1 register is set.

8.4.2 Transparent audio mode

In transparent audio mode, the ISP1109 will disable its DP and DM driver. The carkit interrupt detector is enabled. The built-in analog switches will be tuned based on the selection of carkit audio mode:

- Stereo mode: SPKR_L on DM and SPKR_R on DP
- Mono and MIC mode: SPKR_L on DM and MIC on DP.

The ISP1109 is in transparent audio mode, if bit UART_EN of the Mode Control 1 register is cleared, and bit AUDIO_EN of the Audio Control register is set.

8.4.3 Transparent general-purpose buffer mode

In transparent general-purpose buffer mode, the DAT/VP and SE0/VM pins are connected to the DP and DM pins, respectively. Using bits TRANSP_BDIR1 and TRANSP_BDIR0 of the Mode Control 2 register as specified in Table 14, you can control the direction of data transfer. The ISP1109 is in transparent general-purpose buffer mode if bit UART_EN = 0, bit AUDIO_EN = 0, and bit TRANSP_EN = 1.

Table 13 provides a summary of the device operating modes.

Table 13: Summary of device operating modes

Mode	Bit					Description
	UART_EN	UART_PIN_SEL	AUDIO_EN	AUDIO_MONO	TRANSP_EN	
USB mode	0	X	0	X	0	USB ATX enabled
Transparent general purpose buffer mode	0	X	0	X	1	USB ATX disabled. SE0/VM ↔ DM DAT/VP ↔ DP See Table 14
Transparent Audio mode (stereo)	0	X	1	0	X	USB ATX disabled. SPKR_L → DM SPKR_R → DP
Transparent Audio mode (mono)	0	X	1	1	X	USB ATX disabled. SPKR_L → DM MIC ← DP
Transparent UART mode (mode 1)	1	0	X	X	X	USB ATX disabled. UART_TXD → DM UART_RXD ← DP
Transparent UART mode (mode 2)	1	1	X	X	X	USB ATX disabled. SE0/VM → DM DAT/VP ← DP

Table 14: Transparent general-purpose buffer mode

Bit TRANSP_BDIR[1:0]	Direction of the data flow	
00	DAT/VP → DP	SE0/VM → DM
01	DAT/VP → DP	SE0/VM ← DM
10	DAT/VP ← DP	SE0/VM → DM
11	DAT/VP ← DP	SE0/VM ← DM

9. Serial controller

9.1 Register map

Table 15 provides an overview of the serial controller registers.

Table 15: Register overview

Register	Width (bits)	Access	Memory address [1]	Functionality	Reference
Vendor ID	16	R	00h to 01h	device identification registers	Section 9.1.1 on page 20
Product ID	16	R	02h to 03h		
Version ID	16	R	14h to 15h		
Mode Control 1	8	R/S/C	**Set** — 04h **Clear** — 05h	control registers	Section 9.1.2 on page 21
Mode Control 2	8	R/S/C	**Set** — 12h **Clear** — 13h		
Audio Control	8	R/S/C	**Set** — 16h **Clear** — 17h		
Timer Control	8	R/S/C	**Set** — 18h **Clear** — 19h		
Resistor Control	8	R/S/C	**Set** — 06h **Clear** — 07h		
Interrupt Source	8	R	**Read** — 08h	interrupt registers	Section 9.1.3 on page 24
Interrupt Latch	8	R/S/C	**Set** — 0Ah **Clear** — 0Bh		
Interrupt Enable Low	8	R/S/C	**Set** — 0Ch **Clear** — 0Dh		
Interrupt Enable High	8	R/S/C	**Set** — 0Eh **Clear** — 0Fh		

[1] The R/S/C access type represents a field that can be read, set or cleared (set to 0). A register can be read from either of the indicated addresses—set or clear. Writing logic 1 to the set address causes the associated bit to be set. Writing logic 1 to the clear address causes the associated bit to be cleared. Writing logic 0 to an address has no effect.

9.1.1 Device identification registers

9.1.1.1 Vendor ID register

Table 16 provides the bit description of the Vendor ID register.

Table 16: VENDORID - Vendor ID register (address 00h to 01h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	VENDORID[15:0]	R	04CCh*	Philips Semiconductors' Vendor ID

9.1.1.2 Product ID register

The bit description of the Product ID register is given in Table 17.

Table 17: PRODUCTID - Product ID register (address 02h to 03h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	PRODUCTID[15:0]	R	1109h*	Product ID of the ISP1109

9.1.1.3 Version ID register

Table 18 shows the bit description of the register.

Table 18: VERSIONID - Version ID register (address 14h to 15h) bit description

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15 to 0	VERSIONID[15:0]	R	0110h*	Version number of the ISP1109

9.1.2 Control registers

9.1.2.1 Mode Control 1 register

The bit allocation of the Mode Control 1 register is given in Table 19.

Table 19: Mode Control 1 register (address Set = 04h, Clear = 05h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UART_PIN_SEL	UART_EN	reserved		TRANSP_EN	DAT_SE0	SUSPEND	SPEED
Reset	0	0	0	0	0	1	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 20: Mode Control 1 register (address Set = 04h, Clear = 05h) bit description

Bit	Symbol	Description
7	UART_PIN_SEL	Select UART interface pins for transparent UART mode. **0 —** UART_TXD → DM; UART_RXD ← DP **1 —** DAT/VP → DP; SE0/VM ← DM.
6	UART_EN	When asserted, the ATX is in transparent UART mode. **0 —** UART mode is not enabled **1 —** UART mode is enabled.
5 to 4	-	reserved; cleared (set to 0)
3	TRANSP_EN	When set, the ATX is in transparent mode.
2	DAT_SE0	**0 —** VP_VM mode **1 —** DAT_SE0 mode.
1	SUSPEND	Sets the transceiver in low power mode. **0 —** Active power mode **1 —** Low power mode (differential receiver is disabled if SPEED = 1).
0	SPEED	Set the rise time and the fall time of the transmit driver in USB modes. **0 —** Low-speed mode **1 —** Full-speed mode.

9.1.2.2 Mode Control 2 register

For the bit allocation of this register, see Table 21.

Table 21: Mode Control 2 register (address Set = 12h, Clear = 13h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		AUDIO_EN	TRANSP_BDIR1	TRANSP_BDIR0	BI_DI	SPD_SUSP_CTRL	PWR_DN
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 22: Mode Control 2 register (address Set = 12h, Clear = 13h) bit description

Bit	Symbol	Description
7 to 6	-	reserved; cleared (set to 0)
5	AUDIO_EN	Enables the ISP1109 in carkit audio mode. **0 —** Audio disable: analog switches are turned off, DP_INT detector is turned off, and single-ended receivers are turned on **1 —** Audio enable: analog switches are turned on, DP_INT detector is turned on, and single-ended receivers are turned off.
4 to 3	TRANSP_BDIR[1:0]	Controls the direction of data transfer in transparent general-purpose buffer mode; see Table 14
2	BI_DI	**0 —** Direction of DAT/VP and SE0/VM are fixed (only transmit) **1 —** Direction of DAT/VP and SE0/VM are controlled by OE_N.
1	SPD_SUSP_CTRL	Controls speed and suspend in USB modes: **0 —** Controlled by pins SPEED and SUSPEND **1 —** Controlled by the Mode Control 1 register bits SPEED and SUSPEND.
0	PWR_DN	Set to Power-down mode; activities on pin SPI_CLK/I2C_SCL or the interrupt event can wake-up the chip; see Section 9

9.1.2.3 Audio Control register

Table 23 provides bit allocation of the register.

Table 23: Audio Control register (address Set = 16h, Clear = 17h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	PH_ID_ACK	PH_ID_INT	DP_SRP_EN	ISET_STATE	ISET_DRV_EN	SW_MIC_SPKR_R	SW_MIC_SPKR_L	AUDIO_MONO
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 24: Audio Control register (address Set = 16h, Clear = 17h) bit description

Bit	Symbol	Description
7	PH_ID_ACK	If set, wait for time $t_{int(ID)}$, turn on the ID pull-down switch for $t_{Wint(ID)}$, then turn off. Bit PH_ID_ACK auto-clears to 0. See Table 6.
6	PH_ID_INT	If set, turn on the ID pull-down switch for time $t_{Wint(ID)}$ and then turn off. Bit PH_ID_INT auto-clears to 0. See Table 6.
5	DP_SRP_EN	Enables the DP pull-up resistor ($R_{UP(DP)}$). **0 —** Disable; DP pull-up can only be enabled using bit DP_PULLUP when V_{BUS} is above $V_{th(svc)}$ **1 —** Enable; DP pull-up is connected.

Table 24: Audio Control register (address Set = 16h, Clear = 17h) bit description...continued

Bit	Symbol	Description
4	ISET_STATE	Determines the logic level for pin ISET when bit ISET_DRV_EN is logic 1. **0** — ISET outputs LOW **1** — ISET outputs HIGH.
3	ISET_DRV_EN	Enables software control of the state of pin ISET: **0** — Disable; the ISET output will be controlled by hardware **1** — Enable; the ISET output will be controlled by bit ISET_STATE.
2	SW_MIC_SPKR_R	Audio loopback test: **0** — Turn off the switch between the MIC and SPKR_R pins **1** — Turn on the switch between the MIC and SPKR_R pins.
1	SW_MIC_SPKR_L	Audio loopback test: **0** — Turn off the switch between the MIC and SPKR_L pins **1** — Turn on the switch between the MIC and SPKR_L pins.
0	AUDIO_MONO	Selection between stereo and mono audio modes: **0** — Stereo mode: SPKR_L ↔ DM, SPKR_R ↔ DP **1** — Mono mode: SPKR_L ↔ DM, MIC ↔ DP.

9.1.2.4 Timer Control register (S/C: 18h/19h)

The bit allocation of the Timer Control register is given in Table 25.

Table 25: Timer Control register (address Set = 18h, Clear = 19h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TMR_SE1[3:0]				reserved			
Reset	0	0	0	1	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 26: Timer Control register (address Set = 18h, Clear = 19h) bit description

Bit	Symbol	Description
7 to 4	TMR_SE1[3:0]	Program the timer value to detect SE1 on the DP and DM lines. The interval is 1 ms (Default value = 1 ms).
3 to 0	-	reserved

9.1.2.5 Resistor Control register

Table 27 shows the bit allocation of the Resistor Control register.

Table 27: Resistor Control register (address Set = 06h, Clear = 07h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	VBUS_CHRG	VBUS_DISCHRG	reserved	ID_PULLDN	DM_PULLDOWN	DP_PULLDOWN	DP_WKPU_EN	DP_PULLUP
Reset	0	0	0	0	0	0	1	1
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 28: Resistor Control register (address Set = 06h, Clear = 07h) bit description

Bit	Symbol	Description
7	VBUS_CHRG	Charge V_{BUS} through a pull-up resistor ($R_{UP(VBUS)}$) that is connected to REG3V3. **0** — Disconnect the resistor **1** — Connect the resistor.
6	VBUS_DISCHRG	Discharge V_{BUS} through a pull-down resistor ($R_{DN(VBUS)}$). **0** — Disconnect the resistor **1** — Connect the resistor.
5	reserved	reserved; cleared (set to 0)
4	ID_PULLDN	Connect pin ID to ground. See Table 6. **0** — Disconnected **1** — Connected.
3	DM_PULLDOWN	Connect the DM pull-down resistor ($R_{DN(DM)}$). **0** — DM pull-down resistor is disconnected **1** — DM pull-down resistor is connected.
2	DP_PULLDOWN	Connect the DP pull-down resistor ($R_{DN(DP)}$). **0** — DP pull-down resistor is disconnected **1** — DP pull-down resistor is connected.
1	DP_WKPU_EN	Connect the DP weak pull-up resistor ($R_{weakUP(DP)}$). **0** — DP weak pull-up resistor is disconnected **1** — DP weak pull-up resistor is connected.
0	DP_PULLUP	Connect the DP pull-up resistor ($R_{UP(DP)}$). The pull-up resistor will be connected to the DP line only when $V_{BUS} > V_{th(svc)}$. **0** — DP pull-up resistor is disconnected **1** — DP pull-up resistor is connected, if $V_{BUS} > V_{th(svc)}$.

9.1.3 Interrupt registers

9.1.3.1 Interrupt Source register

Table 29 shows the bit allocation of this register that indicates the current state of the signals that can generate an interrupt.

Table 29: Interrupt Source register (address 08h) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DP_INT	reserved	ID_FLOAT	SE1	ID_GND	DP_HI	SESS_VLD	VBUS_DET
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 30: Interrupt Source register (address 08h) bit description

Bit	Symbol	Description
7	DP_INT	Set to logic 1 when the DP voltage is higher than carkit interrupt threshold $V_{th(DP)L}$ (0.4 V to 0.6 V). **0** — Voltage on DP is below $V_{th(DP)L}$ **1** — Voltage on DP is above $V_{th(DP)L}$.
6	-	reserved
5	ID_FLOAT	Indicates the status of pin ID: **0** — ID pin is not floating **1** — ID pin is floating.
4	SE1	DP and DM SE1 detected. The period of SE1 needed is controlled by TMR_SE1 bits. **0** — SE1 is not detected **1** — SE1 is detected.
3	ID_GND	Indicates the status of pin ID: **0** — ID pin is not grounded **1** — ID pin is grounded.
2	DP_HI	DP single-ended receiver output: **0** — LOW **1** — HIGH.
1	SESS_VLD	V_{BUS} session valid detector: **0** — V_{BUS} is lower than $V_{th(svc)}$ **1** — V_{BUS} is higher than $V_{th(svc)}$.
0	VBUS_DET	V_{BUS} HIGH detector: **0** — V_{BUS} is lower than $V_{th(VBUS\_HI)}$ **1** — V_{BUS} is higher than $V_{th(VBUS\_HI)}$.

9.1.3.2 Interrupt Latch register

This register indicates the source that generates an interrupt. For bit allocation, see Table 31.

Table 31: Interrupt Latch register (address Set = 0Ah, Clear = 0Bh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DP_INT_INT	reserved	ID_FLOAT_INT	SE1_INT	ID_GND_INT	DP_HI_INT	SESS_VLD_INT	VBUS_DET_INT
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 32: Interrupt Latch register (address Set = 0Ah, Clear = 0Bh) bit description

Bit	Symbol	Description
7	DP_INT_INT	**0** — No interrupt **1** — Interrupt on the DP_INT status change.

Table 32: Interrupt Latch register (address Set = 0Ah, Clear = 0Bh) bit description...*continued*

Bit	Symbol	Description
6	-	reserved
5	ID_FLOAT_INT	**0** — No interrupt **1** — Interrupt on the ID_FLOAT status change.
4	SE1_INT	**0** — No interrupt **1** — Interrupt on the SE1 status change.
3	ID_GND_INT	**0** — No interrupt **1** — Interrupt on the ID_GND status change.
2	DP_HI_INT	**0** — No interrupt **1** — Interrupt on the DP_HI status change.
1	SESS_VLD_INT	**0** — No interrupt **1** — Interrupt on the SESS_VLD status change.
0	VBUS_DET_INT	**0** — No interrupt **1** — Interrupt on the VBUS_DET status change.

9.1.3.3 Interrupt Enable Low register

The bits in this register enable interrupts when the corresponding bits in the Interrupt Source register changes from logic 1 to logic 0.

Table 33 shows the bit allocation of the register.

Table 33: Interrupt Enable Low register (address Set = 0Ch, Clear = 0Dh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DP_INT_IEL	reserved	ID_FLOAT_IEL	SE1_IEL	ID_GND_IEL	DP_HI_IEL	SESS_VLD_IEL	VBUS_DET_IEL
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 34: Interrupt Enable Low register (address Set = 0Ch, Clear = 0Dh) bit description

Bit	Symbol	Description
7	DP_INT_IEL	**0** — Disable **1** — Enable.
6	-	reserved
5	ID_FLOAT_IEL	**0** — Disable **1** — Enable.
4	SE1_IEL	**0** — Disable **1** — Enable.
3	ID_GND_IEL	**0** — Disable **1** — Enable.
2	DP_HI_IEL	**0** — Disable **1** — Enable.
1	SESS_VLD_IEL	**0** — Disable **1** — Enable.
0	VBUS_DET_IEL	**0** — Disable **1** — Enable.

9.1.3.4 Interrupt Enable High register

The bit allocation of the register is given in Table 35. The bits in this register enable interrupts when the corresponding bits in the Interrupt Source register changes from logic 0 to logic 1.

Table 35: Interrupt Enable High register (address Set = 0Eh, Clear = 0Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DP_INT_IEH	reserved	ID_FLOAT_IEH	SE1_IEH	ID_GND_IEH	DP_HI_IEH	SESS_VLD_IEH	VBUS_DET_IEH
Reset	0	0	0	0	0	0	0	0
Access	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C	R/S/C

Table 36: Interrupt Enable High register (address Set = 0Eh, Clear = 0Fh) bit description

Bit	Symbol	Description
7	DP_INT_IEH	**0** — Disable **1** — Enable.
6	-	reserved
5	ID_FLOAT_IEH	**0** — Disable **1** — Enable.
4	SE1_IEH	**0** — Disable **1** — Enable.
3	ID_GND_IEH	**0** — Disable **1** — Enable.
2	DP_HI_IEH	**0** — Disable **1** — Enable.
1	SESS_VLD_IEH	**0** — Disable **1** — Enable.
0	VBUS_DET_IEH	**0** — Disable **1** — Enable.

9.2 Interrupts

Any of the Interrupt Source register signals given in Table 29 can generate an interrupt when the signal becomes either LOW or HIGH. After an interrupt is generated, the SoC can read the status of each signal and the bit that indicates whether or not that signal generated the interrupt.

A bit in the Interrupt Latch register is set when any of these occurs:

- Writing logic 1 to its set address causes the corresponding bit to be set.
- The corresponding bit in the Interrupt Enable High register is set, and the associated signal changes from LOW-to-HIGH.
- The corresponding bit in the Interrupt Enable Low register is set, and the associated signal changes from HIGH-to-LOW.

9.3 SPI interface

9.3.1 Pinout description

The SPI interface consists of four signals as given in Table 37.

Table 37: SPI interface pin description

Pin name	Description
SPI_MOSI	serial data input line
SPI_MISO	serial data output line
SPI_CLK	clock input line
SPI_CS	clock enable line (active HIGH)

9.3.2 Interface overview

The SPI interface has the following characteristics:

- The maximum clock rate is 26 MHz.
- Data is transmitted, most significant bit first. Each data field consists of a total of 32 bits.
- The data and SPI_CLK signals are ignored, if SPI_CS is LOW. SPI_MISO is set to three-state, if SPI_CS is programmed LOW.
- SPI_CS is active (HIGH) only during the serial data transmission.
- All input data is sampled at the rising edge of the SPI_CLK signal. Any transition on SPI_MOSI must occur at least 5 ns before the rising edge of SPI_CLK and remain stable for at least 5 ns after the rising edge of SPI_CLK.
- All output data is updated at the rising edge of the SPI_CLK signal. Any transition on SPI_MISO must occur at least 5 ns before the rising edge of SPI_CLK and remain stable for at least 19.23 ns after the rising edge of SPI_CLK.
- SPI_CS must be active (HIGH) at least 5 ns before the rising edge of the first SPI_CLK signal, and must remain active (HIGH) at least 61.5 ns after the last falling edge of SPI_CLK.
- Coincident rising or falling edge of SPI_CLK and SPI_CS are not allowed.
- If SPI_CS goes LOW before enough bits are sent, then the data bits sent are ignored.
- When SPI_CS goes LOW to complete the SPI operation, the next rising edge of SPI_CS must be delayed by at least 30 ns.

9.3.3 Interface protocol description

The SPI port is configured to use 32-bit serial data words, using 1 bit for R/W, 5 bits for address, 1 bit for null, and 25 bits for data.

For each SPI transfer, a one is written to pin SPI_MOSI, if this SPI transfer is to be a write. A zero is written to the pin, if this is to be a read-only command. If a zero is written, then any data sent after the address bits is ignored and the internal contents of the field addressed do not change when the 32nd SPI_CLK is sent. Next, the 5-bit address is written to pin SPI_MOSI MSB first. Finally, data bits are written to the pin MSB first. Once all the data bits are written, data is transferred to the actual registers on the 32nd SPI_CLK. SPI_CS must go LOW and return to HIGH to start the next SPI data transfer.

To read a field of data, pin SPI_MISO will output the data field pointed to by the five address bits loaded at the beginning of the SPI sequence.

Figure 7 shows the details of an SPI transfer.

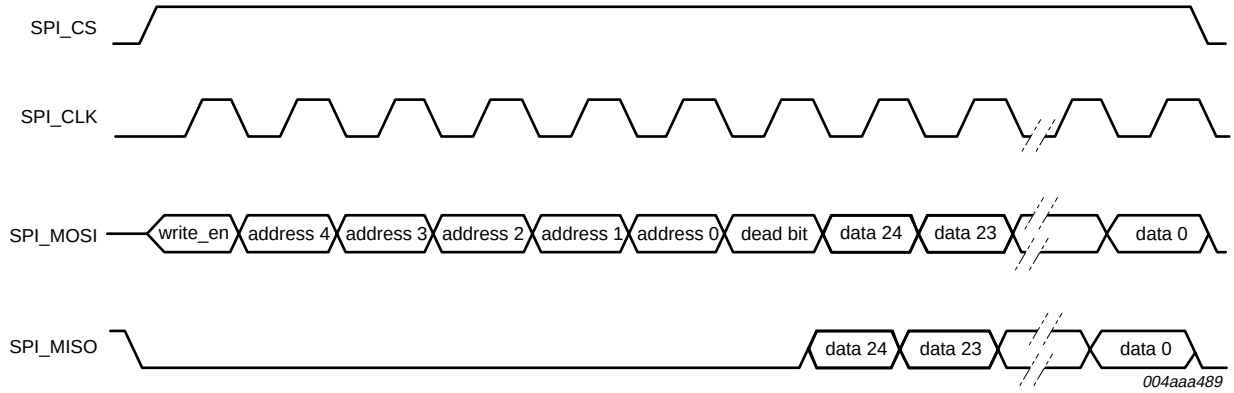


Fig 7. SPI transfer.

Figure 8 shows a multiple read and write by using the SPI bus.

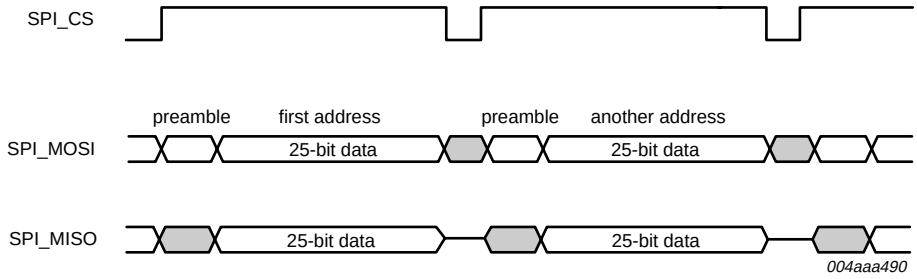


Fig 8. SPI multiple read and write.

9.4 I²C-bus protocol

For detailed information, refer to *The I²C-bus Specification; Version 2.1*.

9.4.1 I²C-bus byte transfer format

Table 38: I²C-bus byte transfer format

S [1]	Byte 1	A [2]	Byte 2	A [2]	Byte 3	A [2]	..	A [2]	P [3]
	8 bits		8 bits		8 bits		..		

[1] S = Start.

[2] A = Acknowledge.

[3] P = Stop.

9.4.2 I²C-bus device address

Table 39: I²C-bus slave address bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	A6	A5	A4	A3	A2	A1	A0	R/W_N
Value	0	1	0	1	1	0	[1]	X

[1] Determined by logic level on pin I2C_ADR: LOW = 0, HIGH = 1.

Table 40: I²C-bus slave address bit description

Bit	Symbol	Description
7 to 1	A[6:0]	**Device address**: The device address of the ISP1109 is: 01 0110 (A0).
0	R/W_N	Read or write command. **0 —** write **1 —** read.

9.4.3 Write format

A write operation can be performed as:

- One-byte write to the specified register address
- Multiple-byte write to N consecutive registers, starting from the specified start address. N defines the number of registers to write to. If N = 1, only the start register is written.

9.4.3.1 One-byte write

Table 41 describes the transfer format for a one-byte write.

Table 41: Transfer format description for a one-byte write

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits address of register K
ACK	slave generates an acknowledgment
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
P	master generates a STOP condition

9.4.3.2 Multiple-byte write

Table 42 describes the transfer format for a multiple-byte write.

Table 42: Transfer format description for a multiple-byte write

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment

Table 42: Transfer format description for a multiple-byte write*...continued*

Byte	Description
Register address K	master transmits address of register K. This is the start address for writing multiple data bytes to consecutive registers. After a byte is written, the register address is automatically incremented by 1. **Remark:** If the master writes to a nonexistent register, the slave must send a 'not ACK' and also must not increment the index address.
ACK	slave generates an acknowledgment
Write data K	master writes data to register K
ACK	slave generates an acknowledgment
Write data K + 1	master writes data to register K + 1
ACK	slave generates an acknowledgment
:	:
Write data K + N – 1	master writes data to register K + N – 1. When the incremented address K + N – 1 becomes > 255, the register address rolls over to 0. Therefore, it is possible that some registers may be overwritten, if the transfer is not stopped before the rollover.
ACK	slave generates an acknowledgment
P	master generates a STOP condition

Figure 9 illustrates the write format for a one-byte write and a multiple-byte write.

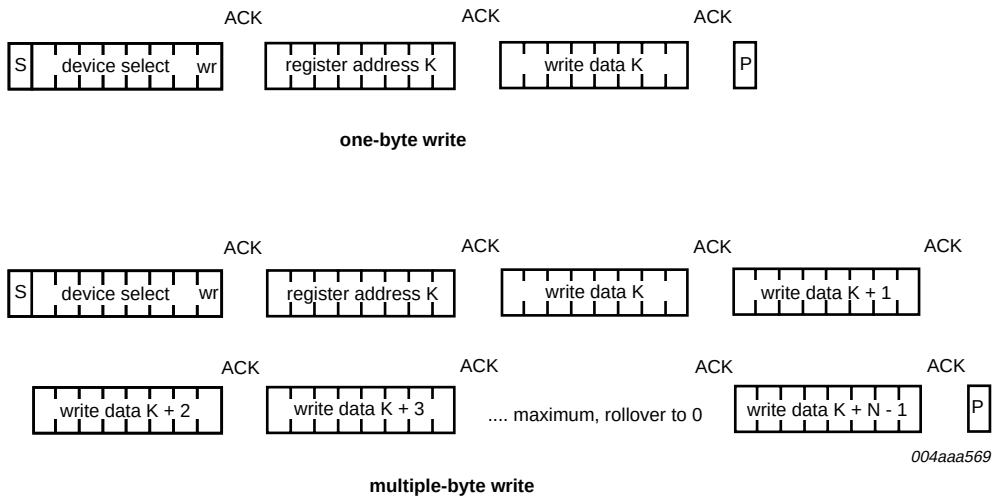


Fig 9. Writing data to the ISP1109 registers.

9.4.4 Read format

A read operation can be performed in two ways:

- Current address read: to read the register at the current address.
  - Single-register read.
- Random address read: to read N registers starting at a specified address. N defines the number of registers to be read. If N = 1, only the start register is read.
  - Single-register read

– Multiple-register read.

9.4.4.1 Current address read

The transfer format description for a current address read is given in Table 43. For illustration, see Figure 10.

Table 43: Transfer format description for current address read

Byte	Description
S	master starts with a START condition
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. If the start address is not specified, the read operation starts from where the index register is pointing to because of a previous read or write operation.
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a stop condition

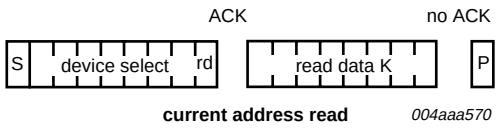


Fig 10. Current address read.

9.4.4.2 Random address read—Single read

Table 44 describes the transfer format for a single-byte read. Figure 11 illustrates the byte sequence.

Table 44: Transfer format description for single-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K to be read from
ACK	slave generates an acknowledgment
S	master restarts with a START condition
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a STOP condition

9.4.4.3 Random address read—Multiple read

The transfer format description for a multiple-byte read is given in Table 45. Figure 11 illustrates the byte sequence.

Table 45: Transfer format description for a multiple-byte read

SDA line	Description
S	master starts with a START condition
Device select	master transmits device address and write command bit R/W = 0
ACK	slave generates an acknowledgment
Register address K	master transmits (start) address of register K to be read from
ACK	slave generates an acknowledgment
S	master restarts with a START condition
Device select	master transmits device address and read command bit R/W = 1
ACK	slave generates an acknowledgment
Read data K	slave transmits and master reads data from register K. After a byte is read, the address is automatically incremented by 1.
ACK	slave generates an acknowledgment
Read data K + 1	slave transmits and master reads data from register K + 1
ACK	slave generates an acknowledgment
:	:
Read data K + N – 1	slave transmits and master reads data register K + N – 1. This is the last register to read. After incrementing, the address rolls over to 0. Here, N represents the number of addresses available in the slave.
No ACK	master terminates the read operation by generating a No Acknowledge
P	master generates a STOP condition

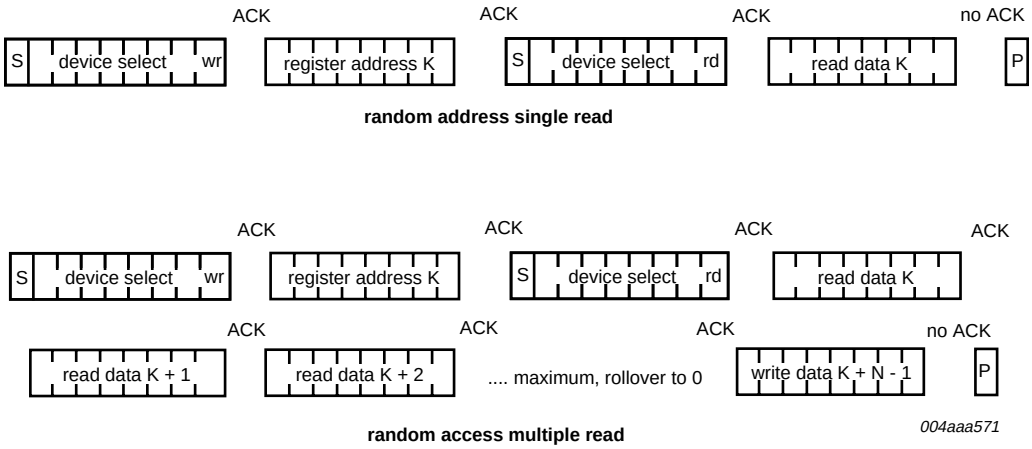


Fig 11. Random address read.

10. Clock wake-up scheme

This section explains the ISP1109 clock stop timing, events triggering the clock to wake up, and the timing of the clock wake-up.

10.1 Power-down event

If $V_{CC(I/O)}$ is not present and the V_{BUS} voltage is below the SESS_VLD threshold (0.8 V to 2.0 V), the ISP1109 is in Power-down mode and internal clocks are turned off. The internal clock—LazyClock or I^2C-bus clock or both—is stopped when bit PWR_DN is set. It takes approximately 8 ms for the clock to stop from the time the Power-down condition is detected.

If SPI mode is selected, a register read or write access is normal, as when in Power-down mode. If I^2C-bus mode is selected, the internal clock must first be woken up before any register read or write operation.

10.2 Clock wake-up event

The clock wakes up when any of the following events occurs on ISP1109 pins:

- Pin SPI_CLK/I2C_SCL goes LOW, if I^2C-bus mode is selected (pin SPI_I2C_SEL is HIGH).
- Pin V_{BUS} goes above the session valid threshold (0.8 V to 2.0 V), provided bit SESS_VLD_IEH of the Interrupt Enable High register is set.
- Status bit ID_FLOAT changes from logic 1 to logic 0, provided bit ID_FLOAT_IEL of the Interrupt Enable Low register is set.
- Status bit ID_FLOAT changes from logic 0 to logic 1, provided bit ID_FLOAT_IEH of the Interrupt Enable High register is set.
- Status bit SE1 changes from logic 0 to logic 1, provided bit SE1_IEH of the Interrupt Enable High register is set.

The event triggers the clock to start. A stable clock is guaranteed within 100 µs.

When an event is triggered and the clock is started, it will remain active for approximately 8 ms. If bit PWR_DN is not cleared within this 8 ms period, the clock will stop. If the clock wakes up because of any event other than SPI_CLK/I2C_SCL going LOW, an interrupt will be generated once the clock is active.

11. Electro-Static Discharge (ESD)

11.1 ESD protection

The pins that are connected to the USB connector—DP, DM, ID, V_{BUS}, V_{CC}, GNDA and GNDD—have a minimum of ±12 kV ESD protection. The ±12 kV measurement is limited by the test equipment. Capacitors of 4.7 µF connected from REG3V3 to GNDA and V_{BUS} to GNDA are required to achieve this ±12 kV ESD protection. See Figure 12.

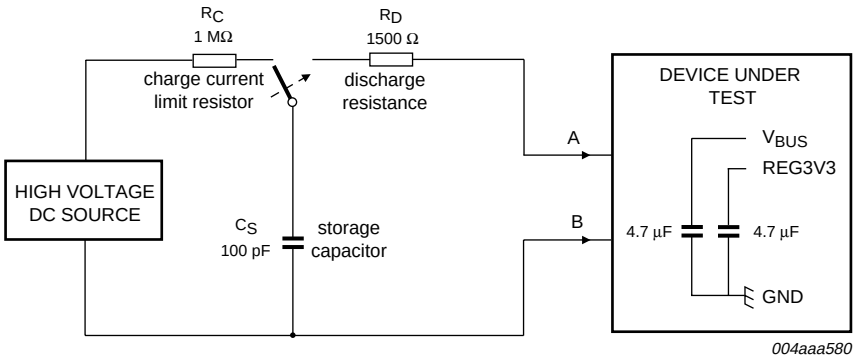


Fig 12. Human Body ESD test model.

11.2 ESD test conditions

A detailed report on test setup and results is available on request.

12. Limiting values

Table 46: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Voltage						
V_{CC}	supply voltage			–0.5	+7.0	V
$V_{CC(I/O)}$	I/O supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	$V_{CC(I/O)}$ + 0.5 V	V
V_{BUS}	V_{BUS} input voltage			–0.5	+7.0	V
$V_{I(ID)}$	ID input voltage			–0.5	+5.5	V
V_{esd}	electrostatic discharge voltage	I_{LI} < 1 µA				
		pins DP, DM, ID, V_{BUS}, V_{CC}, GNDA and GNDD	[2] [3]	–12	+12	kV
		all other pins		–2	+2	kV
Current						
I_{lu}	latch-up current			-	100	mA

[1] Input voltage on all digital pins.

[2] Testing equipment limits measurement to only ±12 kV. 4.7 µF capacitors needed on V_{BUS} and REG3V3 (see Section 11).

[3] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model).

13. Recommended operating conditions

Table 47: Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Voltage							
V_{CC}	supply voltage			3.0	-	5.25	V
$V_{CC(I/O)}$	I/O supply voltage		[1]	1.65	-	3.6	V
V_{REF}	audio supply voltage			2.65	-	3.0	V
V_I	input voltage		[2]	0	-	$V_{CC(I/O)}$	V
$V_{I(AI/O)}$	input voltage on analog I/O pins DP and DM			0	-	3.6	V
$V_{O(OD)}$	open-drain output pull-up voltage			1.65	-	3.6	V
Temperature							
T_{amb}	ambient temperature			–40	-	+85	°C

[1] $V_{CC(I/O)}$ must be less than or equal to V_{CC}.

[2] Input voltage on all digital pins.

14. Static characteristics

Table 48: Static characteristics: supply pins

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Voltage							
$V_{O(REG3V3)}$	regulated supply voltage output	$I_{LOAD} \leq 300$ µA	[1]	3.0	3.3	3.6	V
Current							
I_{CC}	operating supply current	transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins DP and DM	[2]	-	4	8	mA
$I_{CC(I/O)}$	operating I/O supply current	transmitting and receiving at 12 Mbit/s	[2]	-	1	2	mA
$I_{CC(I/O)(isolate)}$	isolate mode I/O supply current	V_{CC} not connected		-	-	10	µA
$I_{CC(idle)}$	supply current during full-speed idle and SE0	idle: $V_{DP} > 2.7$ V, $V_{DM} < 0.3$ V; SE0: $V_{DP} < 0.3$ V, $V_{DM} < 0.3$ V	[3]	-	-	300	µA
$I_{CC(I/O)(static)}$	static I/O supply current	idle, SE0 or suspend		-	-	20	µA
$I_{CC(pd)}$	Power-down mode supply current	bit PWR_DN = 1 or $V_{CC(I/O)}$ = 0 V	[3]	-	-	20	µA
I_{VREF}	supply current on pin V_{REF}			-	-	100	µA

[1] In Power-down mode, the minimum voltage is 2.7 V.

[2] Maximum value characterized only, not tested in production. Typical value measured at V_{CC} = 5 V, $V_{CC(I/O)}$ = 1.8 V and T_{amb} = 25 °C.

[3] Excluding any load current to the 1.5 kΩ and 15 kΩ pull-up and pull-down resistors (200 µA typical).

Table 49: Static characteristics: digital pins (except for ISET)

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input level voltage							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.6V_{CC(I/O)}$	-	-	V
Output level voltage							
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA		-	-	0.4	V
		I_{OL} = 100 µA		-	-	0.15	V
V_{OH}	HIGH-level output voltage	I_{OH} = 2 mA	[1]	$V_{CC(I/O)}$ − 0.4 V	-	-	V
		I_{OH} = 100 µA		$V_{CC(I/O)}$ − 0.15 V	-	-	V
Leakage current							
I_{LI}	input leakage current		[2]	−1	-	+1	µA
Open-drain output current							
I_{OZ}	OFF-state output current			−5	-	+5	µA
Capacitance							
C_{IN}	input capacitance	pin to GND		-	-	10	pF

[1] Not applicable for open-drain outputs.

[2] $V_{CC(I/O)}$ is not greater than $V_{O(REG3V3)}$.

Table 50: Static characteristics: digital pin ISET

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage						
$V_{th(ISET)}$	V_{CC} threshold voltage for ISET function		1.5	-	2.5	V
$V_{OH(ISET)}$	V_{OH} on pin ISET	$V_{CC} \geq 3.0$ V	2.4	-	-	V
		$V_{CC} < 3.0$ V	$0.8V_{CC}$	-	-	V
Timing						
$t_{d(ISET)}$	time from ISET condition to the ISET pin HIGH		-	-	1.5	ms

Table 51: Static characteristics: analog I/O pins DP and DM

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input level voltage						
V_{DI}	differential input sensitivity	$\|V_{DP} - V_{DM}\|$	0.2	-	-	V
V_{CM}	differential common mode voltage	includes V_{DI} range	0.8	-	2.5	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
Output level voltage						
V_{OL}	LOW-level output voltage	R_L of 1.5 kΩ to +3.6 V	-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L of 15 kΩ to GND	2.8	-	3.6	V
Voltage						
$V_{th(DP)L}$	DP LOW threshold		0.4	-	0.6	V
V_{TERM}	termination voltage for the upstream port pull-up resistor (R_{PU})		3.0	-	3.6	V
Leakage current						
I_{LZ}	OFF-state leakage current		−1	-	+1	μA
Capacitance						
C_{IN}	input capacitance	pin to GNDA	-	-	10	pF
Resistance						
R_{PD}	pull-down resistance on pins DP and DM		14.25	-	24.8	kΩ
$R_{UP(DP)}$	pull-up resistance on pin DP	bus idle	900	-	1575	Ω
		bus driven	1425	-	3090	Ω
$R_{weakUP(DP)}$	weak pull-up resistance on pin DP		91	-	169	kΩ
Z_{DRV}	driver output impedance	steady-state drive [1]	34	-	44	Ω
Z_{INP}	input impedance		10	-	-	MΩ

[1] Includes external series resistors of 33 Ω ± 1 % each on DP and DM.

Table 52: Static characteristics: analog I/O pins ID and ID_PU

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage						
$V_{th(ID\_GND)}$	ID_GND comparator threshold		0.2	-	0.8	V
$V_{th(ID\_FLOAT)}$	ID_FLOAT comparator threshold		2.0	-	$V_{O(REG3V3)}$ − 0.2 V	V
$V_{th(ID\_FM)}$	ID factory mode detector threshold		3.0	-	3.8	V
Resistance						
R_{PU_ID}	ID pull-up switch impedance between pins ID_PU and V_{REF}		-	-	500	Ω
R_{PD_ID}	ID impedance to GND	bit ID_PULLDOWN = 1	-	-	50	Ω

Table 53: Static characteristics: analog I/O pin V_{BUS}

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage						
$V_{th(VBUS\_HI)}$	V_{BUS} detector		3.0	-	3.8	V
$V_{th(svc)}$	V_{BUS} session valid comparator threshold		0.8	-	2.0	V
$V_{hys(svc)}$	V_{BUS} session valid comparator hysteresis		-	200	-	mV
Resistance						
$R_{UP(VBUS)}$	pull-up resistance on pin V_{BUS}	connect to REG3V3 when VBUS_CHRG = 1	460	-	1000	Ω
$R_{DN(VBUS)}$	pull-down resistance on pin V_{BUS}	connect to GND when VBUS_DISCHRG = 1	660	-	1200	Ω

Table 54: Static characteristics: analog I/O pins SPKR_L, SPKR_R and MIC

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Capacitance						
C_{IN}	input capacitance	pin to GNDA	-	-	10	pF
Impedance						
$Z_{asw(on)}$	audio switch ON state impedance	0 kHz to 20 kHz	50	-	150	Ω
$Z_{asw(off)}$	audio switch OFF state impedance	0 kHz to 20 kHz	2	-	-	MΩ

15. Dynamic characteristics

Table 55: Dynamic characteristics: reset and clock

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset						
$t_{W(RESET\_N)}$	pulse width on input RESET_N		10	-	-	µs
Internal clock						
f_{clk}	clock frequency	bit GLOBAL_PWR_DN = 0	70	100	130	kHz

Table 56: Dynamic characteristics: bus turnaround timing (USB bidirectional mode)

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TOI}	bus turnaround time (OE_N to DAT/VP and SE0/VM)	output-to-input; see Figure 17	0	-	5	ns
t_{TIO}	bus turnaround time (OE_N to DAT/VP and SE0/VM)	input-to-output; see Figure 17	0	-	5	ns

Table 57: Dynamic characteristics: analog I/O pins DP and DM

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics							
t_{FR}	rise time	C_L = 50 pF to 125 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 13		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF to 125 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 13		4	-	20	ns
FRFM	differential rise time and fall time matching (t_{FR}/t_{FF})	excluding the first transition from the idle state		90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from the idle state; see Figure 14	[1]	1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	propagation delay (DAT/VP, SE0/VM to DP, DM)	LOW-to-HIGH; see Figure 14 and Figure 21		-	-	18	ns
$t_{PHL(drv)}$	propagation delay (DAT/VP, SE0/VM to DP, DM)	HIGH-to-LOW; see Figure 14 and Figure 21		-	-	18	ns
t_{PHZ}	disable delay (OE_N to DP, DM)	HIGH-to-OFF; see Figure 15 and Figure 22		-	-	15	ns
t_{PLZ}	disable delay (OE_N to DP, DM)	LOW-to-OFF; see Figure 15 and Figure 22		-	-	15	ns
t_{PZH}	enable delay (OE_N to DP, DM)	OFF-to-HIGH; see Figure 15 and Figure 22		-	-	15	ns
t_{PZL}	enable delay (OE_N to DP, DM)	OFF-to-LOW; see Figure 15 and Figure 22		-	-	15	ns

Table 57: Dynamic characteristics: analog I/O pins DP and DM...*continued*

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver timing						
Differential receiver						
$t_{PLH(rcv)}$	propagation delay (DP, DM to RCV)	LOW-to-HIGH; see Figure 16 and Figure 23	-	-	15	ns
$t_{PHL(rcv)}$	propagation delay (DP, DM to RCV)	HIGH-to-LOW; see Figure 16 and Figure 23	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	propagation delay (DP, DM to VP and DAT/VP, VM and SE0/VM)	LOW-to-HIGH; see Figure 16 and Figure 23	-	-	18	ns
$t_{PHL(se)}$	propagation delay (DP, DM to VP and DAT/VP, VM and SE0/VM)	HIGH-to-LOW; see Figure 16 and Figure 23	-	-	18	ns

[1] Characterized only; not tested. Limits guaranteed by design.

Table 58: Dynamic characteristics: analog I/O pin ID

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{Wint(ID)}$	ID interrupt pulse width		4	-	8	ms
$t_{int(ID)}$	ID interrupt wait time		4	-	8	ms

Table 59: Dynamic characteristics: audio switches

V_{CC} = 3.0 V to 5.25 V; $V_{CC(I/O)}$ = 1.65 V to 3.6 V; C_L = 50 pF; R_{PU} = 1.5 kΩ on DP to V_{TERM}; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
PSRR	Power Supply Rejection Ratio; see Section 17.1	noise on V_{CC}: $V_{(p-p)}$ = 0.5 V, f = 217 Hz, 20 Hz to 20 kHz	[1]	-	-	−80	dB
		noise on V_{REF}: $V_{(p-p)}$ = 50 mV, f = 20 Hz to 20 kHz	[1]	-	-	−45	dB
$\alpha_{ct(audio)}$	crosstalk audio; see Section 17.2	$V_{(p-p)}$ = 1 V, f = 1 kHz	[1]	-	-	−66	dB
THD	Total Harmonic Distortion; see Section 17.1	$V_{(p-p)}$ = 2.3 V, f = 1 kHz	[1]	-	-	1	%
		$V_{(p-p)}$ = 2.0 V, f = 1 kHz	[1]	-	-	0.3	%
$\alpha_{iso(d-a)}$	data to audio isolation; see Section 17.3	USB 12 Mbit active on DP and DM, < 20 kHz signal components observed on the SPKR_L, SPKR_R or MIC pins		-	-	−70	dB
$V_{io(aud)}$	audio input or output voltage range			0.1	-	2.55	V

[1] $V_{(p-p)}$ indicates peak-to-peak voltage, and f indicates frequency.

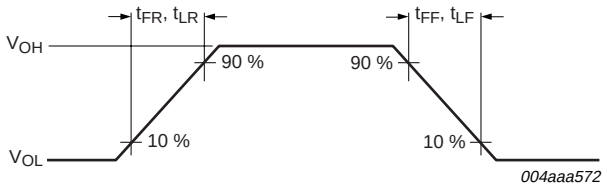


Fig 13. Rise and fall times.

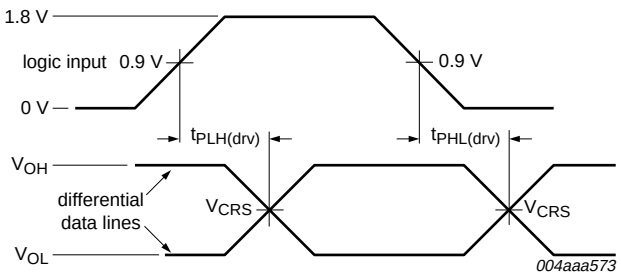


Fig 14. Timing of DAT/VP and SE0/VM to DP and DM.

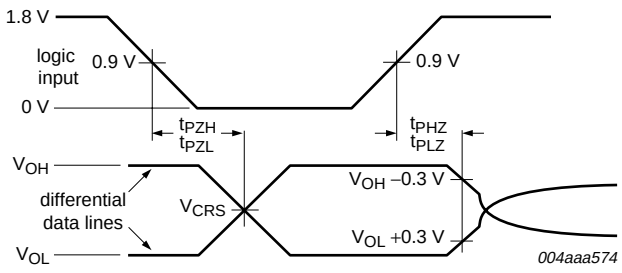


Fig 15. Timing of OE_N to DP and DM.

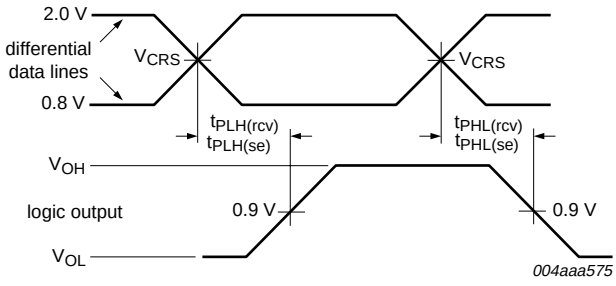


Fig 16. Timing of DP and DM to RCV, VP or DAT/VP and VM or SE0/VM.

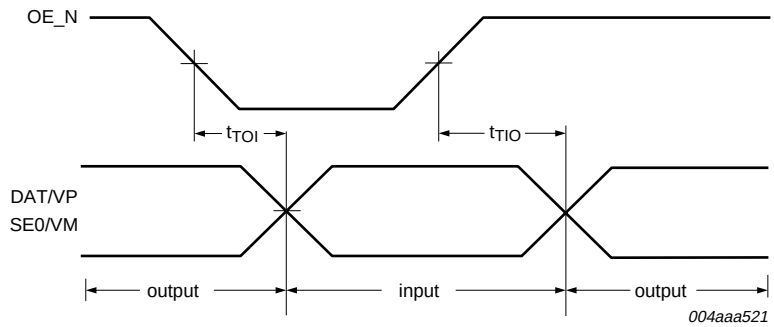


Fig 17. SIE interface bus turnaround timing.

15.1 SPI bus characteristics

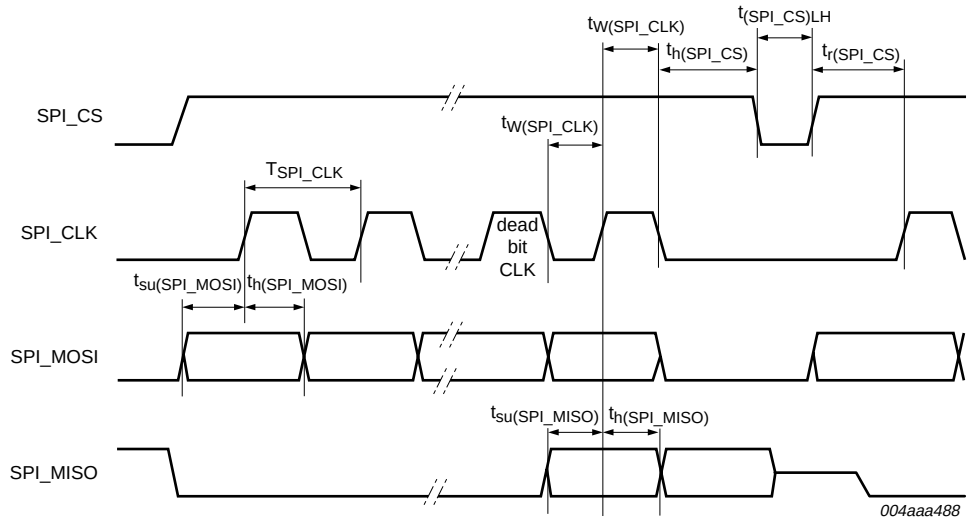


Fig 18. SPI timing diagram.

Table 60: SPI timing

Symbol	Parameter	Min	Max	Unit
T_{SPI_CLK}	SPI_CLK cycle time	38.46	-	ns
$t_{W(SPI\_CLK)}$	SPI_CLK HIGH or LOW time	19.23	-	ns
$t_{rf(SPI\_CLK)}$	SPI_CLK rise or fall time	7.6	-	ns
$t_{(SPI\_CS)LH}$	transfer delay time between queues (SPI_CS from falling edge to rising edge)	30	-	ns
$t_{r(SPI\_CS)}$	SPI_CS rise time (SPI_CS setup to SPI_CLK first rise edge)	10	-	ns
$t_{h(SPI\_CS)}$	SP_CS hold time (SPI_CS hold after SPI_CLK last fall edge)	61.5	-	ns
$t_{su(SPI\_MOSI)}$	SPI_MOSI setup time (SPI_MOSI valid to SPI_CLK rise edge)	5	-	ns
$t_{h(SPI\_MOSI)}$	SPI_MOSI hold time (SPI_CLK rise edge to SPI_MOSI valid)	5	-	ns
$t_{su(SPI\_MISO)}$	SPI_MISO setup time (SPI_MISO valid to SPI_CLK rise edge)	5	-	ns
$t_{h(SPI\_MISO)}$	SPI_MISO hold time (SPI_CLK rise edge to SPI_MISO valid)	19.23	-	ns

15.2 I²C-bus characteristics

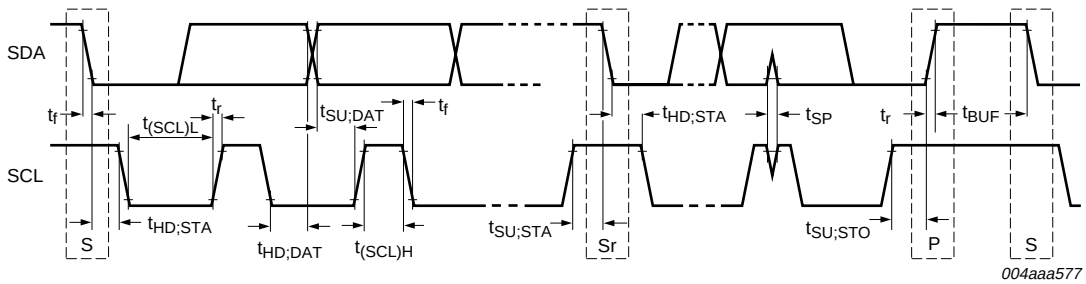


Fig 19. Definition of timing for standard-mode or fast-mode devices on the I²C-bus.

Table 61: Characteristics of I²C-bus lines (SDA, SCL)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
$t_{HD;STA}$	hold time for the START condition		4.0	-	0.6	-	µs
$t_{(SCL)L}$	LOW period of the SCL clock		4.7	-	1.3	-	µs
$t_{(SCL)H}$	HIGH period of the SCL clock		4.0	-	0.6	-	µs
$t_{SU;STA}$	setup time for the START condition		4.7	-	0.6	-	µs
$t_{SU;DAT}$	data setup time		250	-	100	-	ns
$t_{HD:DAT}$	data hold time		0	-	0	0.9	µs
t_r	rise time	SDA and SCL signals	-	1000	20 + 0.1 C_b [1]	300	ns
t_f	fall time	SDA and SCL signals	-	300	20 + 0.1 C_b [1]	300	ns
$t_{SU;STO}$	setup time for the STOP condition		4.0	-	0.6	-	µs
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	µs

[1] C_b is the capacitive load for each bus line in pF. If mixed with high-speed mode devices, faster fall times are allowed.

16. Application information

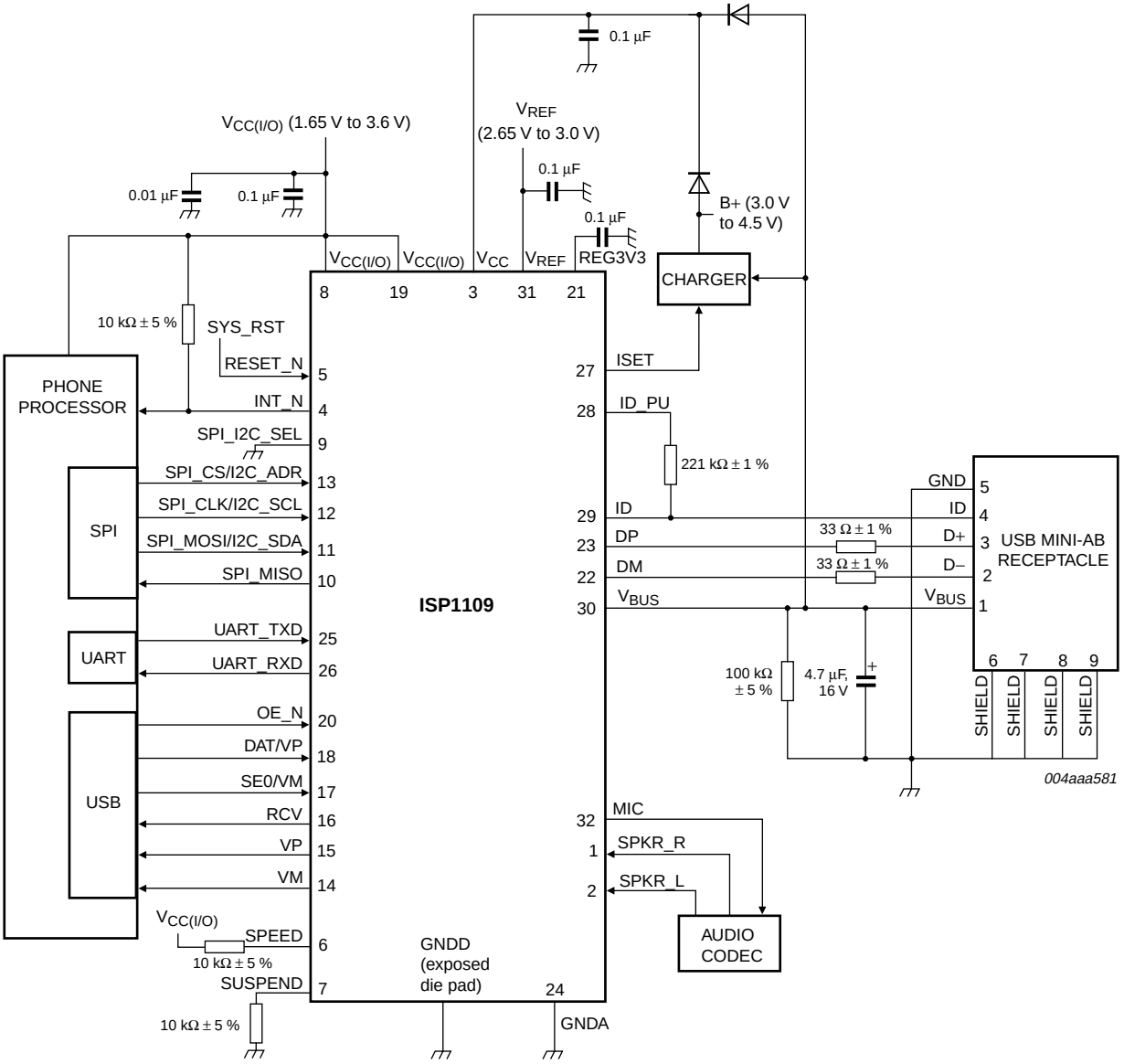
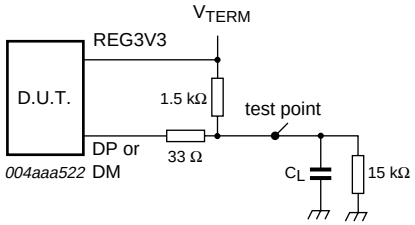


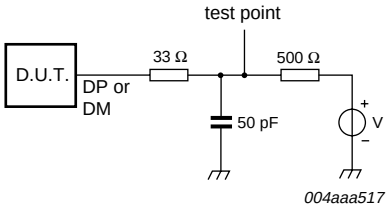
Fig 20. Application diagram.

17. Test information



Load capacitance C_L = 50 pF (minimum or maximum timing).

Fig 21. Load on pins DP and DM.



V = 0 V for t_{PZH} and t_{PHZ}.

V = $V_{O(REG3V3)}$ for t_{PZL} and t_{PLZ}.

Fig 22. Load on pins DP and DM for enable time and disable time.

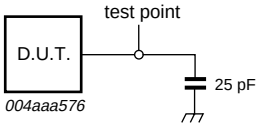


Fig 23. Load on pins VM, SE0/VM, VP, DAT/VP and RCV.

17.1 Test configurations

Table 62: Test configurations

Parameter	Pins or switches	Configuration 1	Configuration 2
Termination impedances	DP	60 kΩ	200 Ω, 1.4 V DC
	DM	60 kΩ	60 kΩ
	SPKR_R	200 Ω	200 Ω, 1.4 V DC
	SPKR_L	200 Ω	200 Ω, 1.4 V DC
	MIC	10 kΩ	10 kΩ
Switch positions [1]	S1	on	off
	S2	off	on
	S3	on	on

Table 62: Test configurations *...continued*

Parameter	Pins or switches	Configuration 1	Configuration 2
Measured ports		DP	MIC
		DM	DM

[1] For details on switches S1, S2 and S3, see Figure 5.

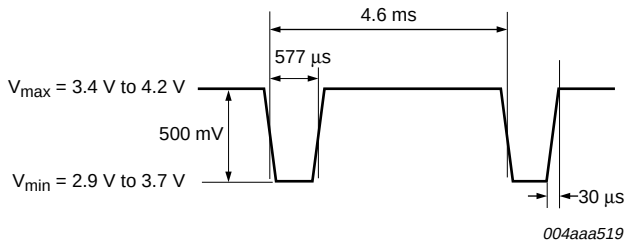


Fig 24. V_{CC} with 217 Hz noise.

17.2 Audio crosstalk test conditions

V_{CC} sweeps from 2.9 V to 4.2 V (DC waveform).

17.2.1 Test 1

- S2 = on, S3 = on
- DP is terminated using a 200 Ω; DM is terminated using a 60 kΩ
- MIC is terminated using a 10 kΩ; SPKR_L is terminated using a 200 Ω, 1.4 V DC
- Drive f = 1 kHz, $V_{(p-p)}$ = 1 V to DP; signal on DM must be 66 dB below; where f represents frequency and $V_{(p-p)}$ represents peak-to-peak voltage.

17.2.2 Test 2

- S1 = on, S3 = on
- DP and DM are terminated using a 60 kΩ
- SPKR_L and SPKR_R are terminated using a 200 Ω, 1.4 V DC
- Drive f = 1 kHz, $V_{(p-p)}$ = 1 V to SPKR_R; signal on DM must be 66 dB below; where f represents frequency and $V_{(p-p)}$ represents peak-to-peak voltage.

17.2.3 Test 3

- S1 = on, S3 = on
- DP and DM are terminated using a 60 kΩ
- SPKR_L and SPKR_R are terminated using a 200 Ω, 1.4 V DC
- Drive f = 1 kHz, $V_{(p-p)}$ = 1 V to SPKR_L; signal on DP must be 66 dB below; where f represents frequency and $V_{(p-p)}$ represents peak-to-peak voltage.

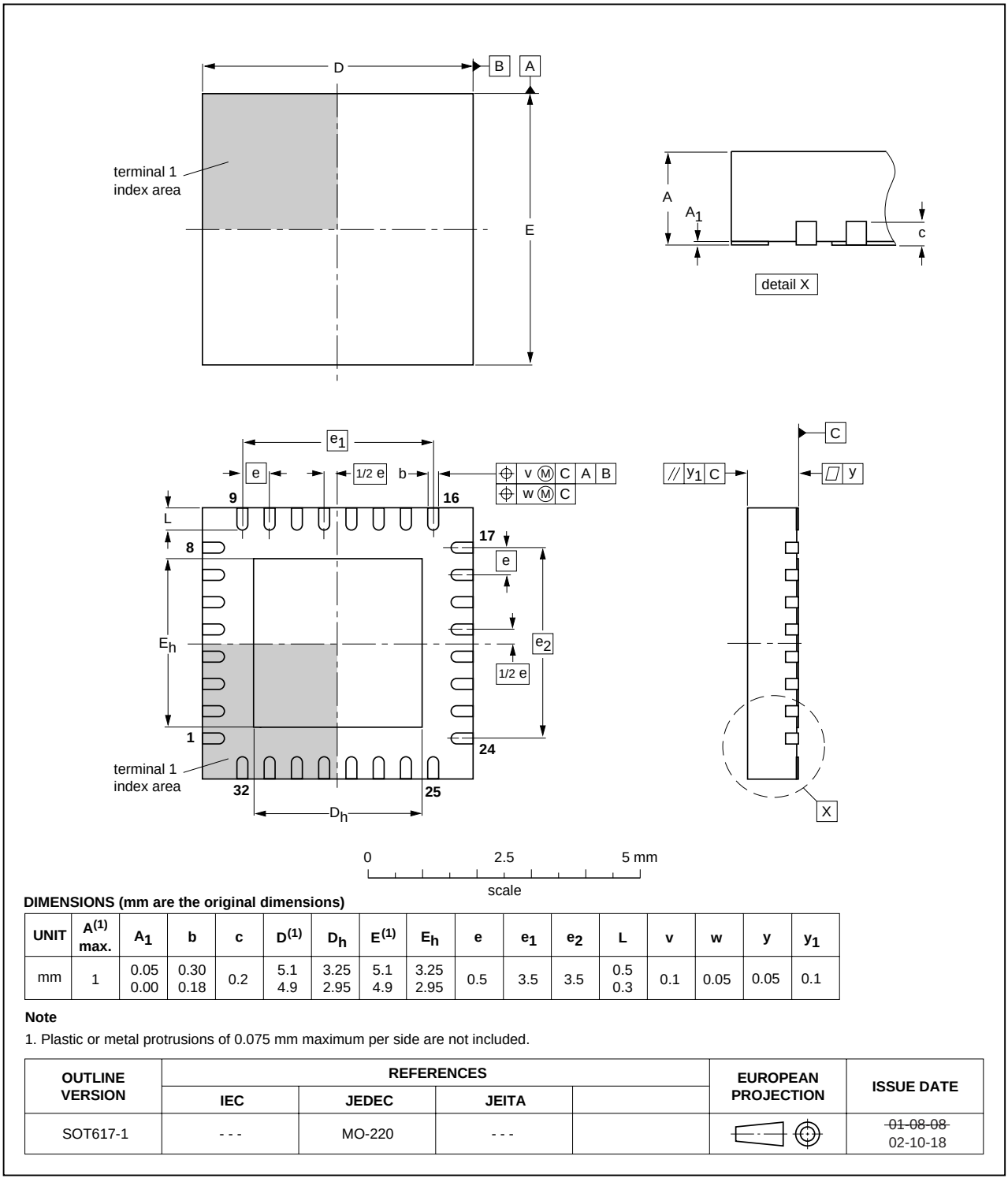
17.3 Data to audio isolation test conditions

- V_{CC} is swept from 2.9 V to 4.2 V (DC waveform)

- 12 Mbit USB data must be active on the DP and DM pins
- All audio switches must be left open
- MIC must be terminated using a 10 kΩ
- SPKR_L and SPKR_R are each terminated using a 200 Ω
- Taking an FFT on the SPKR_R, MIC and SPKR_L pins, the USB data components below 20 kHz will be < −70 dB below the USB data level (3.6 V).

18. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 25. Package outline SOT617-1 (HVQFN32).

19. Soldering

19.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

19.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

19.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

19.5 Package related soldering information

Table 63: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

20. Abbreviations

Table 64: Abbreviations

Acronym	Description
ATX	Analog USB transceiver
DC	Direct Current
ESD	Electro-Static Discharge
I^2C-bus	Inter IC-bus
LSB	Least Significant Bit
MIC	Microphone
MSB	Most Significant Bit
OTG	On-The-Go
POR	Power-On Reset
PORP	Power-On Reset Pulse
RxD	Receive Data
SE1	Single-Ended One
SoC	System-on-a-Chip
SPI	Serial Parallel Interface
SRP	Session Request Protocol
TxD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

21. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] CEA–936–A, Mini-USB Analog Carkit Interface

[3] The I^2C-bus Specification; Version 2.1

[4] ECN_27%_ Resistor (http://www.usb.org/developers/docs).

22. Revision history

Table 65: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
ISP1109_1	20050714	Product data sheet	-	9397 750 13355	-

23. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

24. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

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