

# SED1575 Series

## Dot Matrix LCD Driver

- Support up to 65×168 Display
- Built-in Power Supply Circuit for LCD

### ■ OVERVIEW

The 1575 series is a 1-chip dot matrix liquid crystal driver that can be connected to the bus of a microcomputer. It stores the 8-bit parallel or serial display data sent from the microcomputer in the built-in display data RAM and generates liquid crystal drive signals independently of the microcomputer. Since it incorporates 65 × 200 bits of the display data RAM and the one-dot pixel of the liquid crystal panel and one bit of the built-in RAM have a one-to-one correspondence, it enables display with the high degree of freedom.

The SED1575 series incorporates 65 circuits of the common output and 168 circuits of the segment output and can display 65 × 168 dots (capable of displaying 10 columns × 4 rows of a 16 × 16 dot kanji font) using the single chip. The SED1577 Series incorporates 33 circuits of the common output and 200 circuits of the segment output and can display 33 × 200 dots (capable of displaying 12 columns × 2 rows of a 16 × 16 dot kanji font). It can also expand the display capacity by using the two chips for the master and slave configuration.

Since the read/write operation of the display data RAM does not require external operation clocks, the SED1575 series can be operated with the minimum current consumption. Since it also incorporates a liquid crystal drive power supply with low current consumption, liquid crystal drive power supply voltage adjusting resistor, and display clock CR oscillator circuit, it can provide a display system for high performance handy equipment with the minimum current consumption and the minimum parts configuration.

### ■ FEATURES

- Direct display of RAM data using the display data RAM
  - RAM bit data      "1" .... goes on.
  - "0" .... goes off (at display normal rotation).
- RAM capacity
  - 65 × 200 = 13,000 bits
- Liquid crystal drive circuit
  - The SED1575 Series
    - 65 circuits for the common output and 168 circuits for the segment output
  - The SED1577 Series
    - 33 circuits for the common output and 200 circuits for the segment output
- High-speed 8-bit MPU interface (Both the 80 and 68 series MPUs can directly be connected.)/serial interface enabled
- Abundant command functions
  - Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Status Read, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V5 Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, Common Output State Selection, and Built-in Oscillator Circuit ON

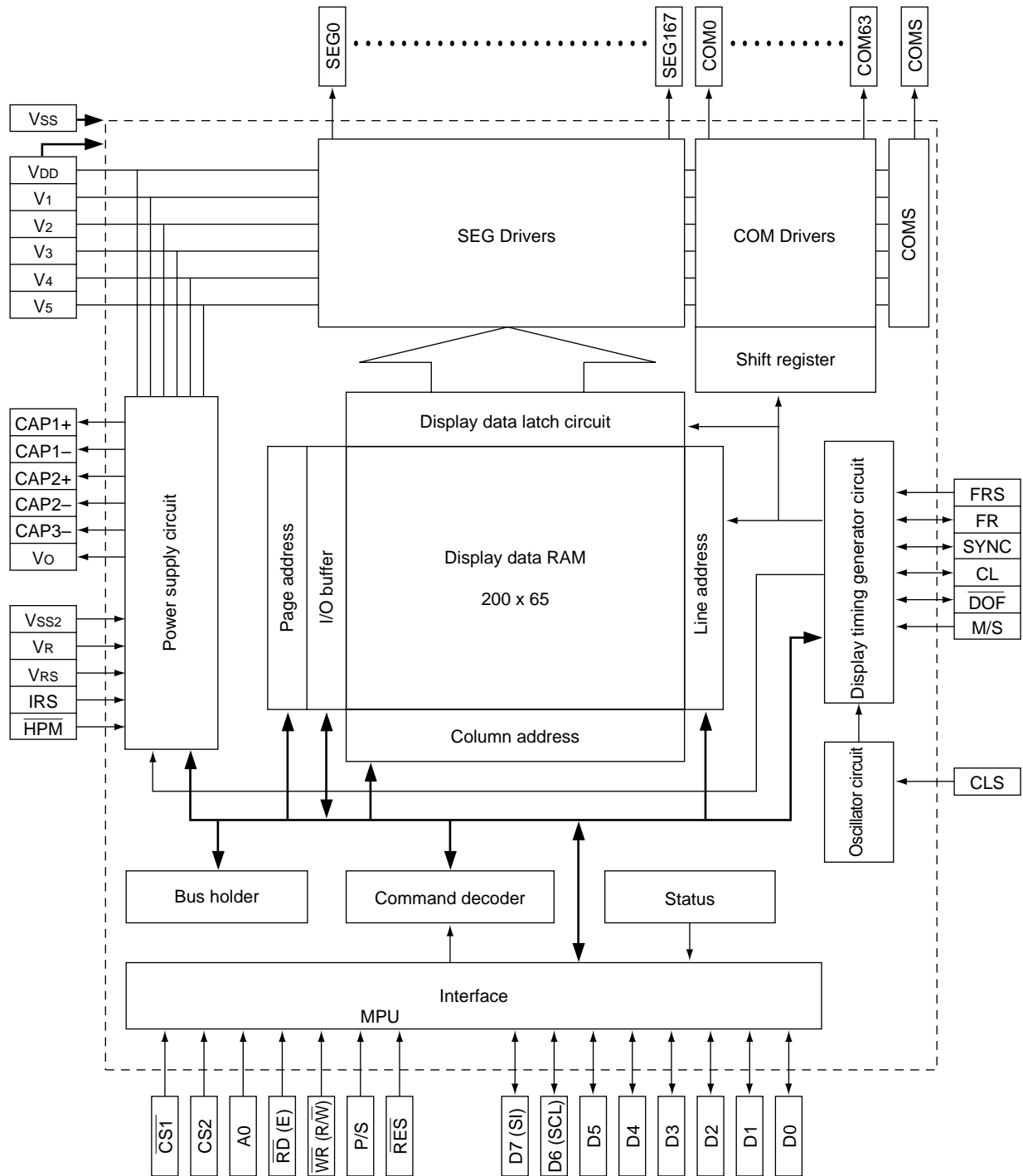
# SED1575 Series

- Built-in static drive circuit for indicators (One set, blinking speed variable)
- Built-in power supply circuit for low power supply liquid crystal drive  
Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- 3% high accuracy alternating current voltage adjusting circuit (Temperature gradient:  $-0.05\%/^{\circ}\text{C}$ )  
Built-in  $V_5$  voltage adjusting resistor, built-in  $V_1$  to  $V_4$  voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Ultra-low power consumption
- Power supplies  
Logic power supply:  $V_{DD} - V_{SS} = 2.4$  to  $3.6$  V  
(SED1575D3B, SED1577D3B)  
 $V_{DD} - V_{SS} = 3.6$  to  $5.5$  V  
(SED1575D0B, SED1577D0B)  
Boosting reference power supply:  $V_{DD} - V_{SS} = 1.8$  to  $6.0$  V  
Liquid crystal drive power supply:  $V_5 - V_{DD} = -4.5$  to  $-18.0$  V (SED1575\*\*)/ $-4.5$  to  $-16.0$  V (SED1577\*\*)
- Wide operating temperature range  $-40$  to  $85^{\circ}\text{C}$
- CMOS process
- Shipping forms : Bare chip, TCP
- No light-resistant and radiation-resistant design are provided.

## Series Specification

Product name	Voltage [V]	Duty	Bias	SEG Dr	COM Dr	VREG temperature gradient	Shipping form
SED1575D0B	$-3.6$ to $-5.5$	1/65	1/9, 1/7	168	65	$-0.05\%/^{\circ}\text{C}$	Bare chip
SED1575D3B	$-2.4$ to $-3.6$	1/65	1/9, 1/7	168	65	$-0.05\%/^{\circ}\text{C}$	Bare chip
SED1575T0A	$-3.6$ to $-5.5$	1/65	1/9, 1/7	168	65	$-0.05\%/^{\circ}\text{C}$	TCP
SED1575T3A	$-2.4$ to $-3.6$	1/65	1/9, 1/7	168	65	$-0.05\%/^{\circ}\text{C}$	TCP
SED1577D0B	$-3.6$ to $-5.5$	1/33	1/6, 1/5	200	33	$-0.05\%/^{\circ}\text{C}$	Bare chip
SED1577D3B	$-2.4$ to $-3.6$	1/33	1/6, 1/5	200	33	$-0.05\%/^{\circ}\text{C}$	Bare chip
SED1577T0*	$-3.6$ to $-5.5$	1/33	1/6, 1/5	200	33	$-0.05\%/^{\circ}\text{C}$	TCP
SED1577T3*	$-2.4$ to $-3.6$	1/33	1/6, 1/5	200	33	$-0.05\%/^{\circ}\text{C}$	TCP

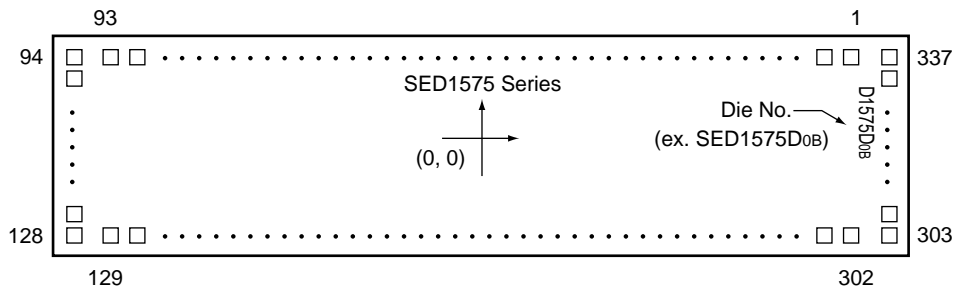
## ■ BLOCK DIAGRAM



# SED1575 Series

## ■ PIN ASSIGNMENT

### ● Chip Specification



Item	Size			Unit	
	X	Y			
Chip size	13.30	×	2.81	mm	
Chip thickness	0.625			mm	
Bump pitch	71 (Min.)			μm	
Bump size	PAD No.1 to 93	85	×	85	μm
	PAD No.94	85	×	73	μm
	PAD No.95 to 127	85	×	47	μm
	PAD No.128	85	×	73	μm
	PAD No.129	73	×	85	μm
	PAD No.130 to 301	47	×	85	μm
	PAD No.302	73	×	85	μm
	PAD No.303	86	×	73	μm
	PAD No.304 to 336	85	×	47	μm
PAD No.337	85	×	73	μm	
Bump height	17 (Typ.)			μm	

## ■ PIN DESCRIPTION

### ● Power Supply Pin

Pin name	I/O	Description	Number of pins																									
VDD	Power supply	Commonly used with the MPU power supply pin Vcc.	12																									
VSS	Power supply	0 V pin connected to the system ground (GND)	9																									
VSS2	Power supply	Boosting circuit reference power supply for liquid crystal drive	5																									
VRS	Power supply	External input pin for liquid crystal power supply voltage adjusting circuit They are set to OPEN	2																									
V1, V2 V3, V4 V5	Power supply	<p>Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied.</p> <p>The potential needs to be specified based on VDD to establish the relationship of dimensions shown below:</p> $V_{DD} (=V_0) \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ <p>Master operation When the power supply is ON, the following voltages are applied to V1 ~ V4 from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th colspan="2">SED1575*<sub>**</sub></th> <th colspan="2">SED1577*<sub>**</sub></th> </tr> </thead> <tbody> <tr> <td>V1</td> <td>1/9•V5</td> <td>1/7•V5</td> <td>1/6•V5</td> <td>1/5•V5</td> </tr> <tr> <td>V2</td> <td>2/9•V5</td> <td>2/7•V5</td> <td>2/6•V5</td> <td>2/5•V5</td> </tr> <tr> <td>V3</td> <td>7/9•V5</td> <td>5/7•V5</td> <td>4/6•V5</td> <td>3/5•V5</td> </tr> <tr> <td>V4</td> <td>8/9•V5</td> <td>6/7•V5</td> <td>5/6•V5</td> <td>4/5•V5</td> </tr> </tbody> </table>		SED1575* <sub>**</sub>		SED1577* <sub>**</sub>		V1	1/9•V5	1/7•V5	1/6•V5	1/5•V5	V2	2/9•V5	2/7•V5	2/6•V5	2/5•V5	V3	7/9•V5	5/7•V5	4/6•V5	3/5•V5	V4	8/9•V5	6/7•V5	5/6•V5	4/5•V5	10
	SED1575* <sub>**</sub>		SED1577* <sub>**</sub>																									
V1	1/9•V5	1/7•V5	1/6•V5	1/5•V5																								
V2	2/9•V5	2/7•V5	2/6•V5	2/5•V5																								
V3	7/9•V5	5/7•V5	4/6•V5	3/5•V5																								
V4	8/9•V5	6/7•V5	5/6•V5	4/5•V5																								

### ● LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.	2
CAP1–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
CAP2+	O	Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.	2
CAP2–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.	2
CAP3–	O	Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.	2
VOUT	O	Boosting output pin. Connects a capacitor between the pin and VSS2.	2
VR	I	Voltage adjusting pin. Applies voltage between VDD and V5 using a split resistor. Valid only when the V5 voltage adjusting built-in resistor is not used (IRS="L") Do not use VR when the V5 voltage adjusting built-in resistor is used (IRS="H")	1

# SED1575 Series

## ● System Bus Connecting Pins

Pin name	I/O	Description	Number of pins															
D7 to D0 (SI) (SCL)	I/O	An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), D7: Serial data entry pin (SI) D6: Serial clock input pin (SCL) In this case, D0 to D5 are set to high impedance. When Chip Select is in the non-active state, D0 to D7 are set to high impedance.	8															
A0	I	Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands. A0="H": Indicates that D0 to D7 are display data. A0="L": Indicates that D0 to D7 are control data.	1															
RES	I	Initialized by setting RES to "L". Reset operation is performed at the RES signal level.	1															
CS1 CS2	I	Chip Select signal. When CS1="L" and CS2="H", this signal becomes active and the input/output of data/commands is enabled.	2															
RD (E)	I	<ul style="list-style-type: none"> <li>When the 80 series MPU is connected, active "L" is set. Pin that connects the RD signal of the 80 series MPU. When this signal is "L", the SED1575 series data bus is set in the output state.</li> <li>When the 68 series MPU is connected, active "H" is set. 68 series MPU enable clock input pin</li> </ul>	1															
WR (R/W)	I	<ul style="list-style-type: none"> <li>When the 80 series MPU is connected, active "L" is set. Pin that connects the WR signal of the 80 series MPU. The data bus signal is latched on the leading edge of the WR signal.</li> <li>When the 68 series MPU is connected, Read/write control signal input pin R/W="H": Read operation R/W="L": Write operation</li> </ul>	1															
FRS	O	Output pin for static drive Used together with the SYNC pin	1															
C86	I	MPU interface switching pin C86="H": 68 series MPU interface C86="L": 80 series MPU interface	1															
P/S	I	<p>Switching pin for parallel data entry/serial data entry P/S="H": Parallel data entry P/S="L": Serial data entry According to the P/S state, the following table is given.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>P/S</th> <th>Data/command</th> <th>Data</th> <th>Read/write</th> <th>Serial clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>A0</td> <td>D0 to D7</td> <td>RD, WR</td> <td></td> </tr> <tr> <td>"L"</td> <td>A0</td> <td>SI (D7)</td> <td>Write-only</td> <td>SCL (D6)</td> </tr> </tbody> </table> <p>When P/S="L", D0 to D5 are set to high impedance. D0 to D5 can be "H", "L", or "OPEN". RD(E) and WR (R/W) are fixed to "H" or "L". For the serial data entry, RAM display data cannot be read.</p>	P/S	Data/command	Data	Read/write	Serial clock	"H"	A0	D0 to D7	RD, WR		"L"	A0	SI (D7)	Write-only	SCL (D6)	1
P/S	Data/command	Data	Read/write	Serial clock														
"H"	A0	D0 to D7	RD, WR															
"L"	A0	SI (D7)	Write-only	SCL (D6)														

# SED1575 Series

Pin name	I/O	Description	Number of pins																																													
CLS	I	<p>Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks.</p> <p>CLS="H": Built-in oscillator circuit valid  CLS="L": Built-in oscillator circuit invalid (external input)</p> <p>When CLS="L", display clocks are input from the CL pin.</p> <p>When the SED1575 series is used for the master/slave configuration, each of the CLS pins is set to the same level together.</p> <table border="1"> <thead> <tr> <th>Display clock</th> <th>Master</th> <th>Slave</th> </tr> </thead> <tbody> <tr> <td>Built-in oscillator circuit used</td> <td>"H"</td> <td>"H"</td> </tr> <tr> <td>External input</td> <td>"L"</td> <td>"L"</td> </tr> </tbody> </table>	Display clock	Master	Slave	Built-in oscillator circuit used	"H"	"H"	External input	"L"	"L"	1																																				
Display clock	Master	Slave																																														
Built-in oscillator circuit used	"H"	"H"																																														
External input	"L"	"L"																																														
M/S	I	<p>Pin that selects the master/slave operation for the SED1575 series.</p> <p>The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation.</p> <p>M/S="H": Master operation  M/S="L": Slave operation</p> <p>According to the M/S and CLS states, the following table is given.</p> <table border="1"> <thead> <tr> <th>M/S</th> <th>CLS</th> <th>Oscillator circuit</th> <th>Power supply circuit</th> <th>CL</th> <th>FR</th> <th>SYNC</th> <th>FRS</th> <th>DOF</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>"H"</td> <td>Valid</td> <td>Valid</td> <td>Output</td> <td>Output</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>"H"</td> <td>"L"</td> <td>Invalid</td> <td>Valid</td> <td>Input</td> <td>Output</td> <td>Output</td> <td>Output</td> <td>Output</td> </tr> <tr> <td>"L"</td> <td>"H"</td> <td>Invalid</td> <td>Invalid</td> <td>Input</td> <td>Input</td> <td>Input</td> <td>Output</td> <td>Input</td> </tr> <tr> <td>"L"</td> <td>"L"</td> <td>Invalid</td> <td>Invalid</td> <td>Input</td> <td>Input</td> <td>Input</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table>	M/S	CLS	Oscillator circuit	Power supply circuit	CL	FR	SYNC	FRS	DOF	"H"	"H"	Valid	Valid	Output	Output	Output	Output	Output	"H"	"L"	Invalid	Valid	Input	Output	Output	Output	Output	"L"	"H"	Invalid	Invalid	Input	Input	Input	Output	Input	"L"	"L"	Invalid	Invalid	Input	Input	Input	Output	Input	1
M/S	CLS	Oscillator circuit	Power supply circuit	CL	FR	SYNC	FRS	DOF																																								
"H"	"H"	Valid	Valid	Output	Output	Output	Output	Output																																								
"H"	"L"	Invalid	Valid	Input	Output	Output	Output	Output																																								
"L"	"H"	Invalid	Invalid	Input	Input	Input	Output	Input																																								
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CL	I/O	<p>Display clock I/O pin</p> <p>According to the M/S and CLS states, the following table is given.</p> <table border="1"> <thead> <tr> <th>M/S</th> <th>CLS</th> <th>CL</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>"H"</td> <td>Output</td> </tr> <tr> <td>"H"</td> <td>"L"</td> <td>Input</td> </tr> <tr> <td>"L"</td> <td>"H"</td> <td>Input</td> </tr> <tr> <td>"L"</td> <td>"L"</td> <td>Input</td> </tr> </tbody> </table> <p>When the SED1575 series is used for the master/slave configuration, each CL pin is connected.</p>	M/S	CLS	CL	"H"	"H"	Output	"H"	"L"	Input	"L"	"H"	Input	"L"	"L"	Input	1																														
M/S	CLS	CL																																														
"H"	"H"	Output																																														
"H"	"L"	Input																																														
"L"	"H"	Input																																														
"L"	"L"	Input																																														
FR	I/O	<p>Liquid crystal alternating current signal I/O pin</p> <p>M/S="H": Output  M/S="L": Input</p> <p>When the SED1575 series is used for the master/slave configuration, each FR pin is connected.</p>	1																																													
SYNC	I/O	<p>Liquid crystal synchronizing current signal I/O pin</p> <p>M/S="H": Output  M/S="L": Input</p> <p>When the SED1575 series is used for the master/slave configuration, each SYNC pin is connected.</p>	2																																													
DOF	I/O	<p>Liquid crystal display blanking control pin</p> <p>M/S="H": Output  M/S="L": Input</p> <p>When the SED1575 series is used for the master/slave configuration, each DOF pin is connected.</p>	1																																													
IRS	I	<p>V<sub>5</sub> voltage adjusting resistor selection pin</p> <p>IRS="H": Built-in resistor used  IRS="L": Built-in resistor not used. The V<sub>5</sub> voltage is adjusted by the VR pin and stand-alone split resistor.</p> <p>Valid only at master operation. The pin is fixed to "H" or "L" at slave operation.</p>	1																																													
HPM	I	<p>Power supply control pin of the power supply circuit for liquid crystal drive</p> <p>HPM="H": Normal mode  HPM="L": High power supply mode</p> <p>Valid only at master operation. The pin is fixed to "H" or "L" at slave operation.</p>	1																																													

# SED1575 Series

## ● Liquid Crystal Drive Pin

Pin name	I/O	Description	Number of pins																																			
SEG0 to SEGn	O	<p>Output pins for the LCD segment drive. For the pin assignment by model, refer to the table below.</p> <table border="1"> <thead> <tr> <th>Product name</th> <th>SEG</th> <th>Number of pins</th> </tr> </thead> <tbody> <tr> <td>SED1575**</td> <td>SEG0 to SEG167</td> <td>168</td> </tr> <tr> <td>SED1577**</td> <td>SEG0 to SEG199</td> <td>200</td> </tr> </tbody> </table> <p>Contents of the display RAM and FR signal are combined to select a desired level among VDD, V2, V3 and V5.</p> <table border="1"> <thead> <tr> <th rowspan="2">RAM data</th> <th rowspan="2">FR</th> <th colspan="2">Output voltage</th> </tr> <tr> <th>Display normal operation</th> <th>Display reversal</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>VDD</td> <td>V2</td> </tr> <tr> <td>H</td> <td>L</td> <td>V5</td> <td>V3</td> </tr> <tr> <td>L</td> <td>H</td> <td>V2</td> <td>VDD</td> </tr> <tr> <td>L</td> <td>L</td> <td>V3</td> <td>V5</td> </tr> <tr> <td>Power save</td> <td>—</td> <td colspan="2">VDD</td> </tr> </tbody> </table>	Product name	SEG	Number of pins	SED1575**	SEG0 to SEG167	168	SED1577**	SEG0 to SEG199	200	RAM data	FR	Output voltage		Display normal operation	Display reversal	H	H	VDD	V2	H	L	V5	V3	L	H	V2	VDD	L	L	V3	V5	Power save	—	VDD		168 or 200
Product name	SEG	Number of pins																																				
SED1575**	SEG0 to SEG167	168																																				
SED1577**	SEG0 to SEG199	200																																				
RAM data	FR	Output voltage																																				
		Display normal operation	Display reversal																																			
H	H	VDD	V2																																			
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Power save	—	VDD																																				
COM0 to COMn		<p>Output pins for the LCD common drive. For the pin assignment by model, refer to the table below.</p> <table border="1"> <thead> <tr> <th>Product name</th> <th>SEG</th> <th>Number of pins</th> </tr> </thead> <tbody> <tr> <td>SED1575**</td> <td>COM0 to COM63</td> <td>64</td> </tr> <tr> <td>SED1577**</td> <td>COM0 to COM31</td> <td>32</td> </tr> </tbody> </table> <p>Scan data and FR signal are combined to select a desired level among VDD, V1, V4 and V5.</p> <table border="1"> <thead> <tr> <th>Scanning data</th> <th>FR</th> <th>Output voltage</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>V5</td> </tr> <tr> <td>H</td> <td>L</td> <td>VDD</td> </tr> <tr> <td>L</td> <td>H</td> <td>V1</td> </tr> <tr> <td>L</td> <td>L</td> <td>V4</td> </tr> <tr> <td>Power save</td> <td>—</td> <td>VDD</td> </tr> </tbody> </table>	Product name	SEG	Number of pins	SED1575**	COM0 to COM63	64	SED1577**	COM0 to COM31	32	Scanning data	FR	Output voltage	H	H	V5	H	L	VDD	L	H	V1	L	L	V4	Power save	—	VDD	64 or 32								
Product name	SEG	Number of pins																																				
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H	L	VDD																																				
L	H	V1																																				
L	L	V4																																				
Power save	—	VDD																																				
COMS	O	<p>Indicator dedicated COM output pin Set to OPEN when not used When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.</p>	2																																			

## ● Test Pin

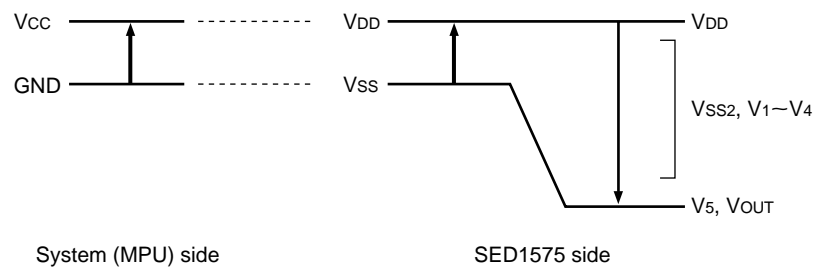
Pin name	I/O	Description	Number of pins
TEST1 to 6	I/O	IC chip test pin. Fix the pin to "H".	6
TEST7 to 9	I/O	IC chip test pin. Take into consideration so that the capacity of lines cannot be exhausted by setting the pin to OPEN.	3



## ■ ABSOLUTE MAXIMUM RATINGS

VSS=0V unless specified otherwise

Item		Symbol	Specification value			Unit
Power supply voltage		VDD	-0.3	to	+7.0	V
Power supply voltage (2) (Based on VDD)	At triple boosting	VSS2	-7.0	to	+0.3	
	At quadruple boosting		-6.0	to	+0.3	
			-4.5	to	+0.3	
Power supply voltage (3) (Based on VDD)		V5, VOUT	-20.0	to	+0.3	
Power supply voltage (4) (Based on VDD)		V1, V2, V3, V4	V5	to	+0.3	
Input voltage		VIN	-0.3	to	VDD+0.3	
Output voltage		VOUT	-0.3	to	VDD+0.3	
Operating temperature		TOPR	-40	to	+85	°C
Storage temperature	TCP	TSTR	-55	to	+100	
	Bare chip		-55	to	+125	



- Notes: 1. The values of the VSS2, V1 to V5, and V<sub>O</sub> voltages are based on VDD=0 V.  
 2. The V1, V2, V3, and V4 voltages must always satisfy the condition of  $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ .  
 3. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

# SED1575 Series

## ■ DC CHARACTERISTICS

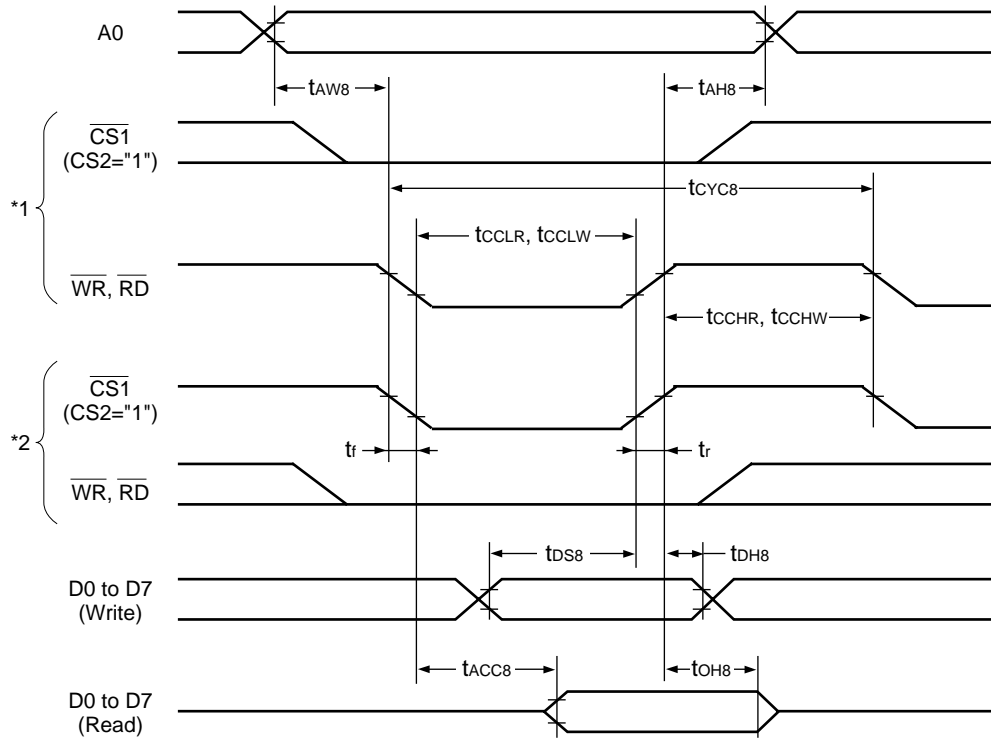
Unless otherwise specified, V<sub>SS</sub>=0 V, T<sub>a</sub>=-40 to 85°C

Item	Symbol	Condition	Specification value			Unit	Applicable pin
			Min.	Typ.	Max.		
Operating voltage (1)	V <sub>DD</sub>	SED1575*3*/SED1577*3*	2.4	—	3.6	V	V <sub>DD</sub>
	V <sub>DD</sub>	SED1575*0*/SED1577*0*	3.6	—	5.5		V <sub>DD</sub>
Operating voltage (2)	V <sub>SS2</sub>	(Based on V <sub>DD</sub> )	-6.0	—	-1.8		V <sub>SS2</sub>
Operating voltage (3)	V <sub>5</sub>	SED1575*** (Based on V <sub>DD</sub> )	-18.0	—	-4.5		V <sub>5</sub>
	V <sub>5</sub>	SED1577*** (Based on V <sub>DD</sub> )	-16.0	—	-4.5		V <sub>5</sub>
	V <sub>1</sub> , V <sub>2</sub>	(Based on V <sub>DD</sub> )	0.4×V <sub>5</sub>	—	V <sub>DD</sub>		V <sub>1</sub> , V <sub>2</sub>
	V <sub>3</sub> , V <sub>4</sub>	(Based on V <sub>DD</sub> )	V <sub>5</sub>	—	0.6×V <sub>5</sub>	V <sub>3</sub> , V <sub>4</sub>	
High level input voltage	V <sub>IHC</sub>		0.8×V <sub>DD</sub>	—	V <sub>DD</sub>		
Low level input voltage	V <sub>ILC</sub>		V <sub>SS</sub>	—	0.2×V <sub>DD</sub>		
High level output voltage	V <sub>OHC</sub>	I <sub>OH</sub> =-0.5mA	0.8×V <sub>DD</sub>	—	V <sub>DD</sub>		
Low level output voltage	V <sub>OLC</sub>	I <sub>OL</sub> =0.5mA	V <sub>SS</sub>	—	0.2×V <sub>DD</sub>		
Input leak current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub>	-1.0	—	1.0	μA	
Output leak current	I <sub>LO</sub>		-3.0	—	3.0		
Liquid crystal driver On resistance	R <sub>ON</sub>	T <sub>a</sub> =25°C	—	2.0	3.5	KΩ	SE <sub>Gn</sub> COM <sub>n</sub>
		(Based on V <sub>DD</sub> )	—	3.2	5.4		
Static current consumption	I <sub>SSQ</sub>		—	0.01	5	μA	V <sub>SS</sub> , V <sub>SS2</sub> V <sub>5</sub>
Output leak current	I <sub>SQ</sub>	V <sub>5</sub> =-18.0V (Based on V <sub>DD</sub> )	—	0.01	15		
Input pin capacity	C <sub>IN</sub>	T <sub>a</sub> =25°C, f=1MHz	—	5.0	8.0	pF	
Oscillating frequency	Built-in oscillation	f <sub>OSC</sub>	T <sub>a</sub> =25°C	18	22	kHz	CL
	External input	f <sub>CL</sub>		4.5	5.5		

Item	Symbol	Condition	Specification value			Unit	Applicable pin	
			Min.	Typ.	Max.			
Built-in power supply circuit	Input voltage	V <sub>SS2</sub>	At triple boosting (Based on V <sub>DD</sub> )	-6.0	—	-1.8	V	V <sub>SS2</sub>
		V <sub>SS2</sub>	At quadruple boosting (Based on V <sub>DD</sub> )	-4.5	—	-1.8		V <sub>SS2</sub>
	Boosting output voltage	V <sub>OUT</sub>	(Based on V <sub>DD</sub> )	-20.0	—	—	V <sub>OUT</sub>	
	Voltage adjusting circuit operating voltage	V <sub>OUT</sub>	(Based on V <sub>DD</sub> )	-20.0	—	-6.0	V <sub>OUT</sub>	
	V/F circuit operating voltage	V <sub>5</sub>	SED1575*** (Based on V <sub>DD</sub> )	-18.0	—	-4.5	V <sub>5</sub>	
		V <sub>5</sub>	SED1577*** (Based on V <sub>DD</sub> )	-16.0	—	-4.5	V <sub>5</sub>	
Reference voltage	V <sub>REG0</sub>	T <sub>a</sub> =25°C, -0.05%/°C	-2.04	-2.10	-2.16			

## ■ TIMING CHARACTERISTICS

### ● System bus read/write characteristics 1 (80 series MPU)

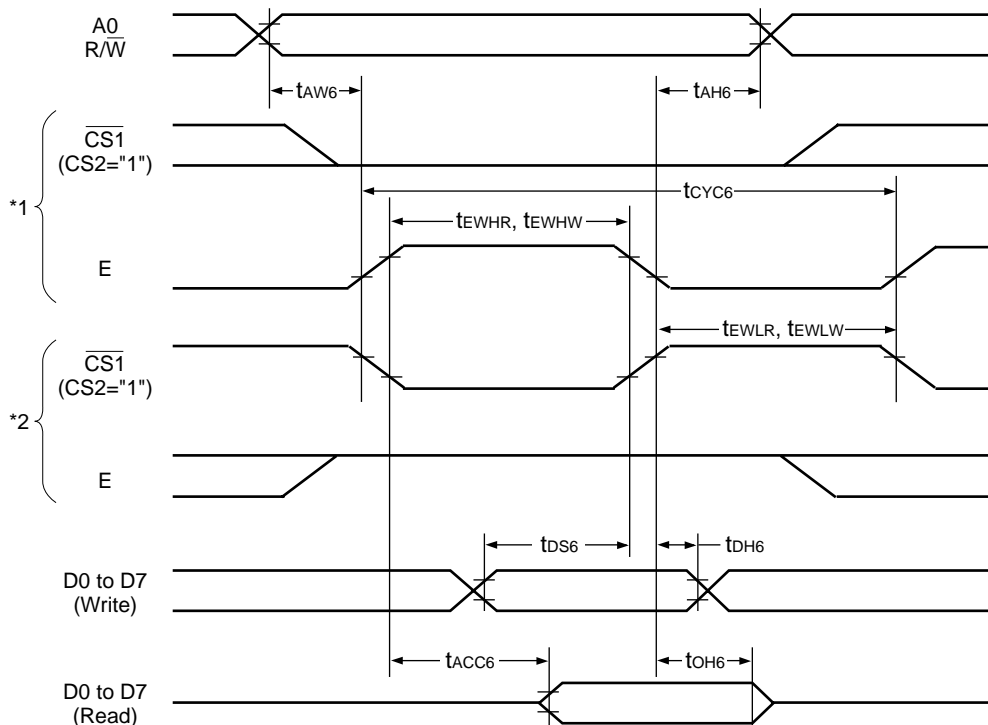


[SED1575\*0\*, SED1577\*0\*: VDD=4.5V to 5.5V, Ta=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		250	—	
Control L pulse width ( $\overline{WR}$ )	$\overline{WR}$	tcCLW		30	—	
Control L pulse width ( $\overline{RD}$ )	$\overline{RD}$	tcCLR		70	—	
Control H pulse width ( $\overline{WR}$ )	$\overline{WR}$	tcCHW		30	—	
Control H pulse width ( $\overline{RD}$ )	$\overline{RD}$	tcCHR		30	—	
Data setup time	D0 to D7	tDS8		30	—	
Data hold time		tDH8		10	—	
$\overline{RD}$ access time		tACC8	CL=100pF	—	70	
Output disable time		tOH8		5	50	

# SED1575 Series

## ● System bus read/write characteristics 2 (68 series MPU)



[SED1575\*0\*, SED1577\*0\*: V<sub>DD</sub>=4.5V to 5.5V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		0	—	ns
Address setup time		t <sub>AW6</sub>		0	—	
System cycle time		t <sub>CYC6</sub>		250	—	
Data setup time	D0 to D7	t <sub>DS6</sub>		30	—	
Data hold time		t <sub>DH6</sub>		10	—	
Access time		t <sub>ACC6</sub>	CL=100pF	—	70	
Output disable time		t <sub>OH6</sub>		5	50	
Enable H pulse width	Read	E	t <sub>EWHR</sub>	70	—	
	Write		t <sub>EWHW</sub>	30	—	
Enable L pulse width	Read	E	t <sub>EWLR</sub>	30	—	
	Write		t <sub>EWLW</sub>	30	—	

# SED1575 Series

[SED1575\*0\*, SED1577\*0\*: V<sub>DD</sub>=3.6V to 4.5V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		0	—	ns
Address setup time		t <sub>AW6</sub>		0	—	
System cycle time		t <sub>CYC6</sub>		300	—	
Data setup time	D0 to D7	t <sub>DS6</sub>		40	—	
Data hold time		t <sub>DH6</sub>		15	—	
Access time		t <sub>ACC6</sub>	CL=100pF	—	140	
Output disable time		t <sub>OH6</sub>		10	100	
Enable H pulse width	Read Write	E	t <sub>EWHR</sub>	120	—	
			t <sub>EWHW</sub>	60	—	
Enable L pulse width	Read Write	E	t <sub>EWLR</sub>	60	—	
			t <sub>EWLW</sub>	60	—	

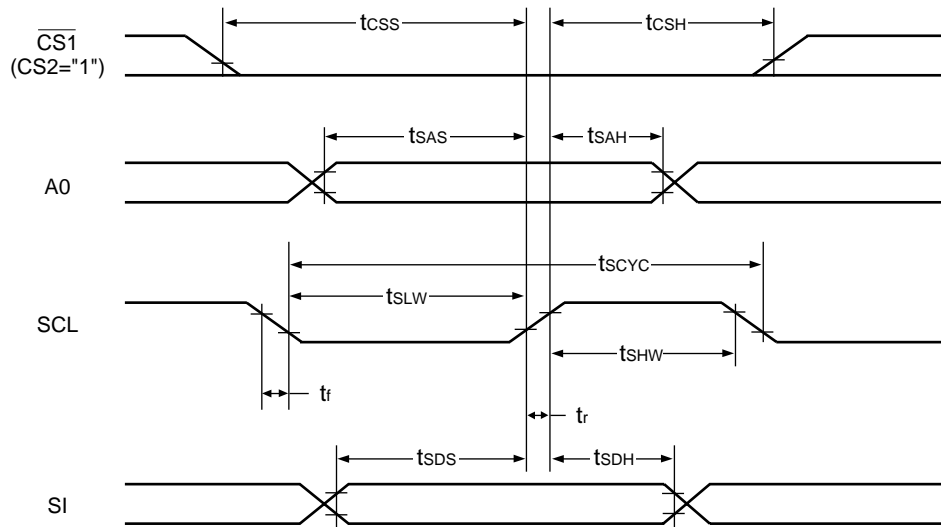
[SED1575\*3\*, SED1577\*3\*: V<sub>DD</sub>=2.4V to 3.6V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t <sub>AH6</sub>		0	—	ns
Address setup time		t <sub>AW6</sub>		0	—	
System cycle time		t <sub>CYC6</sub>		800	—	
Data setup time	D0 to D7	t <sub>DS6</sub>		80	—	
Data hold time		t <sub>DH6</sub>		30	—	
Access time		t <sub>ACC6</sub>	CL=100pF	—	280	
Output disable time		t <sub>OH6</sub>		10	200	
Enable H pulse width	Read Write	E	t <sub>EWHR</sub>	240	—	
			t <sub>EWHW</sub>	120	—	
Enable L pulse width	Read Write	E	t <sub>EWLR</sub>	120	—	
			t <sub>EWLW</sub>	120	—	

- Notes: 1. The rise and fall times (t<sub>r</sub> and t<sub>f</sub>) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t<sub>r</sub>+t<sub>f</sub>) ≤ (t<sub>CYC6</sub>-t<sub>EWLW</sub>-t<sub>EWHW</sub>) or (t<sub>r</sub>+t<sub>f</sub>) ≤ (t<sub>CYC6</sub>-t<sub>EWLR</sub>-t<sub>EWHR</sub>).
2. All timings are specified based on the 20 and 80% of V<sub>DD</sub>.
3. t<sub>EWLW</sub> and t<sub>EWLR</sub> are specified for the overlap period when CS1 is at "L" (CS2= "H") level and E is at the "H" level.

# SED1575 Series

## ● Serial interface



[SED1575\*0\*, SED1577\*0\*:  $V_{DD}=4.5V$  to  $5.5V$ ,  $T_a=-40$  to  $85^{\circ}C$ ]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	$t_{SCYC}$		200	—	ns
SCL "H" pulse width		$t_{SHW}$		75	—	
SCL "L" pulse width		$t_{SLW}$		75	—	
Address setup time	A0	$t_{SAS}$		50	—	
Address hold time		$t_{SAH}$		100	—	
Data setup time	SI	$t_{SDS}$		50	—	
Data hold time		$t_{SDH}$		50	—	
CS-SCL time	CS	$t_{CSS}$		100	—	
		$t_{CSH}$		100	—	

# SED1575 Series

[SED1575\*0\*, SED1577\*0\*: V<sub>DD</sub>=3.6V to 4.5V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	tSCYC		250	—	ns
SCL "H" pulse width		tSHW		100	—	
SCL "L" pulse width		tSLW		100	—	
Address setup time	A0	tSAS		150	—	
Address hold time		tSAH		150	—	
Data setup time	SI	tSDS		100	—	
Data hold time		tSDH		100	—	
CS-SCL time	CS	tCSS		150	—	
		tCSH		150	—	

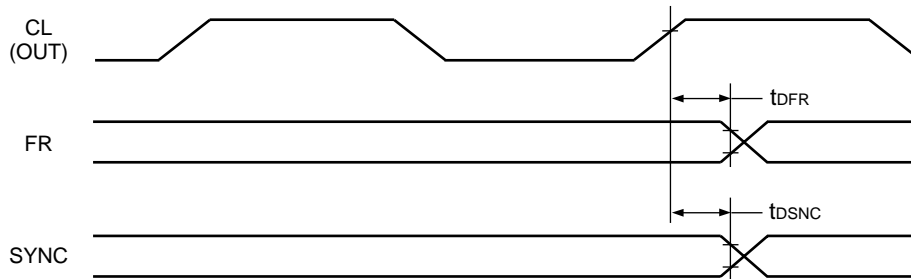
[SED1575\*3\*, SED1577\*3\*: V<sub>DD</sub>=2.4V to 3.6V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	tSCYC		400	—	ns
SCL "H" pulse width		tSHW		150	—	
SCL "L" pulse width		tSLW		150	—	
Address setup time	A0	tSAS		250	—	
Address hold time		tSAH		250	—	
Data setup time	SI	tSDS		150	—	
Data hold time		tSDH		150	—	
CS-SCL time	CS	tCSS		250	—	
		tCSH		250	—	

- Notes: 1. The rise and fall times (t<sub>r</sub> and t<sub>f</sub>) of the input signal are specified for less than 15 ns.  
 2. All timings are specified based on the 20 and 80% of V<sub>DD</sub>.

# SED1575 Series

## ● Display control output timing



[SED1575\*0\*, SED1577\*0\*:  $V_{DD}=4.5V$  to  $5.5V$ ,  $T_a=-40$  to  $85^{\circ}C$ ]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	$t_{DFR}$	$C_L=50pF$	—	10	40	ns
SYNC delay time	SYNC	$t_{DSNC}$	$C_L=50pF$	—	10	40	ns

[SED1575\*0\*, SED1577\*0\*:  $V_{DD}=3.6V$  to  $4.5V$ ,  $T_a=-40$  to  $85^{\circ}C$ ]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	$t_{DFR}$	$C_L=50pF$	—	20	80	ns
SYNC delay time	SYNC	$t_{DSNC}$	$C_L=50pF$	—	20	80	ns

[SED1575\*3\*, SED1577\*3\*:  $V_{DD}=2.4V$  to  $3.6V$ ,  $T_a=-40$  to  $85^{\circ}C$ ]

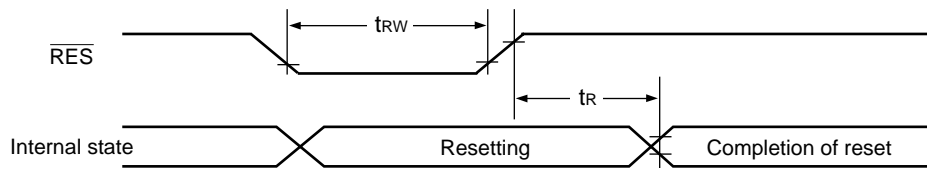
Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	$t_{DFR}$	$C_L=50pF$	—	50	200	ns
SYNC delay time	SYNC	$t_{DSNC}$	$C_L=50pF$	—	50	200	ns

- Notes: 1. Valid only when the master mode is selected.  
 2. All timings are specified based on the 20 and 80% of  $V_{DD}$ .  
 3. Pay attention not to cause delays of the timing signals CL, FR and SYNC to the salve side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.



# SED1575 Series

## ● Reset input timing



[SED1575\*0\*, SED1577\*0\*: V<sub>DD</sub>=4.5V to 5.5V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t <sub>R</sub>		—	—	0.5	μs
Reset "L" pulse width	RES	t <sub>RW</sub>		0.5	—	—	

[SED1575\*0\*, SED1577\*0\*: V<sub>DD</sub>=3.6V to 4.5V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t <sub>R</sub>		—	—	1	μs
Reset "L" pulse width	RES	t <sub>RW</sub>		1	—	—	

[SED1575\*3\*, SED1577\*3\*: V<sub>DD</sub>=2.4V to 3.6V, T<sub>a</sub>=-40 to 85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t <sub>R</sub>		—	—	1.5	μs
Reset "L" pulse width	RES	t <sub>RW</sub>		1.5	—	—	

Note: All timings are specified based on the 20 and 80% of V<sub>DD</sub>.

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