

## ANY-RATE I<sup>2</sup>C PROGRAMMABLE XO/VCXO

### Features

- Any-rate programmable output frequencies from 10 to 945 MHz and select frequencies to 1.4 GHz
- I<sup>2</sup>C serial interface
- 3rd generation DSPLL<sup>®</sup> with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available LVPECL, CMOS, LVDS, and CML outputs
- Industry-standard 5x7 mm package
- Pb-free/RoHS-compliant
- 1.8, 2.5, or 3.3 V supply

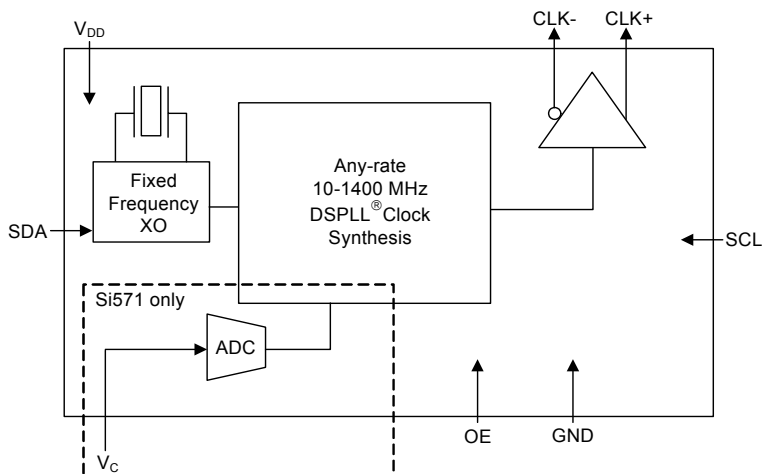
### Applications

- SONET / SDH
- xDSL
- 10 GbE LAN / WAN
- Low-jitter clock generation
- Optical modules
- Clock and data recovery

### Description

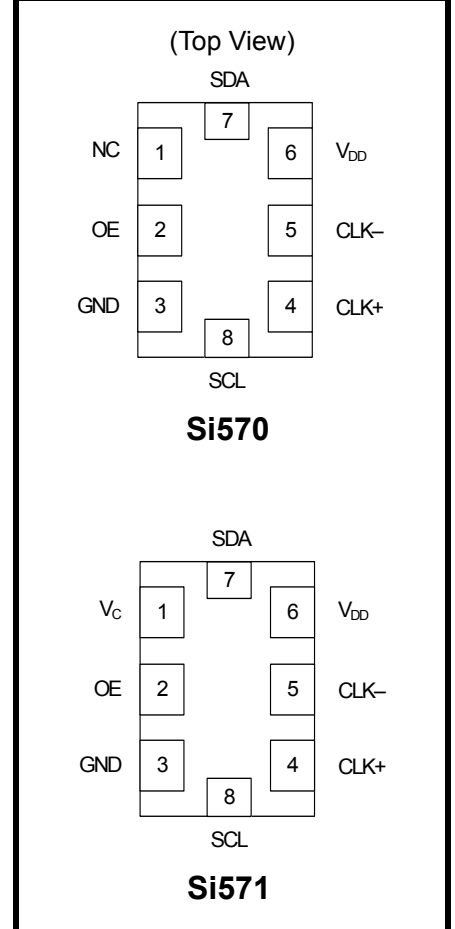
The Si570 XO/Si571 VCXO utilizes Silicon Laboratories' advanced DSPLL<sup>®</sup> circuitry to provide a low-jitter clock at any frequency. The Si570/Si571 are user-programmable to any output frequency from 10 to 945 MHz and select frequencies to 1400 MHz with <1 ppb resolution. The device is programmed via an I<sup>2</sup>C serial interface. Unlike traditional XO/VCXOs where a different crystal is required for each output frequency, the Si57x uses one fixed-frequency crystal and a DSPLL clock synthesis IC to provide any-rate frequency operation. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low-jitter clocks in noisy environments typically found in communication systems.

### Functional Block Diagram



**Ordering Information:**  
See page 21.

**Pin Assignments:**  
See page 20.



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## 1. Detailed Block Diagrams

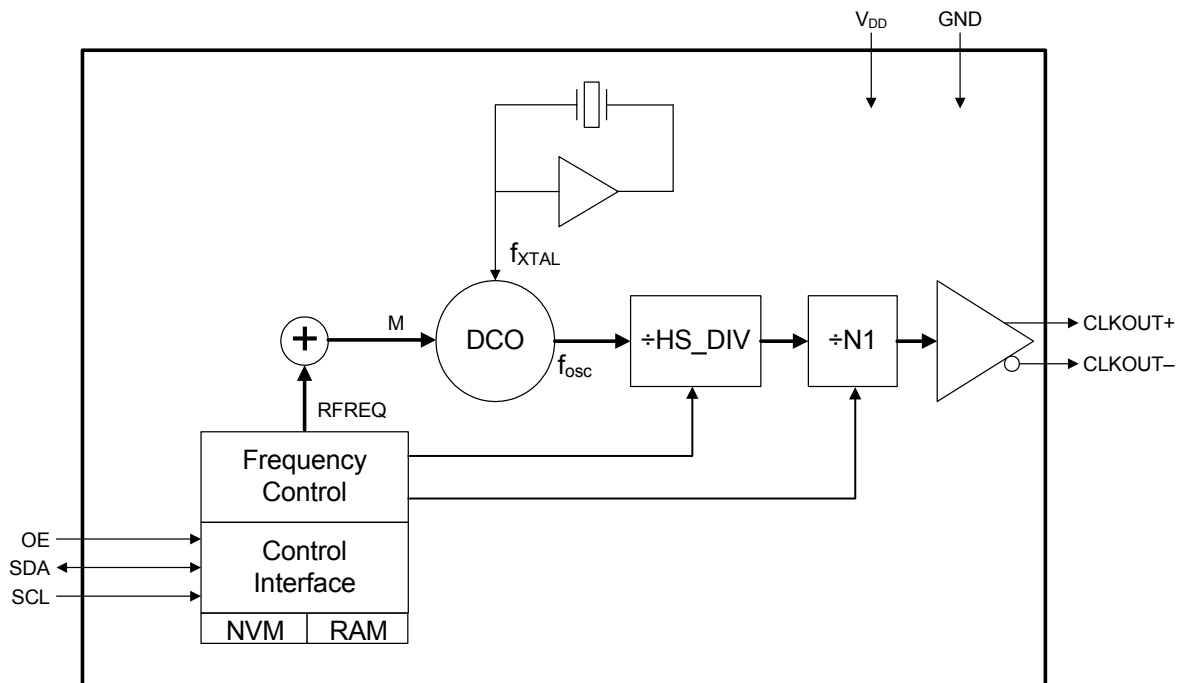


Figure 1. Si570 Detailed Block Diagram

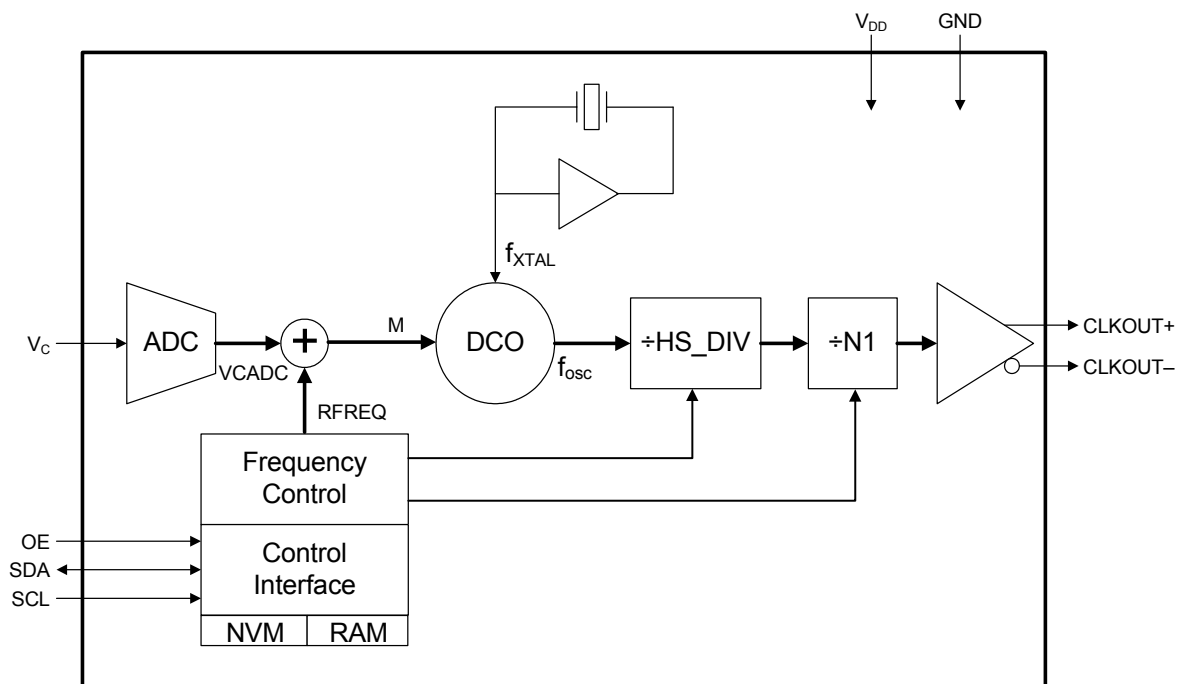


Figure 2. Si571 Detailed Block Diagram

## 2. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage <sup>1</sup>	V <sub>DD</sub>	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I <sub>DD</sub>	Output enabled LVPECL	—	120	130	mA
		CML	—	108	117	
		LVDS	—	99	108	
		CMOS	—	90	98	
		TriState mode	—	60	75	
Output Enable (OE) <sup>2</sup>		V <sub>IH</sub>	0.75 x V <sub>DD</sub>	—	—	V
		V <sub>IL</sub>	—	—	0.5	
Operating Temperature Range	T <sub>A</sub>		–40	—	85	°C

**Notes:**

1. Selectable parameter specified by part number. See Section "7. Ordering Information" on page 21 for further details.
2. OE pin includes a 17 kΩ pullup resistor to V<sub>DD</sub> or a 17 kΩ pulldown to GND depending on the OE polarity specified in the part number. See "7. Ordering Information" on page 21.

**Table 2. V<sub>C</sub> Control Voltage Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope <sup>1,2,3</sup>	K <sub>V</sub>	V <sub>C</sub> 10 to 90% of V <sub>DD</sub>	—	33	—	ppm/V
				45		
				90		
				135		
				180		
Control Voltage Linearity <sup>4</sup>	L <sub>VC</sub>	BSL	–5	±1	+5	%
		Incremental	–10	±5	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V <sub>C</sub> Input Impedance	Z <sub>VC</sub>		500	—	—	kΩ
Nominal Control Voltage	V <sub>CNOM</sub>	@ f <sub>O</sub>	—	V <sub>DD</sub> /2	—	V
Control Voltage Tuning Range	V <sub>C</sub>		0		V <sub>DD</sub>	V

**Notes:**

1. Positive slope; selectable option by part number. See "7. Ordering Information" on page 21.
2. For best jitter and phase noise performance, always choose the smallest K<sub>V</sub> that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K<sub>V</sub>), Stability, and Absolute Pull Range (APR)" for more information.
3. K<sub>V</sub> variation is ±10% of typical values.
4. BSL determined from deviation from best straight line fit with V<sub>C</sub> ranging from 10 to 90% of V<sub>DD</sub>. Incremental slope determined with V<sub>C</sub> ranging from 10 to 90% of V<sub>DD</sub>.

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**Table 3. CLK± Output Frequency Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Programmable Frequency Range <sup>1,2,3</sup>	f <sub>0</sub>	LVPECL/LVDS/CML	10	—	945	MHz
		CMOS	10	—	160	
Temperature Stability <sup>1,4</sup>		T <sub>A</sub> = -40 to +85 °C	-20	—	+20	ppm
			-50	—	+50	
			-100	—	+100	
Aging	f <sub>a</sub>	Frequency drift over first year	—	—	±3	ppm
		Frequency drift over 15 year life	—	—	±10	ppm
Total Stability		Temp stability = ±20 ppm	—	—	±31.5	ppm
		Temp stability = ±50 ppm	—	—	±61.5	ppm
Absolute Pull Range <sup>1,4</sup>	APR		±25	—	±375	ppm
Power up Time <sup>5</sup>	t <sub>OSC</sub>		—	—	10	ms
Settling Time after Frequency Change	t <sub>FRQ</sub>	f <sub>1</sub> within ±100 ppm of f <sub>0</sub>	—	—	100	µs
		f <sub>1</sub> > ±100 ppm of f <sub>0</sub>	—	—	10	ms

**Notes:**

1. See Section "7. Ordering Information" on page 21 for further details.
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
3. Nominal output frequency set by V<sub>CNOM</sub> = 1/2 x V<sub>DD</sub>.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to f<sub>0</sub>.

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option <sup>1</sup>	V <sub>O</sub>	mid-level	V <sub>DD</sub> - 1.42	—	V <sub>DD</sub> - 1.25	V
	V <sub>OD</sub>	swing (diff)	1.1	—	1.9	V <sub>PP</sub>
	V <sub>SE</sub>	swing (single-ended)	0.55	—	0.95	V <sub>PP</sub>
LVDS Output Option <sup>2</sup>	V <sub>O</sub>	mid-level	1.125	1.20	1.275	V
	V <sub>OD</sub>	swing (diff)	0.5	0.7	0.9	V <sub>PP</sub>
CML Output Option <sup>2</sup>	V <sub>O</sub>	mid-level	—	V <sub>DD</sub> - 0.75	—	V
	V <sub>OD</sub>	swing (diff)	0.70	0.95	1.20	V <sub>PP</sub>
CMOS Output Option <sup>3</sup>	V <sub>OH</sub>	I <sub>OH</sub> = 32 mA	0.8 x V <sub>DD</sub>	—	V <sub>DD</sub>	V
	V <sub>OL</sub>	I <sub>OL</sub> = 32 mA	—	—	0.4	
Rise/Fall time (20/80%)	t <sub>R</sub> , t <sub>F</sub>	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C <sub>L</sub> = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V <sub>DD</sub> - 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V <sub>DD</sub> /2	45	—	55	%

**Notes:**

1. 50 Ω to V<sub>DD</sub> - 2.0 V.
2. R<sub>term</sub> = 100 Ω (differential).
3. C<sub>L</sub> = 15 pF

Table 5. CLK± Output Phase Jitter (Si570)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)* for F <sub>OUT</sub> ≥ 500 MHz	ϕ <sub>J</sub>	12 kHz to 20 MHz (OC-48)	—	0.25	0.40	ps
		50 kHz to 80 MHz (OC-192)	—	0.26	0.37	
Phase Jitter (RMS)* for F <sub>OUT</sub> of 125 to 500 MHz	ϕ <sub>J</sub>	12 kHz to 20 MHz (OC-48)	—	0.36	0.50	ps
		50 kHz to 20 MHz (OC-192)	—	0.34	0.42	

**\*Note:** Differential Modes: LVPECL/LVDS/CML. Refer to AN256 for further information.

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**Table 6. CLK± Output Phase Jitter (Si571)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) <sup>1,2,3</sup> for F <sub>OUT</sub> ≥ 500 MHz	$\phi_J$	Kv = 33 ppm/V	—	—	—	ps
		12 kHz to 20 MHz (OC-48)	—	0.26	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 45 ppm/V	—	—	—	
		12 kHz to 20 MHz (OC-48)	—	0.27	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 90 ppm/V	—	—	—	
		12 kHz to 20 MHz (OC-48)	—	0.32	—	
		50 kHz to 80 MHz (OC-192)	—	0.26	—	
		Kv = 135 ppm/V	—	—	—	
		12 kHz to 20 MHz (OC-48)	—	0.40	—	
		50 kHz to 80 MHz (OC-192)	—	0.27	—	
Kv = 180 ppm/V	—	—	—			
12 kHz to 20 MHz (OC-48)	—	0.49	—			
50 kHz to 80 MHz (OC-192)	—	0.28	—			
Kv = 356 ppm/V	—	—	—			
12 kHz to 20 MHz (OC-48)	—	0.87	—			
50 kHz to 80 MHz (OC-192)	—	0.33	—			

**Notes:**

1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K<sub>V</sub> that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K<sub>V</sub>), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCXO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.



Table 6. CLK± Output Phase Jitter (Si571) (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) <sup>1,2,3</sup> for F <sub>OUT</sub> of 125 to 500 MHz	$\phi_J$	Kv = 33 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.37 0.33	— —	ps
		Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.37 0.33	— —	
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.43 0.34	— —	
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.50 0.34	— —	
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.59 0.35	— —	
		Kv = 356 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	1.00 0.39	— —	

**Notes:**

1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K<sub>V</sub> that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K<sub>V</sub>), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCXO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.

Table 7. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J <sub>PER</sub>	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	

**\*Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to "AN279: Estimating Period Jitter from Phase Noise" for further information.

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**Table 8. Typical CLK± Output Phase Noise (Si570)**

Offset Frequency (f)	120.00 MHz LVDS	156.25 MHz LVPECL	622.08 MHz LVPECL	Units
100 Hz	-112	-105	-97	dBc/Hz
1 kHz	-122	-122	-107	
10 kHz	-132	-128	-116	
100 kHz	-137	-135	-121	
1 MHz	-144	-144	-134	
10 MHz	-150	-147	-146	
100 MHz	n/a	n/a	-148	

**Table 9. Typical CLK± Output Phase Noise (Si571)**

Offset Frequency	74.25 MHz 90 ppm/V LVPECL	491.52 MHz 45 ppm/V LVPECL	622.08 MHz 135 ppm/V LVPECL	Units
100 Hz	-87	-75	-65	dBc/Hz
1 kHz	-114	-100	-90	
10 kHz	-132	-116	-109	
100 kHz	-142	-124	-121	
1 MHz	-148	-135	-134	
10 MHz	-150	-146	-146	
100 MHz	n/a	-147	-147	

**Table 10. Absolute Maximum Ratings**

Parameter	Symbol	Rating	Units
Supply Voltage	$V_{DD}$	-0.5 to +3.8	Volts
Input Voltage	$V_I$	-0.5 to $V_{DD} + 0.3$	Volts
Storage Temperature	$T_S$	-55 to +125	°C
ESD Sensitivity (HBM, per JESD22-A114)	ESD	>2500	Volts
Soldering Temperature (lead-free profile)	$T_{PEAK}$	260	°C
Soldering Temperature Time @ $T_{PEAK}$ (lead-free profile)	$t_p$	20-40	seconds

**Notes:**

1. Stresses beyond the absolute maximum ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at [www.silabs.com/VCXO](http://www.silabs.com/VCXO) for further information, including soldering profiles.

**Table 11. Environmental Compliance**

The Si570/571 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016

**Table 12. Programming Constraints**

( $V_{DD} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Frequency	CKO <sub>F</sub>	HS_DIV x N1 >= 6	10	—	945	MHz
		HS_DIV x N1 = 5 N1 = 1	970	—	1134	MHz
		HS_DIV = 4 N1 = 1	1.2125	—	1.4175	GHz
M and RFREQ Value LSB Resolution	M <sub>RES</sub>	114.285 MHz 3rd Overtone Crystal	—	0.09	—	ppb
Internal Oscillator Frequency	f <sub>OSC</sub>		4850	—	5670	MHz
Unfreeze to NewFreq Delay			—	—	10	ms

## 3. Functional Description

The Si570 XO and the Si571 VCXO are low-jitter, programmable oscillators ideally suited for applications requiring multiple frequencies. The Si57x can be programmed to generate any output clock rate between 10 and 1.4 GHz with <1 ppb resolution. Output jitter performance exceeds the strict requirements of high-speed communication systems including OC-48/OC-192 and 10 Gigabit Ethernet.

The Si57x employs Silicon Laboratories' third-generation digital signal processing based phase-locked loop (DSPLL<sup>®</sup>) technology providing excellent jitter performance, digital programmability, and stability while requiring minimal external components. At the core of the Si57x is a digitally-controlled oscillator (DCO) based on DSPLL technology that is driven by a digital frequency control word and produces a low-jitter output clock. (See "1. Detailed Block Diagrams" on page 4.)

### 3.1. Frequency Programming Summary

The output frequency is determined by programming the output dividers (HS\_DIV and N1) and the fine frequency control value (RFREQ). The value programmed into RFREQ is a high-resolution 38-bit value that adjusts the DCO frequency in a range from 4.85 to 5.67 GHz. The output of the DCO is divided down by HS\_DIV and N1 to produce the desired output frequency. The 38-bit length of RFREQ provides an output frequency resolution of better than 1 ppb.

### 3.2. Frequency Programming Details

Programming consists of the following basic steps: deriving the actual crystal frequency, choosing new output dividers (HS\_DIV & N1), calculating a new frequency multiplier (RFREQ), and writing the new frequency set into the device (HS\_DIV, N1, and RFREQ).

#### 3.2.1. Selecting the Correct Output Dividers

By listing all of the combinations of HS\_DIV and N1, one can choose the output divider set with the lowest power within the allowed internal oscillator frequency range as specified in Table 12. The sets of dividers should be sorted to minimize  $f_{osc}$  for power dissipation and to minimize N1 divider's power consumption. Silicon Laboratories' Si57x software automatically provides this optimization and returns the smallest HS\_DIV x N1 combination with the highest HS\_DIV value.

#### 3.2.2. Calculating the Reference Frequency Multiplier (RFREQ)

RFREQ is a binary representation of the reference frequency multiplier and is 38 bits in length. To convert from a decimal number to the binary number RFREQ must be broken into two parts: the integer portion and the fractional portion. The first 10 most-significant-bits (MSBs) of RFREQ represent the integer portion, and the lower 28 least-significant-bits (LSB's) represent the fractional portion. The integer portion can be converted directly from decimal to binary (e.g. decimal 43 = hexadecimal 02Bh--the leading nibble only occupies two bits of RFREQ). The fractional portion should be made into an integer by multiplying by  $2^{28}$  and truncating (or rounding) the result as follows: (e.g.  $0.54587216 \times 2^{28} = 146531442.18730496$ ; then, truncate to 146531442). The truncated value can then be converted to binary (e.g. decimal 146531442 = hexadecimal 8BBE472h). The resulting binary RFREQ for 43.54587216 is 02B8BBE472h (02Bh concatenated with 8BBE472h).

#### 3.2.3. Programming Procedure

The following steps must be followed to set a new output frequency:

1. Read the frequency configuration (RFREQ, HS\_DIV, and N1) from the device after power-up or reset.
2. Calculate the actual nominal crystal frequency ( $f_{XTAL}$ ) as:  $(f_{XTAL} = f_0 \times HS\_DIV \times N1) / RFREQ$  where  $f_0$  is the nominal output frequency.
3. Choose new output frequency ( $f_1$ ).
4. Choose the output dividers (HS\_DIV and N1) for the new output frequency by ensuring the DCO oscillation frequency ( $f_{osc}$ ) is within the allowed internal oscillator frequency (See Table 12) where:  $f_{osc} = f_1 \times HS\_DIV \times N1$ .
5. Calculate the new crystal frequency multiplication ratio (RFREQ<sub>1</sub>) as:  $f_{osc} = f_{XTAL} \times RFREQ_1$ .
6. Freeze the DCO (bit 5 of Register 137).
7. Write the frequency configuration (RFREQ, HS\_DIV, and N1).
8. Unfreeze the DCO and assert the NewFreq bit (bit 6 of Register 135) within the maximum delay specified in Table 12, "Programming Constraints," on page 11.

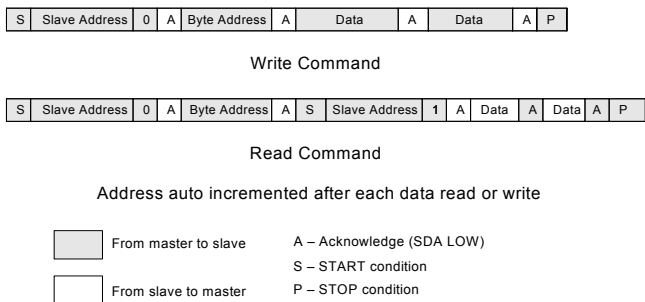
#### 3.2.4. Programming Procedure Example

The Si57x-EVB software can be used to generate examples as needed.

### 3.3. I<sup>2</sup>C Interface

The control interface to the Si570 is an I<sup>2</sup>C-compatible 2-wire bus for bidirectional communication. The bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL). Both lines must be connected to the positive supply via an external pullup. Fast mode operation is supported for transfer rates up to 400 kbps as specified in the I<sup>2</sup>C-Bus Specification standard.

Figure 3 shows the command format for both read and write access. Data is always sent MSB first. The timing specifications and timing diagram for the I<sup>2</sup>C bus can be found in the I<sup>2</sup>C-Bus Specification standard (fast mode operation). The device I<sup>2</sup>C address is specified in the part number.



**Figure 3. I<sup>2</sup>C Command Format**

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## 4. Serial Port Registers

**Note:** Any register not listed here is reserved and must not be written. All bits are R/W unless otherwise noted.

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7	High Speed/ N1 Dividers	HS_DIV[2:0]			N1[6:2]				
8	Reference Frequency	N1[1:0]		RFREQ[37:32]					
9	Reference Frequency	RFREQ[31:24]							
10	Reference Frequency	RFREQ[23:16]							
11	Reference Frequency	RFREQ[15:8]							
12	Reference Frequency	RFREQ[7:0]							
135	Reset/Memory Control	RST_REG	NewFreq						RECALL
137	Freeze DCO			Freeze DCO					

**Register 7. High Speed/N1 Dividers**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HS_DIV[2:0]			N1[6:2]				
Type	R/W			R/W				

Bit	Name	Function
7:5	HS_DIV[2:0]	<p><b>DCO High Speed Divider.</b></p> <p>Sets value for high speed divider that takes the DCO output <math>f_{OSC}</math> as its clock input.</p> <p>000 = 4  001 = 5  010 = 6  011 = 7  100 = Not used.  101 = 9  110 = Not used.  111 = 11</p>
4:0	N1[6:2]	<p><b>CLKOUT Output Divider.</b></p> <p>Sets value for CLKOUT output divider. Allowed values are [1] and [2, 4, 6, ..., <math>2^7</math>]. Illegal odd divider values will be rounded up to the nearest even value. The value for the N1 register can be calculated by taking the divider ratio minus one. For example, to divide by 10, write 0001001 (9 decimal) to the N1 registers.</p> <p>0000000 = 1  1111111 = <math>2^7</math></p>

**Register 8. Reference Frequency**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1[1:0]		RFREQ[37:32]					
Type	R/W		R/W					

Bit	Name	Function
7:6	N1[1:0]	<p><b>CLKOUT Output Divider.</b></p> <p>Sets value for CLKOUT output divider. Allowed values are [1, 2, 4, 6, ..., <math>2^7</math>]. Illegal odd divider values will be rounded up to the nearest even value. The value for the N1 register can be calculated by taking the divider ratio minus one. For example, to divide by 10, write 0001001 (9 decimal) to the N1 registers.</p> <p>0000000 = 1  1111111 = <math>2^7</math></p>
5:0	RFREQ[37:32]	<p><b>Reference Frequency.</b></p> <p>Frequency control input to DCO.</p>

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## Register 9. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[31:24]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[31:24]	<b>Reference Frequency.</b> Frequency control input to DCO.

## Register 10. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[23:16]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[23:16]	<b>Reference Frequency.</b> Frequency control input to DCO.

## Register 11. Reference Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RFREQ[15:8]							
Type	R/W							

Bit	Name	Function
7:0	RFREQ[15:8]	<b>Reference Frequency.</b> Frequency control input to DCO.



**Register 12. Reference Frequency**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	RFREQ[7:0]							
<b>Type</b>	R/W							

Bit	Name	Function
7:0	RFREQ[7:0]	<b>Reference Frequency.</b> Frequency control input to DCO.

**Register 135. Reset/Memory Control**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>Name</b>	RST_REG	NewFreq	N/A				RECALL	
<b>Type</b>	R/W	R/W	R/W				R/W	

Reset settings = 00xx xx00

Bit	Name	Function
7	RST_REG	<b>Internal Reset.</b> 0 = Normal operation. 1 = Reset of all internal logic. Output tristated during reset. Upon completion of internal logic reset, RST_REG is internally reset to zero.
6	NewFreq	<b>New frequency applied.</b> Alerts the DSPLL that a new frequency configuration has been applied. This bit will clear itself when the new frequency is applied.
5:1	N/A	<b>Always zero.</b>
0	RECALL	<b>Recall NVM into RAM.</b> 0 = No operation. 1 = Write NVM bits into RAM. Bit is internally reset following completion of operation.

# Si570/Si571

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## Register 137. Freeze DCO

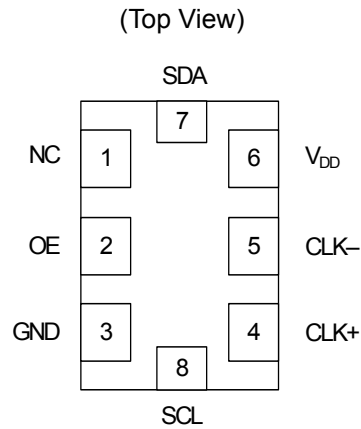
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Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			Freeze DCO					
Type	R/W							

Reset settings = 00xx xx00

Bit	Name	Function
7:6	Reserved	
5	Freeze DCO	<b>Freeze DCO.</b> Freezes the DSPLL so the frequency configuration can be modified.
4:0	Reserved	

## 5. Si570 (XO) Pin Descriptions

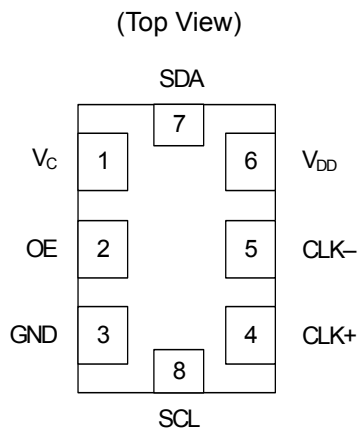


**Table 13. Si570 Pin Descriptions**

Pin	Name	Type	Function
1	NC	N/A	No Connect.
2	OE	Input	Output Enable: See "7. Ordering Information" on page 21.
3	GND	Ground	Electrical and Case Ground.
4	CLK+	Output	Oscillator Output.
5	CLK- (N/A for CMOS)	Output	Complementary Output (N/C for CMOS).
6	V <sub>DD</sub>	Power	Power Supply Voltage.
7	SDA	Bidirectional Open Drain	I <sup>2</sup> C Serial Data.
8	SCL	Input	I <sup>2</sup> C Serial Clock.

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## 6. Si571 (VCXO) Pin Descriptions



**Table 14. Si571 Pin Descriptions**

Pin	Name	Type	Function
1	V <sub>C</sub>	Analog Input	Control Voltage
2	OE	Input	Output Enable: See "7. Ordering Information" on page 21.
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK- (N/A for CMOS)	Output	Complementary Output (N/C for CMOS)
6	V <sub>DD</sub>	Power	Power Supply Voltage
7	SDA	Bidirectional Open Drain	I <sup>2</sup> C Serial Data
8	SCL	Input	I <sup>2</sup> C Serial Clock

## 7. Ordering Information

The Si570/Si571 supports a wide variety of options including frequency range, start-up frequency, temperature stability, tuning slope, output format, and  $V_{DD}$ . Specific device configurations are programmed into the Si570/Si571 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to [www.silabs.com/VCXOPartNumber](http://www.silabs.com/VCXOPartNumber) to access this tool and for further ordering instructions. The Si570/Si571 XO/VCXO series is supplied in an industry-standard, RoHS compliant, Pb-free, 8-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.

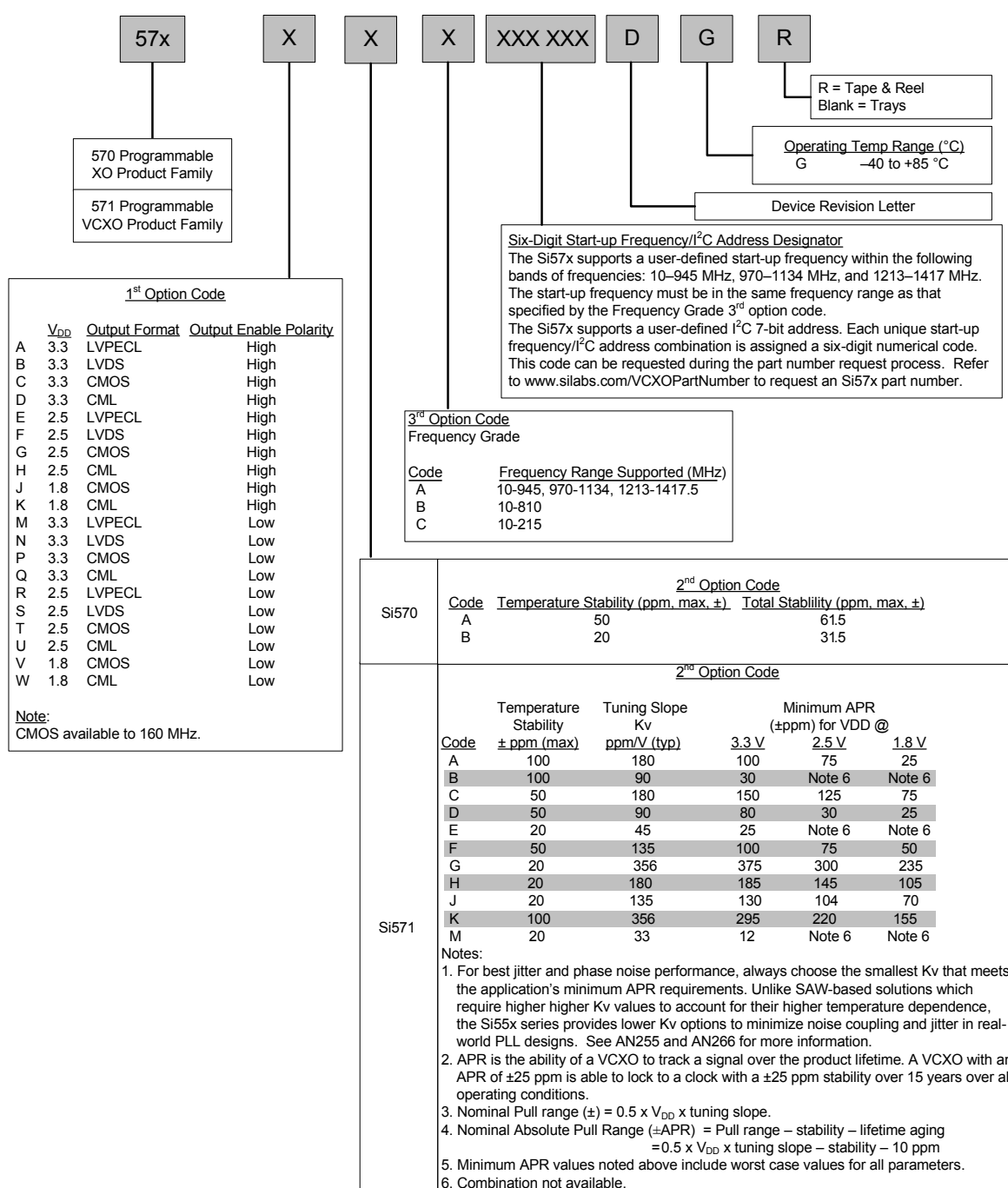


Figure 4. Part Number Convention

# Si570/Si571

## 8. Si57x Mark Specification

Figure 5 illustrates the mark specification for the Si57x. Table 15 lists the line information.

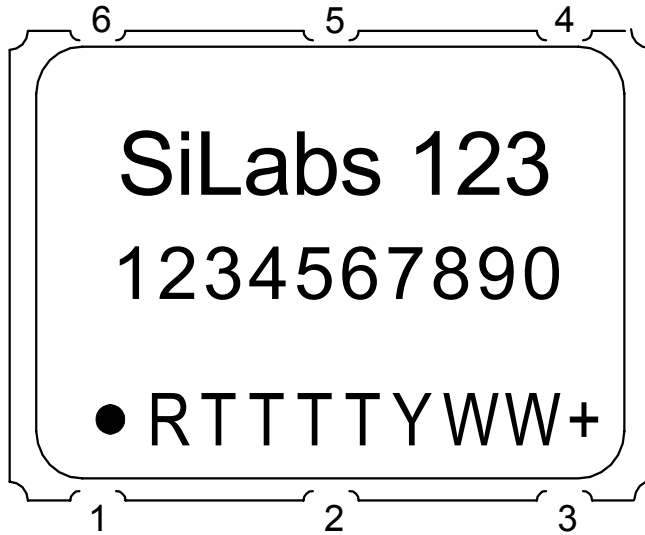


Figure 5. Mark Specification

Table 15. Si57x Top Mark Description

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 5xx (First 3 characters in part number)
2	1–10	Si570, Si571: Option1 + Option2 + Option3 + ConfigNum(6) + Temp
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

## 9. Outline Diagram and Suggested Pad Layout

Figure 6 illustrates the package details for the Si570/Si571. Table 16 lists the values for the dimensions shown in the illustration.

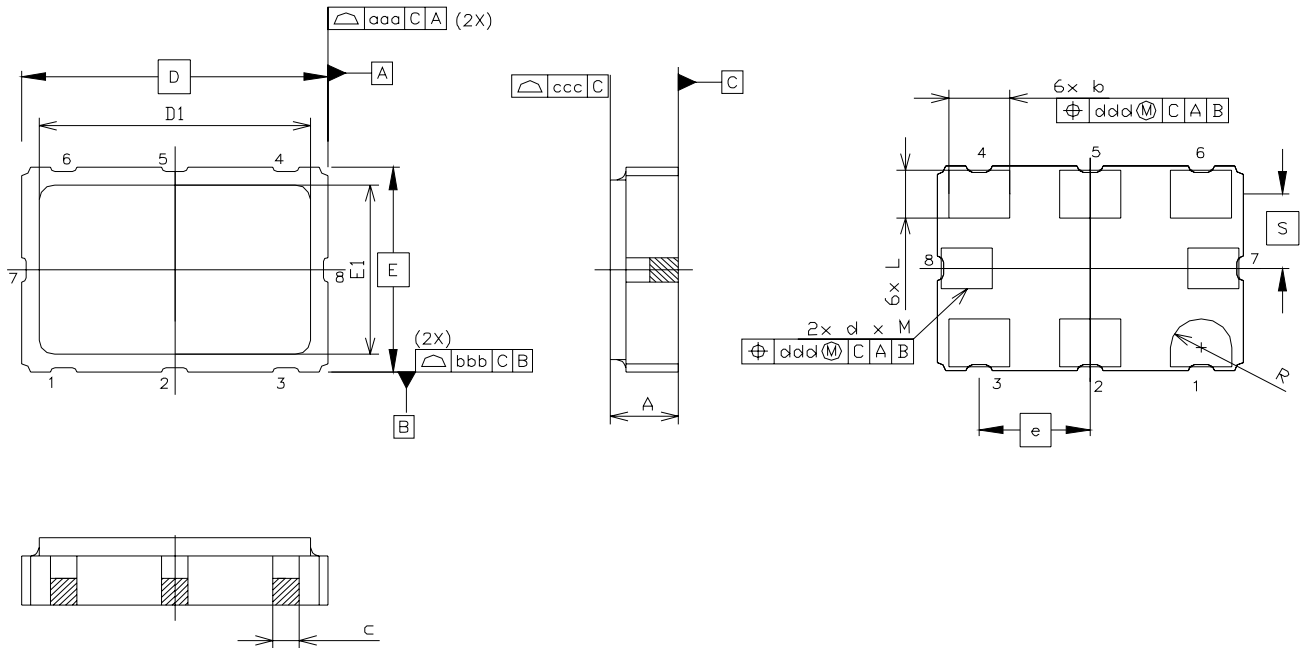


Figure 6. Si570/Si571 Outline Diagram

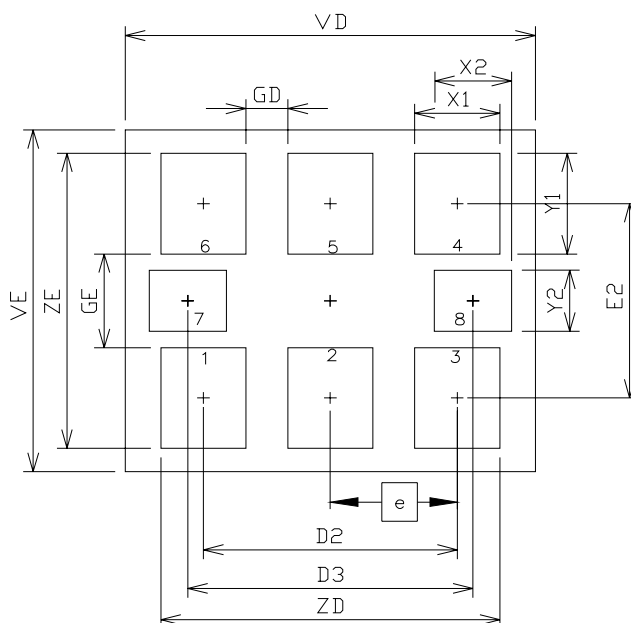
Table 16. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.45	1.65	1.85
b	1.2	1.4	1.6
c	0.60 TYP		
d	0.97	1.17	1.37
D	7.00 BSC		
D1	6.10	6.2	6.30
e	2.54 BSC		
E	5.00 BSC		
E1	4.30	4.40	4.50
L	1.07	1.27	1.47
M	0.8	1.0	1.2
S	1.815 BSC		
R	0.7 REF		
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

# Si570/Si571

## 10. 8-Pin PCB Land Pattern

Figure 7 illustrates the 8-pin PCB land pattern for the Si570/Si571. Table 17 lists the values for the dimensions shown in the illustration.



**Figure 7. Si570/Si571 PCB Land Pattern**

**Table 17. PCB Land Pattern Dimensions (mm)**

Dimension	Min	Max
D2		5.08 REF
D3		5.705 REF
e		2.54 BSC
E2		4.20 REF
GD	0.84	—
GE	2.00	—
VD		8.20 REF
VE		7.30 REF
X1		1.70 TYP
X2		1.545 TYP
Y1		2.15 REF
Y2		1.3 REF
ZD	—	6.78
ZE	—	6.30

**Note:**

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design follows IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).



## DOCUMENT CHANGE LIST

### Revision 0.1 to Revision 0.2

- Updated "Description" on page 1.
- Updated "1. Detailed Block Diagrams" on page 4 for both XO and VCXO.
- Updated the Nominal Control Voltage in Table 2, "V<sub>C</sub> Control Voltage Input," on page 5.
- Updated tables to reflect slight performance differences between Si570 and Si571.
- Added detail to the "3.2. Frequency Programming Details" on page 12.
- Revised "3.2.3. Programming Procedure" on page 12.
  - Procedure now requires use of two frequency configuration register sets.
  - Procedure now recommends disabling output at powerup to protect equipment not expecting the default output frequency.
- Added second frequency configuration register set to the register tables.
- Added frequency configuration select register.
- Updated "7. Ordering Information" on page 21 to be consistent with the Si55x series devices.

### Revision 0.2 to Revision 0.3

- Updated Table 1, "Recommended Operating Conditions," on page 5.
  - Device maintains stable operation over -40 to +85 °C operating temperature range.
  - Supply current specifications updated.
- Updated Table 4, "CLK± Output Levels and Symmetry," on page 7.
  - Updated LVDS differential peak-peak swing specifications.
- Updated Table 5, "CLK± Output Phase Jitter (Si570)," on page 7.
- Updated Table 6, "CLK± Output Phase Jitter (Si571)," on page 8.
- Updated Table 7, "CLK± Output Period Jitter," on page 9.
  - Revised period jitter specifications.
- Updated Table 10, "Absolute Maximum Ratings," on page 10 to reflect the soldering temperature time at 260 °C is 20–40 sec per JEDEC J-STD-020C.
- Updated device programming procedure in Section "3.2.3. Programming Procedure" on page 12.
- Updated "7. Ordering Information" on page 21.
  - Changed ordering instructions to revision D.
- Added "8. Si57x Mark Specification" on page 22.

# Si570/Si571

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