STD150NH02L

N-CHANNEL 24V - 0.003 Ω - 150A ClipPAK™/IPAK STripFET™ III POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD150NH02L	24 V	< 0.0035 Ω	150 A

- TYPICAL R_{DS}(on) = 0.003 Ω @ 10 V
- TYPICAL R_{DS}(on) = 0.005 Ω @ 5 V
- $R_{DS(ON)}$ * Qg INDUSTRY's BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

IPAK TO-251 (Suffix "-1")

ClipPak™ (Suffix "T4")

DESCRIPTION
The STD150NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This novel 0.6μ process utilizes also unique metallization techniques that couple to a "bondless" assembly technique result in outstanding performance with standard DPAK outline. It is therefore ideal in high performance DC-DC converter applications where efficiency it to be achieved at very high out currents.

APPLICATIONS
- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTES
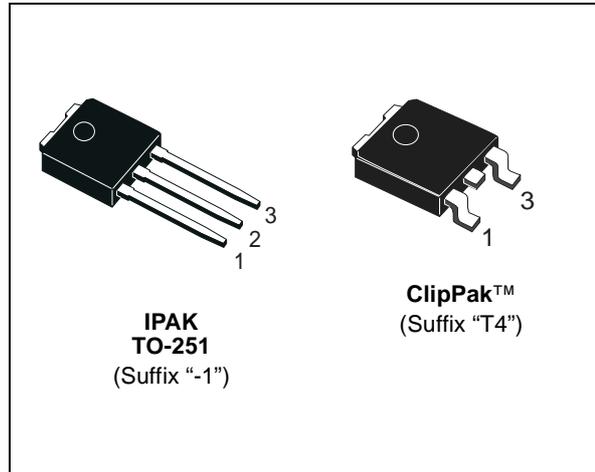
INTERNAL SCHEMATIC DIAGRAM

SC07580
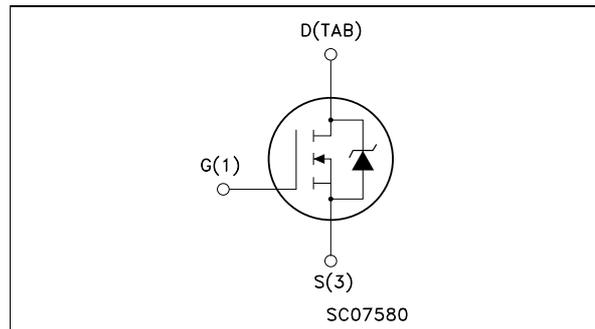
Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD150NH02LT4	D150NH02L	ClipPak	TAPE & REEL
STD150NH02L-1	D150NH02L	TO-251	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{spike(1)}$	Drain-source Voltage Rating	30	V
V_{DS}	Drain-source Voltage (V_{GS} = 0)	24	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	24	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	150	A
I_D	Drain Current (continuous) at T_C = 100°C	107	A
I_{DM}[(2)]	Drain Current (pulsed)	600	A
P_{tot}	Total Dissipation at T_C = 25°C	125	W
	Derating Factor	0.83	W/°C
E_{AS} [(3)]	Single Pulse Avalanche Energy	500	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.2	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 25 mA, V_{GS} = 0	24			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 20 V V_{DS} = 20 V T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON [4]

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1	1.8		V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 75 A V_{GS} = 5 V I_D = 37.5 A		0.003 0.004	0.0035 0.0065	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} [4]	Forward Transconductance	V_{DS} = 10 V I_D = 75 A		60		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 15V f = 1 MHz V_{GS} = 0		4450 1126 141		pF pF pF
R_G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1.6		Ω

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 10 V I_D = 75 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		14 224		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 16V I_D= 150A V_{GS}= 10 V		69 13 9	93	nC nC nC
Q_{oss}[5]	Output Charge	V_{DS}= 16 V V_{GS}= 0 V		27		nC
Q_{gls}[6]	Third-quadrant Gate Charge	V_{DS}< 0 V V_{GS}= 10 V		64		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 10 V I_D = 75 A R_G = 4.7Ω, V_{GS} = 10 V (Resistive Load, Figure 3)		69 40	54	ns ns

SOURCE DRAIN DIODE

| Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				150 600	A A
V_{SD} [4]	Forward On Voltage	I_{SD} = 75 A V_{GS} = 0			1.15	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 150 A di/dt = 100A/μs V_{DD} = 15 V T_j = 150°C (see test circuit, Figure 5)		47 58 2.5		ns nC A

[1] Garanted when external Rg=4.7 Ω and t_f < t_{fmax}.
[2] Pulse width limited by safe operating area
[3] Starting T_j = 25 °C, I_D = 75A, V_{DD} = 10V
.
.

[4] Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
[5] Q_{oss} = C_{oss}*Δ V_{in} , C_{oss} = C_{gd} + C_{ds} . See Appendix A
[6] Gate charge for synchronous operation

Safe Operating Area
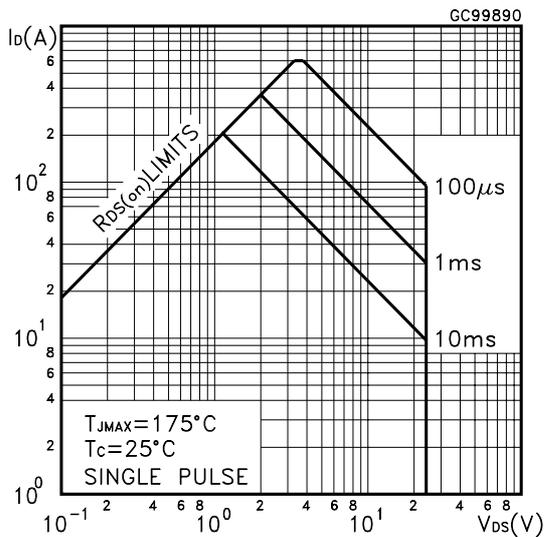
Thermal Impedance
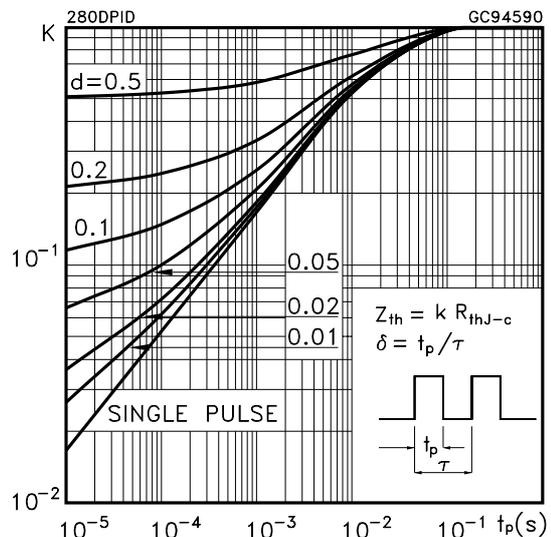
STD150NH02L

Output Characteristics

GC96070b
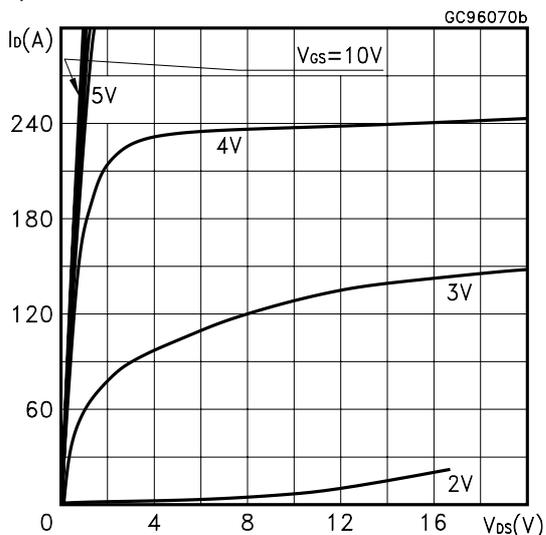
Transfer Characteristics

GC96080

Transconductance

GC96090
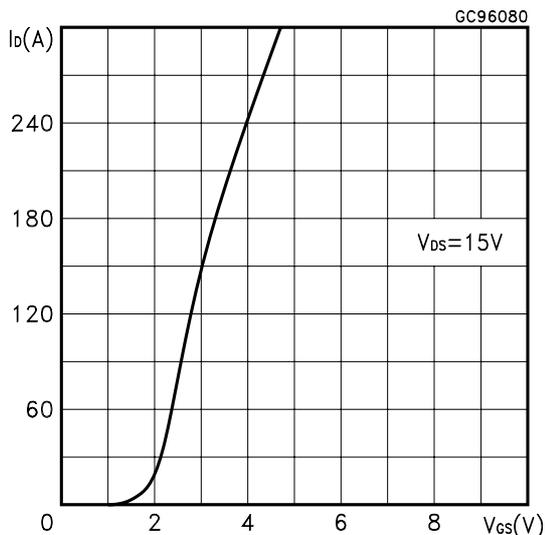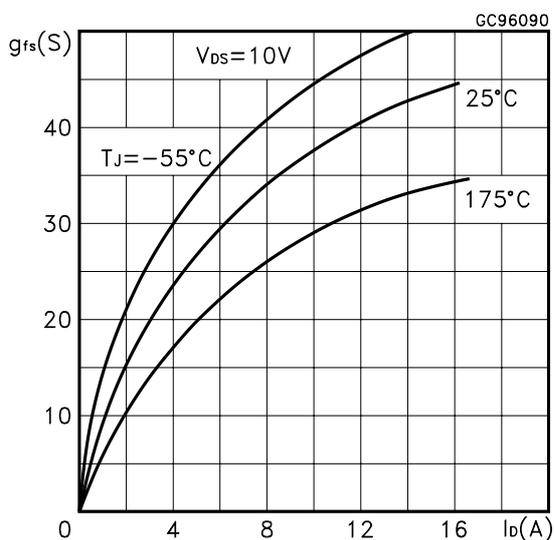
Static Drain-source On Resistance

GC96100b
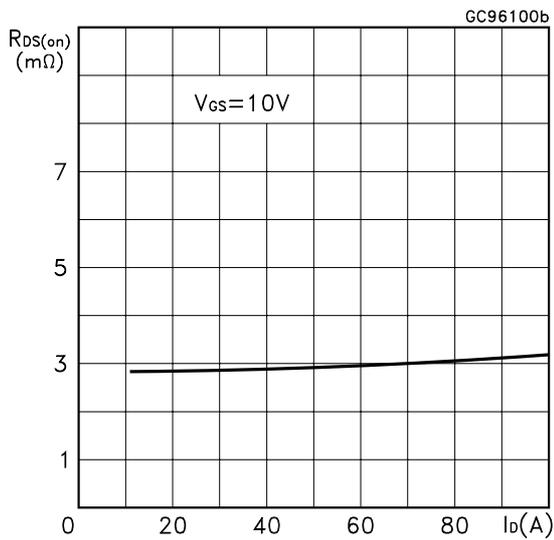
Gate Charge vs Gate-source Voltage

GC96110c
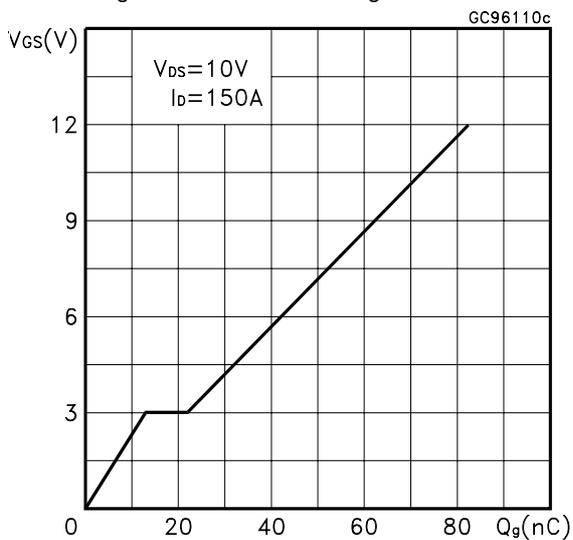
Capacitance Variations

GC96120
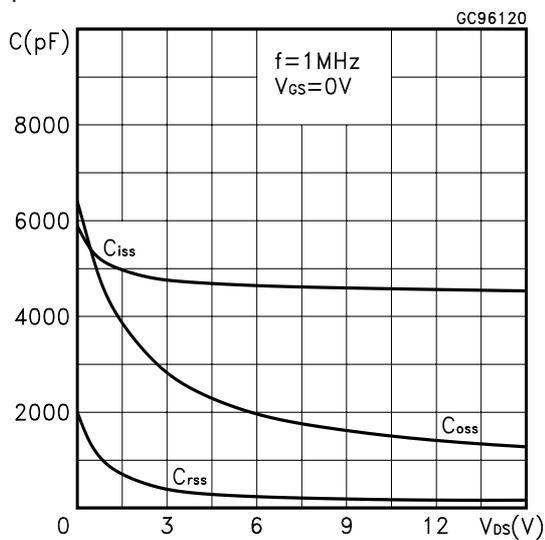
STD150NH02L

Normalized Gate Threshold Voltage vs Temperature

GC96130

$V_{GS}(th)$ (norm)

$V_{DS}=V_{GS}$
$I_D=250\mu A$
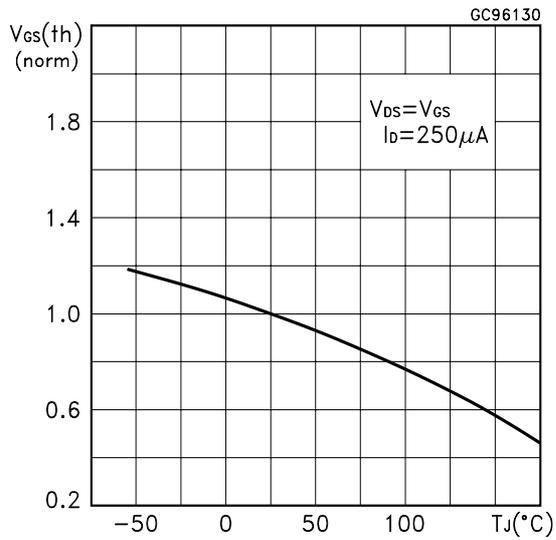
Normalized on Resistance vs Temperature

GC96140c

$R_{DS}(on)$ (norm)

$V_{GS}=10V$
$I_D=75A$
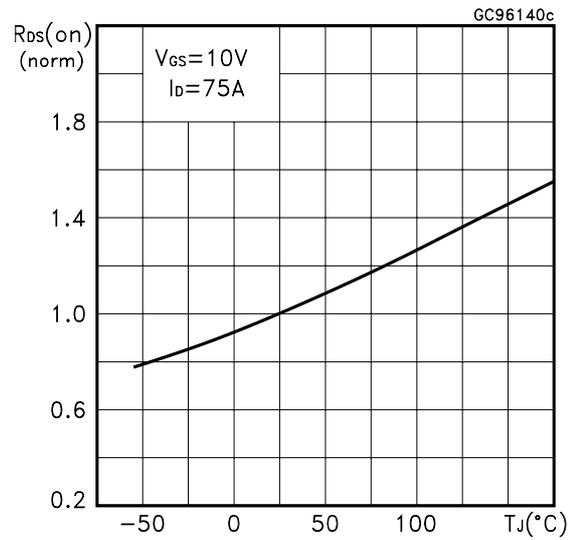
Source-drain Diode Forward Characteristics

GC96150

$V_{SD}(V)$

$T_J=-55°C$ 25°C 175°C

$I_{SD}(A)$
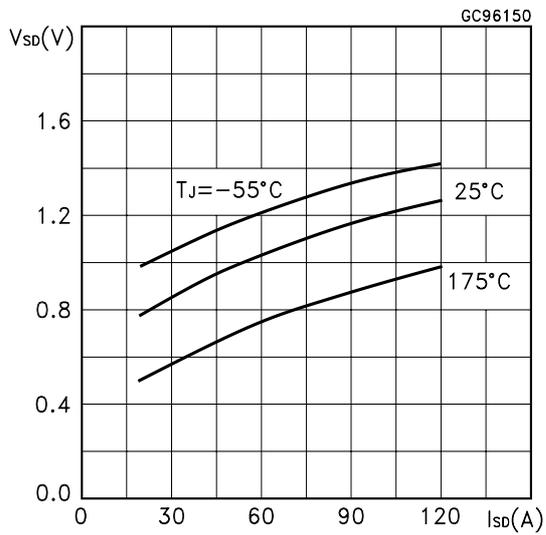
Normalized Breakdown Voltage vs Temperature

GC96160

$V_{(BR)DSS}$ (norm)

$V_{GS}=0$
$I_D=250\mu A$

.   .
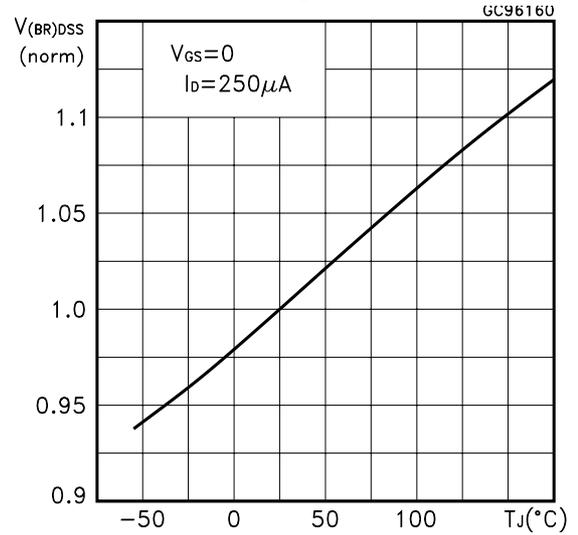
Fig. 1: Unclamped Inductive Load Test Circuit
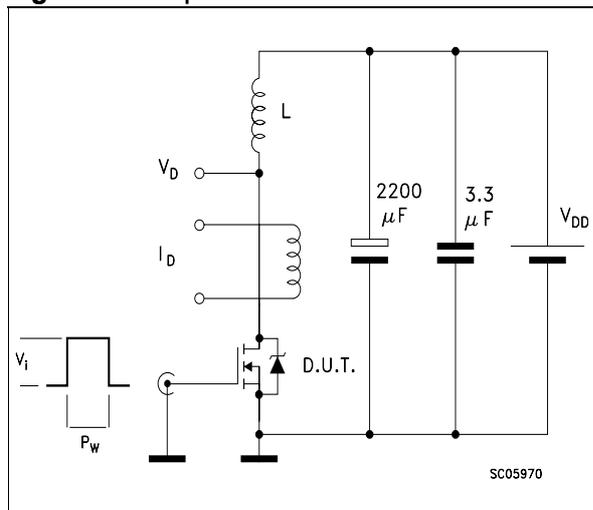

Fig. 2: Unclamped Inductive Waveform
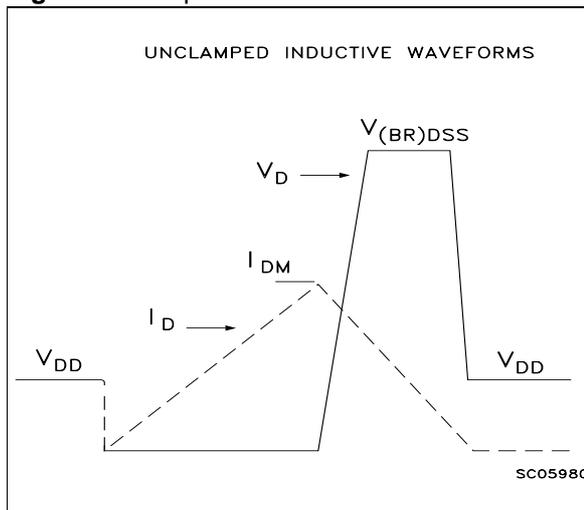

Fig. 3: Switching Times Test Circuits For Resistive Load
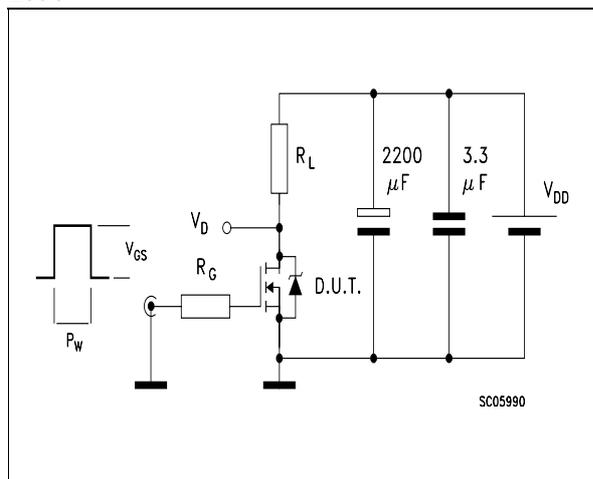

Fig. 4: Gate Charge test Circuit
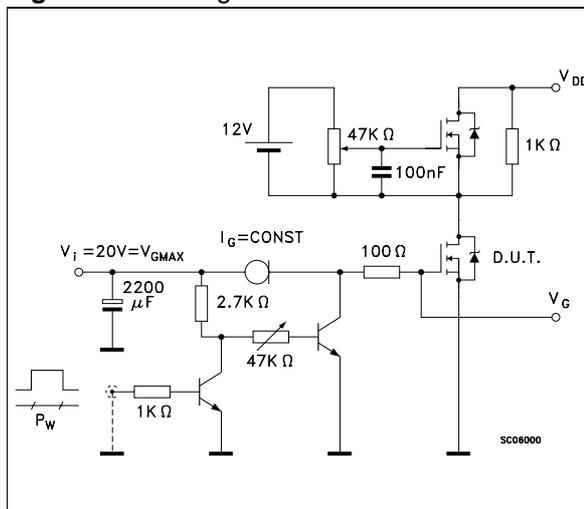
**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times
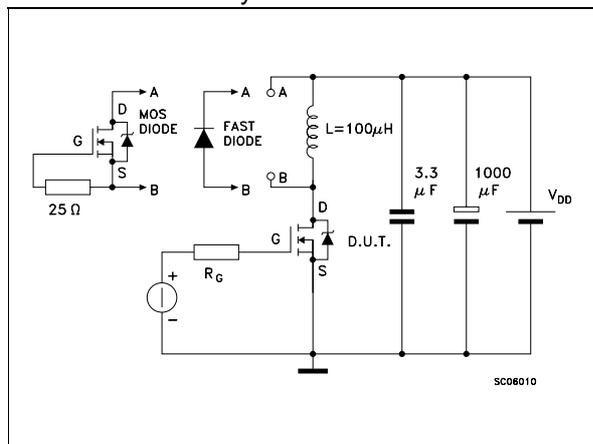
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

0068771-E
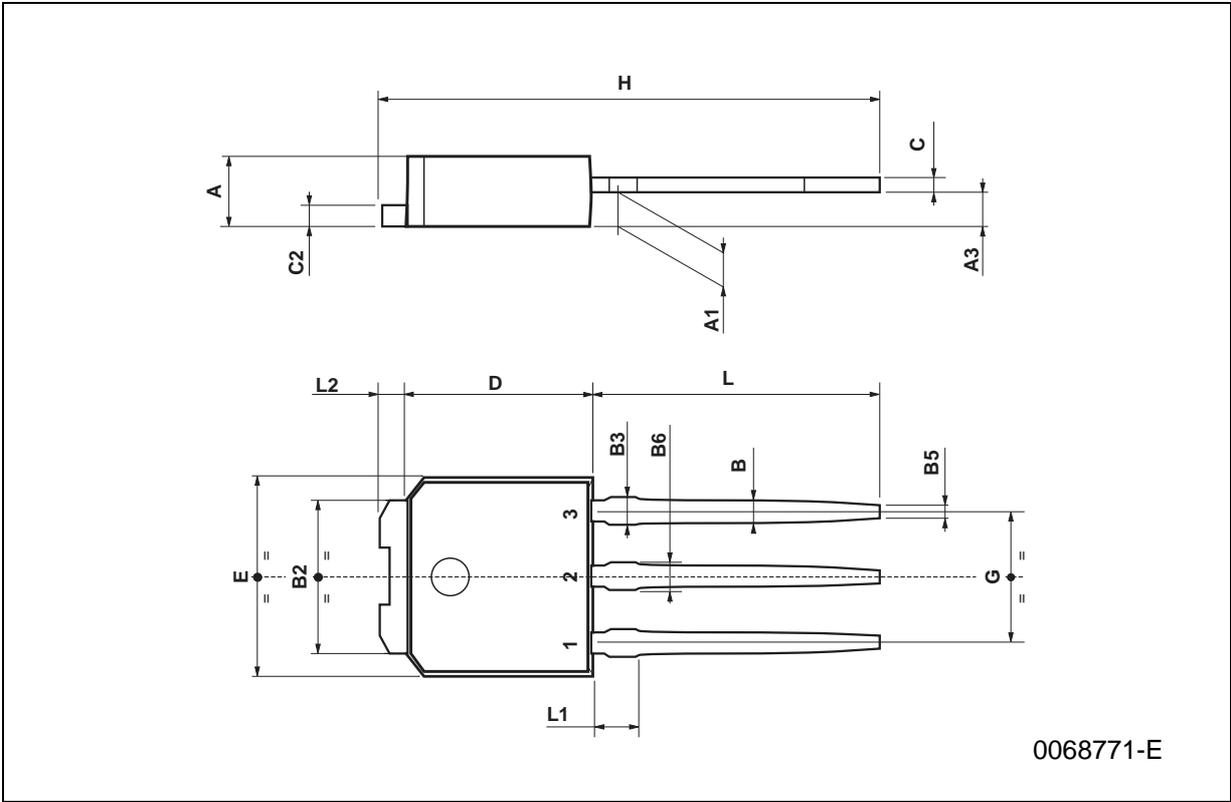
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039

DETAIL "A"

0068772-B
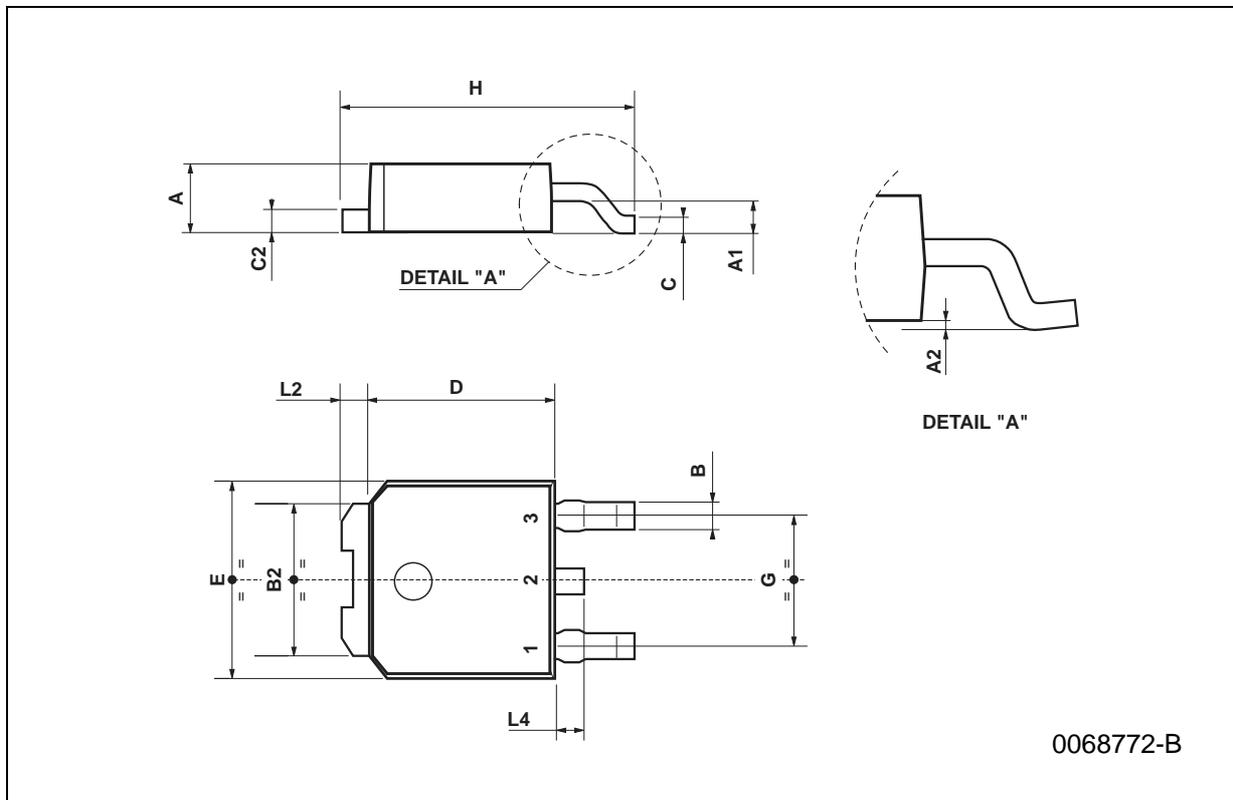
APPENDIX A
Buck Converter: Power Losses Estimation
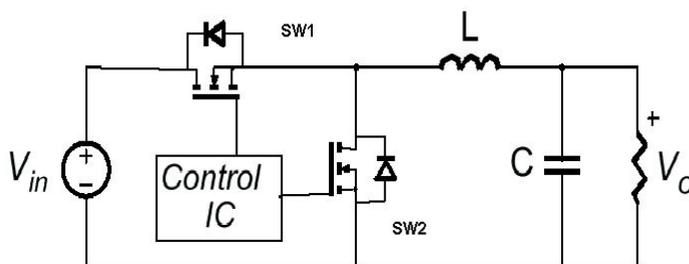
The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (**SW2**) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW_1 during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (**SW1**) device requires:
- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{conduction}$		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1-\delta)$
$P_{switching}$		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \dfrac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$^1V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not Applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
$P_{gate(Q_G)}$		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P_{Qoss}		$\dfrac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\dfrac{V_{in} * Q_{oss(SW2)} * f}{2}$

Parameter	Meaning
δ	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P$_{Qoss}$	Output capacitance losses

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[1] Dissipated by SW1 during turn-on

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