



CelXpres[™] T8207 Asynchronous Transfer Mode (ATM) Interconnect

Features

- 32 multi-PHY (MPHY) operation
- Programmable number of UTOPIA output queues with four levels of priority
- Shared UTOPIA mode
- Egress SDRAM buffer support to extend UTOPIA output priority queues for 32K to 512K cells
 - 64 queues configurable up to four queues per PHY with programmable sizes
 - Programmable insertion of the explicit forward congestion indication (EFCI) bit
- Support of ATM traffic management via partial packet discard (PPD), forward explicit congestion notification (FECN), and the cell loss priority (CLP) bit
- Selectable slew rate GTL+ I/O
 - >1.5 Gbits/s cell bus operation
 - Programmable as bus arbiter
- Flexible per virtual channel (VC) cell counters
- Cell header insertion with virtual path identifier (VPI) and virtual channel identifier (VCI) translation via external SRAM (up to 64K entries)
- Support of network node interface (NNI) and user network interface (UNI) header types with optional generic flow control (GFC) insertion
- Programmable operations and maintenance and resource management (OAM/RM) cell routing
- Support of multicast and broadcast addresses per PHY

- Footprint compatible with the T8206
- Eight GPIO pins
- JTAG support
- Optional monitoring of misrouted cells
- Microprocessor interface, supporting both *Motorola** and *Intel*† modes (multiplexed and nonmultiplexed)
- Control cell transmission and reception through microprocessor port
- Compatible with *Transwitch CellBus*‡
- 3.3 V power supply
- 3.3 V TTL I/O (5 V tolerant)
- 272-pin BGA package
- Industrial temperature range (−40 °C to +85 °C)

Applications

- Asymmetric digital subscriber line (ADSL) digital subscriber line access multiplexer (DSLAMs)
- Access gateways
- Access multiplexers/concentrators
- Multiservice access equipment platforms

* *Motorola* is a registered trademark of Motorola, Inc.

† *Intel* is a registered trademark of Intel Corporation.

‡ *Transwitch* and *CellBus* are registered trademarks of Transwitch Corp.

Description

The *CelXpres* T8207 device integrates all of the required functionality to transport ATM cells across a backplane architecture with high-speed cell traffic exceeding 1.5 Gbits/s to a maximum of 32 destinations. The management of multiple service classes and monitoring of performance on ATM and PHY interfaces is incorporated in the device's functionality. Traffic delivery to multi-PHYs (MPHYs) is managed through the UTOPIA interface.

The *CelXpres* T8207 device meets the ATM Forum's universal test and operations PHY interface for ATM (UTOPIA) Level 1, version 2.01 and Level 2, version 1.0 specifications for cell-level handshake and MPHY data path operation. The T8207 supports the required MPHY operation as described in sections 4.1 and 4.2 of the ATM Forum's Level 2 specification. The T8207 supports MPHY operation for up to 32 ports. In addition to the required UTOPIA signals, the optional transmit parity (TxPRTY) and receive parity (RxPRTY) signals are provided.

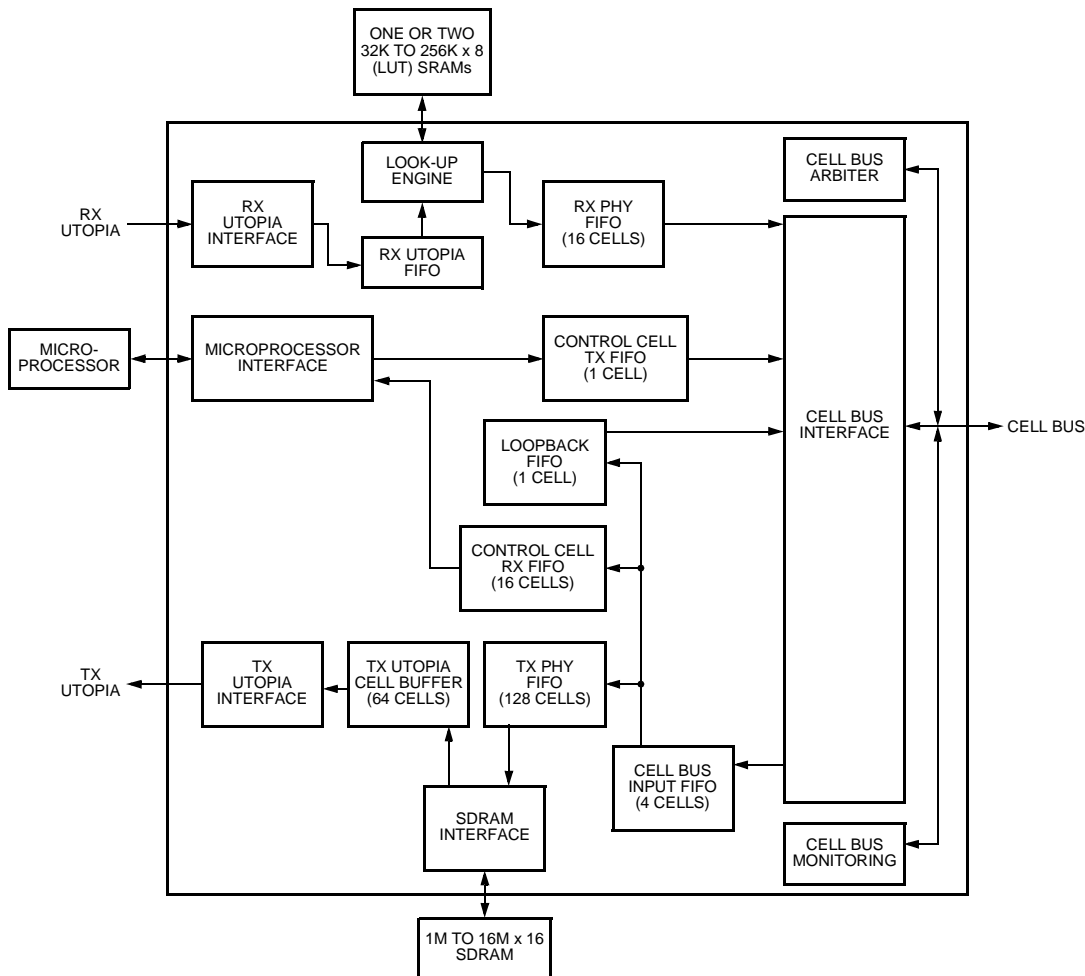


Figure 1. Functional Block Diagram

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Description (continued)

The *CelXpres* T8207 may be configured as an ATM or PHY level device providing cell routing between UTOPIA and a 32-bit wide GTL+ bus. In addition to the 32 data signals, the bus has the following signals:

- Read clock
- Write clock
- Frame sync
- Acknowledge

ATM cells arriving at the UTOPIA receive interface may get VPI and VCI translation and routing information from a look-up table in external SRAM. An external synchronous dynamic random access memory (SDRAM) is used to extend the buffering for ATM cells destined for the UTOPIA transmit interface. This exter-

nal SDRAM may be partitioned into four or less independently sized queues per PHY. The four queues may be used to implement QoS using different priorities for each queue.

The *CelXpres* T8207 provides a shared UTOPIA mode, which allows two devices on different cell buses to share the same UTOPIA bus in ATM mode. Using a glueless interface between the two T8207s, the chips resolve queue priorities for the PHYs and arbitrate the use of the UTOPIA bus. This shared mode can be used to provide redundancy or increase the system capacity.

In addition, an external microprocessor may send or receive control or loopback cells through the microprocessor interface. The 8-bit microprocessor interface may be configured to be *Motorola* or *Intel* compatible and is used to configure and monitor the device.

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