UCN-4805A
BiMOS LATCHED DECODER/DRIVER

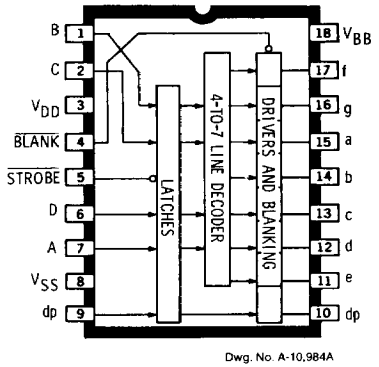
FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Hexadecimal Decoding
- Internal Pull-Up/Pull-Down Resistors
- Wide Supply Voltage Range

DESIGNED for use in high-voltage vacuum fluorescent display driver applications, the UCN-4805A latched decoder/driver combines CMOS logic with bipolar source outputs. The device consists of eight high-voltage bipolar sourcing outputs, with internal pull-down resistors and CMOS input latches, hexadecimal decoder, and control circuitry (strobe and blanking).

Type UCN-4805A is intended to serve as the segment driver with standard 7-segment displays incorporating a colon or decimal point. The integrated circuit uses hexadecimal decoding to display 0-9, A, b, C, d, E, and F.

This BiMOS latched decoder/driver has sufficient speed to permit operation with most microprocessor/LSI-based systems. The CMOS input latches provide operation over the supply voltage range of 5 to 15 V with minimum logic loading. Internal output pull-down resistors eliminate the need for external components usually required for fluorescent display applications. When used with standard TTL or low-speed TTL logic, the device may require employment of input pull-up resistors to insure a proper input logic high.



UCN-4805A

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ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT}	60 V
Logic Supply Voltage Range, V_{DD}	4.5 V to 18 V
Driver Supply Voltage Range, V_{BB}	5.0 V to 60 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT}	−40 mA
Package Power Dissipation, P_D	1.82 W*
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = 25°C.

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
Output Leakage Current		$T_A = 70°C$	—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 15$ V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = 5.0$ V	—	100	μA
		$V_{DD} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	Display "8"	—	9.1	mA
		All outputs OFF	—	100	μA
	I_{DD}	V_{DD} = I/O = STROBE = 5.0 V, All other inputs = 0 V	—	200	μA
		V_{DD} = I/O = STROBE = 15 V, All other inputs = 0 V	—	500	μA
		V_{DD} = STROBE = BLANK = 5.0 V, Data latched, Display "8"	—	7.0	mA
		V_{DD} = STROBE = BLANK = 15 V, Data latched, Display "8"	—	21	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

MAXIMUM ALLOWABLE DUTY CYCLE

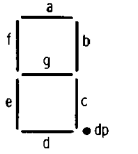
Number of Outputs ON ($I_{OUT} = -25$ mA)	Max. Allowable Duty Cycle at Ambient Temperature of 50°C	60°C	70°C
8	100%	92%	78%
7	↑	100%	89%
6	↕	↑	100%
↕		↕	↕
1	100%	100%	100%

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

UCN-4805A TRUTH TABLE

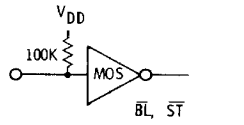
Inputs								Outputs							
D	C	B	A	dp	$\overline{BL}$	$\overline{ST}$	Character	a	b	c	d	e	f	g	dp
0	0	0	0	0	1	0	Zero	1	1	1	1	1	1	0	0
0	0	0	1	0	1	0	One	0	1	1	0	0	0	0	0
0	0	1	0	0	1	0	Two	1	1	0	1	1	0	1	0
0	0	1	1	0	1	0	Three	1	1	1	1	0	0	1	0
0	1	0	0	0	1	0	Four	0	1	1	0	0	1	1	0
0	1	0	1	0	1	0	Five	1	0	1	1	0	1	1	0
0	1	1	0	0	1	0	Six	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	Seven	1	1	1	0	0	0	0	0
1	0	0	0	0	1	0	Eight	1	1	1	1	1	1	1	0
1	0	0	1	0	1	0	Nine	1	1	1	0	0	1	1	0
1	0	1	0	0	1	0	A	1	1	1	0	1	1	1	0
1	0	1	1	0	1	0	b	0	0	1	1	1	1	1	0
1	1	0	0	0	1	0	C	1	0	0	1	1	1	0	0
1	1	0	1	0	1	0	d	0	1	1	1	1	0	1	0
1	1	1	0	0	1	0	E	1	0	0	1	1	1	1	0
1	1	1	1	0	1	0	F	1	0	0	0	1	1	1	0
X	X	X	X	1	1	0	dp	X	X	X	X	X	X	X	1
X	X	X	X	X	0	X	blank	0	0	0	0	0	0	0	0

X = irrelevant

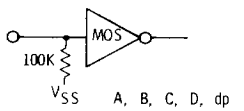


DWG. NO. A-10,985

TYPICAL INPUT CIRCUITS

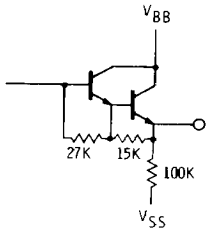


Dwg.No. A-10,979A



Dwg. No. A-10,980

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,981

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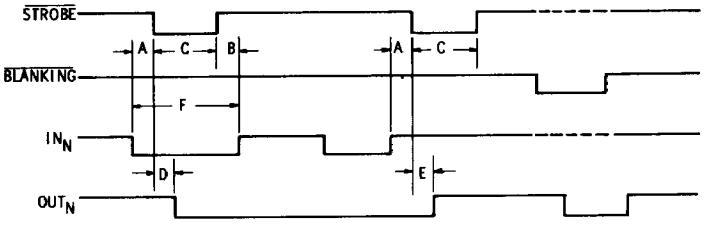
TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})



Dwg. No. A-10,982A

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... 100 ns
C. Minimum Strobe Pulse Width ..... 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition ..... 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition ..... 1.0 μs
F. Minimum Data Pulse Width ..... 500 ns

Information present at an input is transferred to its latch when the $\overline{\text{STROBE}}$ ($\overline{\text{ST}}$) is low. The latches will continue to accept new data as long as the $\overline{\text{STROBE}}$ is held low. Applications where the latches are bypassed ($\overline{\text{STROBE}}$ tied low) ordinarily require that the $\overline{\text{BLANKING}}$ input be low between digit selection because of possible non-synchronous decoding.

When the $\overline{\text{BLANKING}}$ ($\overline{\text{BL}}$) input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the $\overline{\text{BLANKING}}$ input high, the outputs are controlled by the latch/decoder circuitry.