17 X 17 3.2 GBIT/S DIFFERENTIAL CROSSPOINT SWITCH S2018

FEATURES

- SiGe BiCMOS Technology
- 17 x 17 differential crosspoint switch
- Broadcast and multicast switching capability
- Differential 200 mV to 1400 mV input data
- Differential 200 mV to 1300 mV programmable output swing
- Up to 3.2 Gbps NRZ data rate
- LVTTL configuration controls
- Internal 100 Ω line-to-line terminations on high-speed differential inputs
- Reconfigurable without disturbing operation
- 35 mm x 35 mm 352 pin SBGA package
- +3.3 V only power supply
- 4 W typical power dissipation with 800 mV output swing
- Complies with Bellcore and ITU-T Standard

APPLICATIONS

- Dense Wavelength Division Multiplexing (DWDM) systems
- Internet switches
- Digital video
- Digital demultiplexing
- Microwave or fiber-optic data distribution
- High-speed automatic test equipment
- Datacom or telecom switching

GENERAL DESCRIPTION

The S2018 is a high speed 17 x 17 differential crosspoint switch with full broadcast capability. Any of its 17 differential LVPECL input signal pairs can be connected to any or all of its 17 differential CML output signal pairs.

The differential 10K LVPECL logic data path makes the part ideal for high-speed applications. The differential nature of the data path is retained throughout the crosspoint structure to minimize data distortion and to handle NRZ data rates up to 3.2 gigabits per second. The high-speed serial inputs to the S2018 are internally biased and have internal 100 Ω line-to-line terminations.

LVTTL configuration controls simplify interfacing to slower speed circuitry. Once a new configuration has been entered into the configuration register file, the S2018 can be completely reconfigured by pulsing the CONFIGN input.

Figure 1 shows a system block diagram incorporating the S2018 with AMCC serial backplane devices. Figure 2 shows the basic operation of the switch.

Figure 1. System Block Diagram

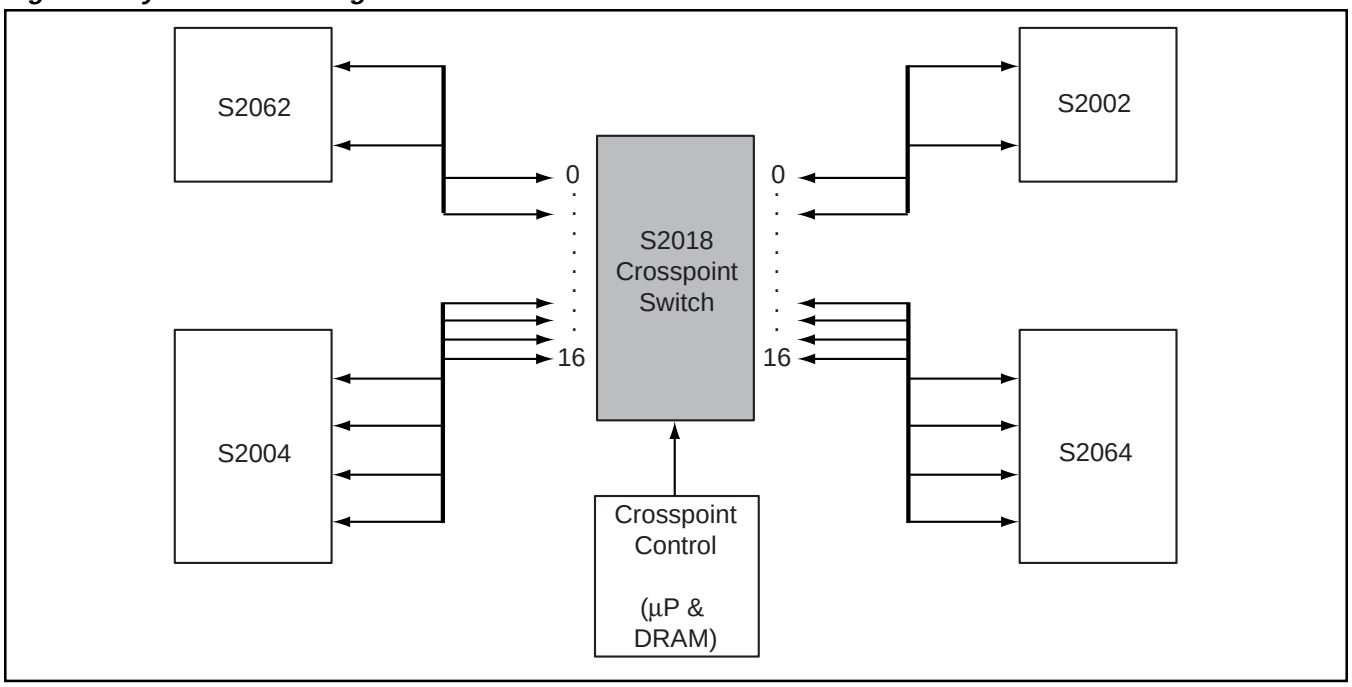


Figure 2. Functional Block Diagram

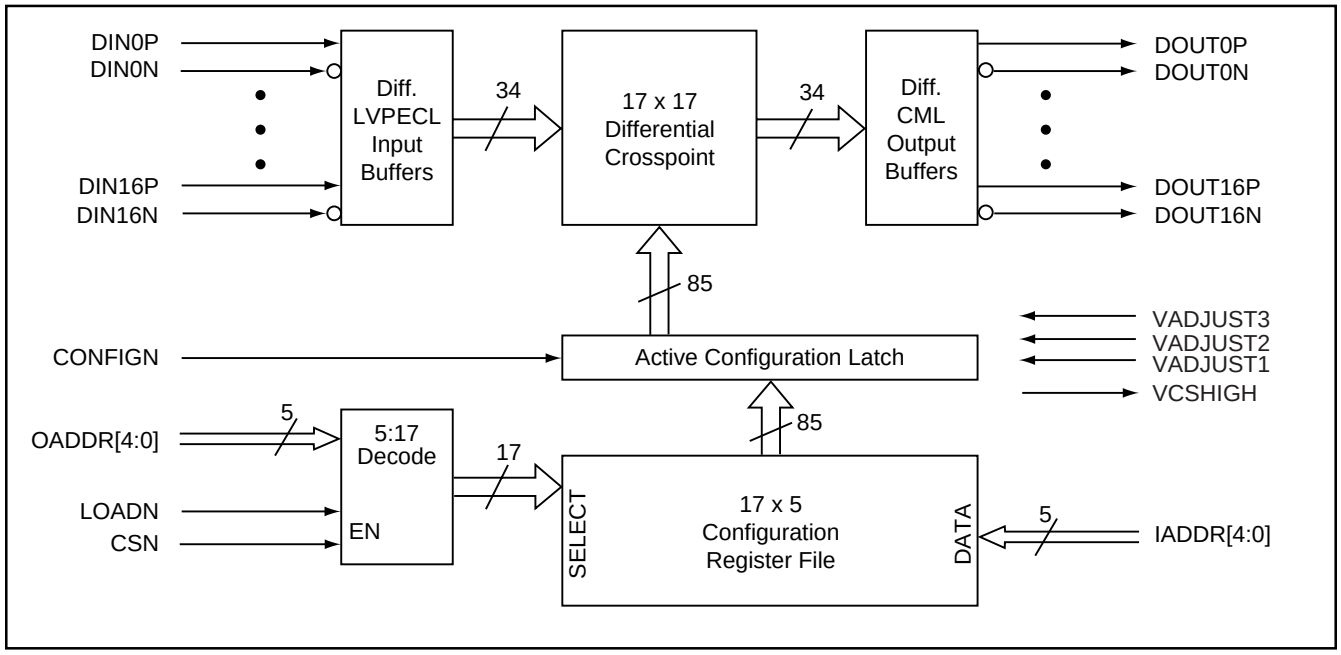


Table 1. Input/Output Address of S2018

DIFF INPUT	IADDR4	IADDR3	IADDR2	IADDR1	IADDR0	**DIFF OUTPUT**	OADDR4	OADDR3	OADDR2	OADDR1	OADDR0
DIN0	0	0	0	0	0	**DOUT0**	0	0	0	0	0
DIN1	0	0	0	0	1	**DOUT1**	0	0	0	0	1
DIN2	0	0	0	1	0	**DOUT2**	0	0	0	1	0
DIN3	0	0	0	1	1	**DOUT3**	0	0	0	1	1
DIN4	0	0	1	0	0	**DOUT4**	0	0	1	0	0
DIN5	0	0	1	0	1	**DOUT5**	0	0	1	0	1
DIN6	0	0	1	1	0	**DOUT6**	0	0	1	1	0
DIN7	0	0	1	1	1	**DOUT7**	0	0	1	1	1
DIN8	0	1	0	0	0	**DOUT8**	0	1	0	0	0
DIN9	0	1	0	0	1	**DOUT9**	0	1	0	0	1
DIN10	0	1	0	1	0	**DOUT10**	0	1	0	1	0
DIN11	0	1	0	1	1	**DOUT11**	0	1	0	1	1
DIN12	0	1	1	0	0	**DOUT12**	0	1	1	0	0
DIN13	0	1	1	0	1	**DOUT13**	0	1	1	0	1
DIN14	0	1	1	1	0	**DOUT14**	0	1	1	1	0
DIN15	0	1	1	1	1	**DOUT15**	0	1	1	1	1
DIN16	1	X	X	X	X	**DOUT16**	1	X	X	X	X

Note: X denotes don't care

DATA TRANSFER

For each configured connection between a differential input pair and an enabled output pair, any data appearing at the input pair will be passed immediately through to the output pair.

CONFIGURATION

The S2018 can be selectively configured one output pair at a time, or any number of output pairs simultaneously. Configuration data is stored in 17 registers, one register for each output pair. The data in these 17 configurations register makes up the configuration register file. As shown in Figure 2, the configuration data is passed in parallel from all 17 registers to a latch, which holds the active switch configuration. This two-stage arrangement allows one or more output pairs to be configured simultaneously. A Chip Select pin (CSN) is provided to simplify interfacing this switch to the system microprocessor.

The S2018 minimizes the configuration time through the use of the active configuration latch. While the switch is operational, and prior to the time at which it must be reconfigured, a new configuration is loaded into the configuration register file. Once the configuration register file contains the desired connection information, the contents of the registers are transferred in parallel to the active configuration latch by the CONFIGN strobe.

To connect an output to a given input, the output to be configured is selected using the OADDR[4:0] (OADDR4=MSB) inputs. See Table 1. With the output configuration register selected, the desired input selection must be provided in the IADDR[4:0] (IADDR4=MSB) inputs. The IADDR[4:0] information is stored into the selected output configuration register by the LOADN strobe. The configuration process is described by the flow chart in Figure 5.

The active configuration latch can be made transparent by activating the CONFIGN input. When this is done, changes strobed into the output pair configuration registers by the LOADN input pair will be passed immediately to the switch.

The S2018 supports both broadcast and multicast operation: any of the 17 differential input pairs can be connected to any or all of the 17 differential output pairs.

Table 2. Output Swing Adjust Pin Settings

Vadjust1	Vadjust2	Vadjust3	DOUTxx (mVpp Diff.)
T	O	O	240
O	T	O	440
T	T	O	600
O	O	T	780
T	O	T	940
O	T	T	1100
T	T	T	1260

Note: T = Ties pin(s) VADJUSTx to pin VCSHIGH
O = Open

OUTPUT SWING ADJUST

The S2018 output swing can be adjusted by connecting one or more of the VADJUSTx pins to the VCSHIGH pin according to Table 2. Note that as the output swing is increased, the power dissipated by the part is proportionally increased (See Table 10).

Figure 3. Data Transfer Waveforms

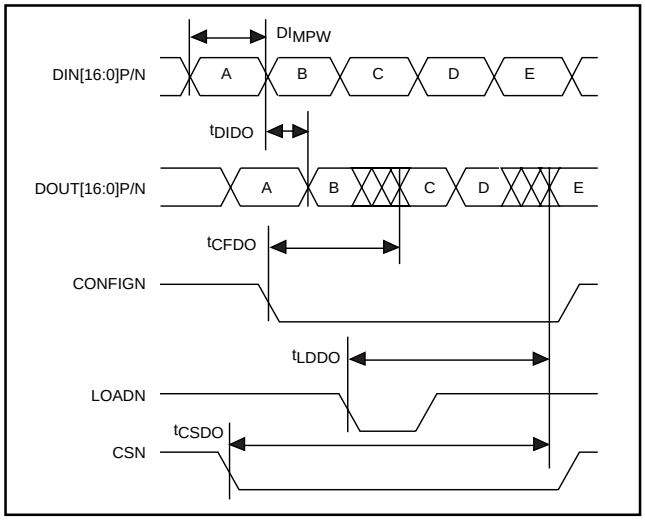


Figure 4. Reconfiguration Waveforms

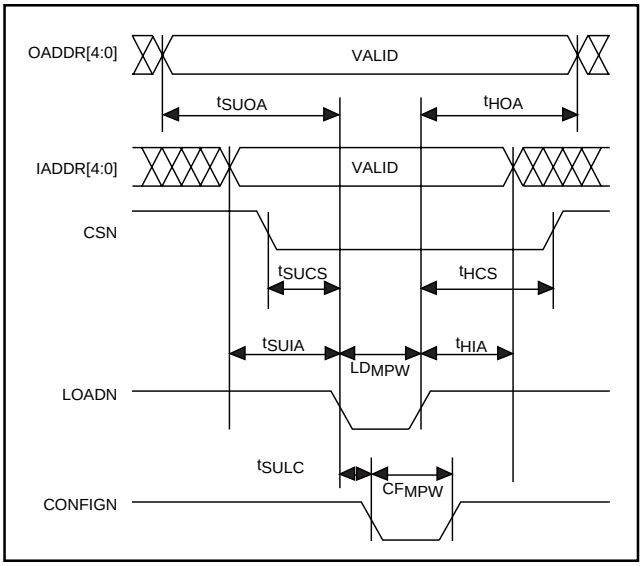


Figure 5. S2018 Configuration Flow Chart

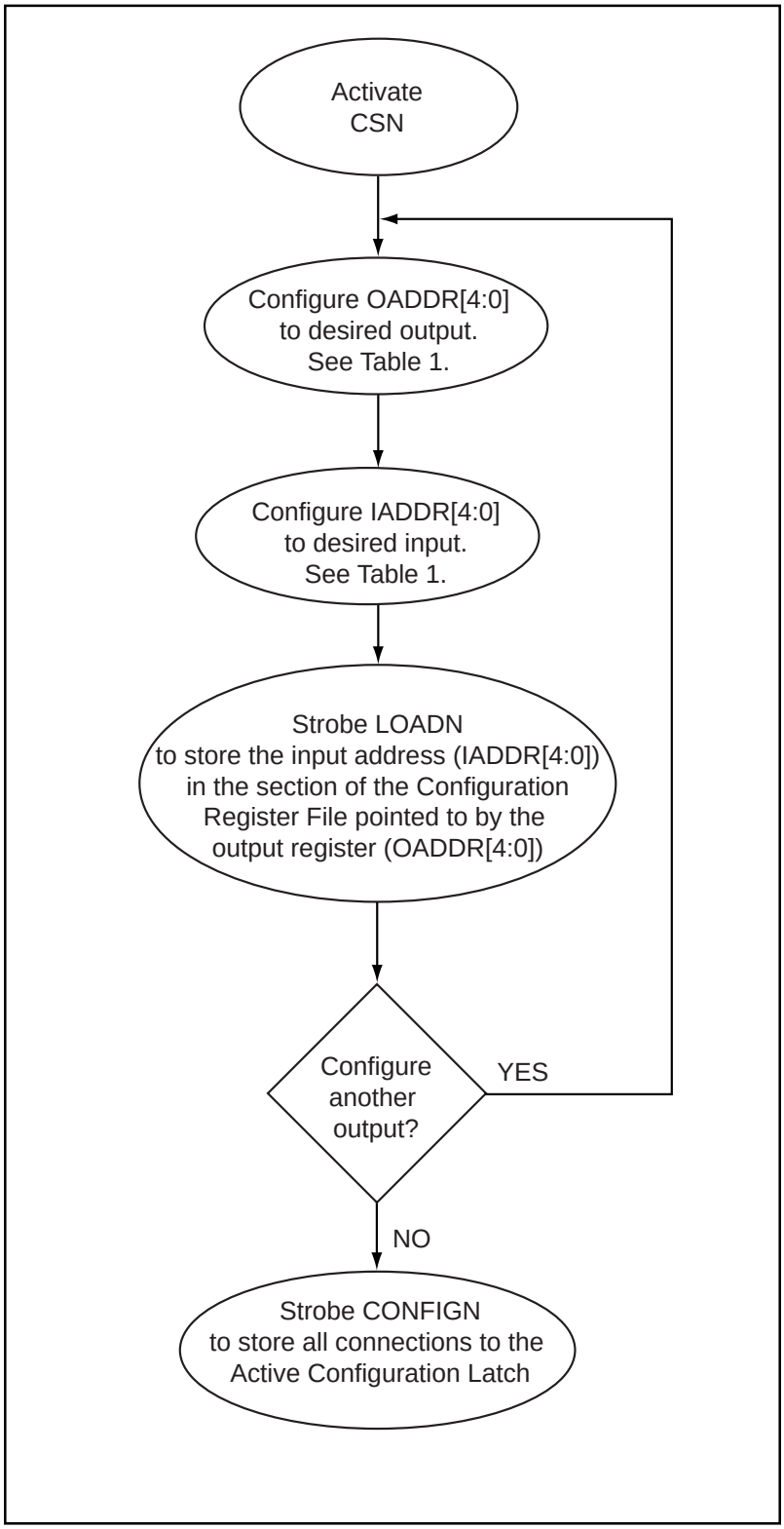


Table 3. Data Transfer Timing[1,2]

Parameter	Description	Min	Typ	Max	Units	Conditions
t_{DIDO}	Propagation delay from DIN[16:0]P/N to DOUT[16:0]P/N			1.5	ns	
t_{CFDO}	Propagation delay from falling edge of CONFIGN to DOUT[16:0]P/N valid			3	ns	
t_{LDDO}	Propagation delay from falling edge of LOADN to DOUT[16:0]P/N valid (when CONFIGN is held Low)			4	ns	
t_{CSDO}	Propagation delay from falling edge of CSN to DOUT[16:0]P/N valid (when CONFIGN is held Low)			10	ns	
DI_{MPW}	Pulse width of DIN[15:0]P/N	280			ps	
$DI16_{MPW}$	Pulse width of DIN16P/N	90			ps	
F_{MAX}	Data Rate			3.2	Gbps	
$T_{jitterRMS}$	Random jitter accumulation, any input to any output at: 3.2 Gbps 2.5 Gbps 1.5 Gbps		 1.9 1.9 1.9	 3 3 3	ps	RMS output jitter accumulated with K28.7 code.Tested on a sample basis.
$T_{jitterDJ}$	Deterministic jitter accumulation, any input to any output: 3.2 Gbps 2.5 Gbps 1.5 Gbps		 19 18 18	 27 27 27	ps	Deterministic output jitter accumulated K28.5 pattern. Tested on a sample basis. Peak-to-peak.
Skewone	Broadcast skew between paths from any one input (DIN[15:0]) to multiple outputs (DOUT[15:0]). Excludes DIN[16] and DOUT[16].			140	ps	
Skewall	Skew between paths from multiple inputs (DIN[15:0]) to multiple outputs (DOUT[15:0]). Excludes DIN[16] and DOUT[16].			150	ps	
Skewone16	Broadcast skew between paths from any one input (DIN[16:0]) to multiple outputs (DOUT[16:0]).			300	ps	
Skewall16	Skew between paths from multiple inputs (DIN[16:0]) to multiple outputs (DOUT[16:0]).			460	ps	
T_r, T_f	Output Edge Rate (20% to 80%)			125	ps	100 Ω line-to-line.

1. All data transfer timing measured from the crossing point of the differential inputs to the crossing point of the differential outputs.
2. All data measured with 800 mVpp swing.

Table 4. Reconfiguration Timing[1]

Parameter	Description	Min	Typ	Max	Units
t_{SUIA}	Setup time of IADDR[4:0] before falling edge of LOADN	0			ns
t_{HIA}	Hold time of IADDR[4:0] after rising edge of LOADN	2			ns
t_{SUOA}	Setup time of OADDR[4:0] before falling edge of LOADN	0			ns
t_{HOA}	Hold time of OADDR[4:0] after rising edge of LOADN	2			ns
t_{SULC}	Setup time of LOADN to CONFIGN so that the falling edge of CONFIGN will start reconfiguration	2			ns
t_{SUCS}	Setup time of CSN before falling edge of LOADN	0			ns
t_{HCS}	Hold time of CSN after rising edge of LOADN	0			ns
LD_{MPW}	Pulse width Low of LOADN	2			ns
CF_{MPW}	Pulse width Low of CONFIGN	2			ns
F_{MAX}	LOAD, CONFIGN			100	MHz

1. All reconfiguration timing measured from the 1.5 V point on the LVTTL signals.

Table 5. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
DIN16P DIN16N DIN15P DIN15N DIN14P DIN14N DIN13P DIN13N DIN12P DIN12N DIN11P DIN11N DIN10P DIN10N DIN9P DIN9N DIN8P DIN8N DIN7P DIN7N DIN6P DIN6N DIN5P DIN5N DIN4P DIN4N DIN3P DIN3N DIN2P DIN2N DIN1P DIN1N DIN0P DIN0N	Diff. LVPECL	I	J2 J1 G2 G1 E2 E1 A4 B4 A6 B6 A8 B8 A10 B10 A12 B12 A14 B14 AE13 AF13 AE11 AF11 AE9 AF9 AE7 AF7 AE5 AF5 AB2 AB1 Y2 Y1 V2 V1	Input data. Differential. Internally terminated with 100 Ω line-to-line. Internally DC biased to V_{CC} -0.84 V.
OADDR4 OADDR3 OADDR2 OADDR1 OADDR0	LVTTL	I	P1 R2 R1 T2 T1	Output address. Used to select an output configuration register in the configuration register file. See Table 1.
IADDR4 IADDR3 IADDR2 IADDR1 IADDR0	LVTTL	I	N2 M2 M1 L2 L1	Input address. IADDR[4:0] selects the input pair to connect to the output pair selected by OADDR[4:0]. See Table 1.
LOADN	LVTTL	I	P2	Load strobe. Active Low. When active, stores the configuration data in IADDR[4:0] into the configuration register file.
CONFIGN	LVTTL	I	N3	Configuration strobe. Active Low. When active, parallel loads the contents of the configuration register file into the active configuration latch.
VCSHIGH		I	AF23	Output Voltage swing adjust. Tie to VADJUSTx pin(s) to set output voltage swing. See Table 2 for details.

Table 5. Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
VADJUST1 VADJUST2 VADJUST3		O	AE23 AC25 AC26	Voltage adjust. These three pins, selectively tied to VCSHIGH, create a coded output which sets the output voltage swing. See Table 2.
CSN	LVTTL	I	N1	Chip select. Active Low. When inactive, the LOADN signal will be ignored. New addresses will not be allowed. When active, the S2018 will operate as specified.
DOUT16P DOUT16N DOUT15P DOUT15N DOUT14P DOUT14N DOUT13P DOUT13N DOUT12P DOUT12N DOUT11P DOUT11N DOUT10P DOUT10N DOUT9P DOUT9N DOUT8P DOUT8N DOUT7P DOUT7N DOUT6P DOUT6N DOUT5P DOUT5N DOUT4P DOUT4N DOUT3P DOUT3N DOUT2P DOUT2N DOUT1P DOUT1N DOUT0P DOUT0N	Diff. CML	O	N26 N25 L26 L25 J26 J25 G26 G25 E26 E25 B23 A23 B21 A21 B19 A19 B17 A17 AF16 AE16 AF18 AE18 AF20 AE20 AF22 AE22 AA26 AA25 W26 W25 U26 U25 R26 R25	Output data. Differential.

Table 6. Power and Ground Signals

Pin Name	Quantity	I/O	Pin #	Description
VCCINPUT	27		A1, A2, A11, B1, B2, B11, C3, C11, C15, D4, D11, D15, F1, F2, V3, V4, AC1, AC2, AC4, AC9, AC13, AD3, AD9, AE1, AE2, AF1, AF2	+3.3 V power supply. Power for high speed inputs.
GNDINPUT	60		A3, A15, A24, B3, B15, B24, C1, C2, C4, C12, C23, C25, C26, D3, D12, D24, D25, D26, F3, F4, K3, K4, L3, L4, M3, M4, N4, R3, R4, T3, T4, U1, U2, U3, U4, W1, W2, W3, W4, AC3, AC10, AC24, AD1, AD2, AD4, AD10, AD13, AD23, AD25, AD26, AE3, AE4, AE10, AE24, AE26, AF3, AF4, AF10, AF24, AF25	Ground for high speed inputs.
TTLVCC	16		C16, D16, J24, K1, K2, P3, AC7, AC23, AD7, AD24, AE14, AE17, AE25, AF14, AF17, AF26	+3.3 V power supply. Power for TTL inputs.
TTLGND	14		A16, B16, J3, J4, J23, P4, AC8, AC14, AC17, AD8, AD14, AD17, AE8, AF8	Ground for TTL inputs.
VCCCORE	31		A5, A7, A9, A13, B5, B7, B9, B13, C5, C7, C9, C13, C17, D1, D2, D5, D7, D9, D13, G3, G4, R24, Y3, Y4, AB3, AC5, AC11, AD5, AD11, AE15, AF15	+3.3 V power supply. Core circuitry power.
GNDCORE	31		C6, C8, C10, C14, D6, D8, D10, D14, D17, E3, E4, H1, H2, H3, H4, R23, AA1, AA2, AA3, AA4, AB4, AC6, AC12, AC15, AD6, AD12, AD15, AE6, AE12, AF6, AF12	Core circuitry ground.

Table 6. Power and Ground Signals (Continued)

Pin Name	Quantity	I/O	Pin #	Description
VCCADJUST	1		AB24	Power for VADJUST input.
GNDADJUST	1		AB23	Ground for VADJUST input.
VCC	50		A18, A20, A22, A25, A26, B18, B20, B22, B25, B26, C18, C20, C24, D18, D20, D23, F23, F24, F25, F26, H23, H24, K23, K24, K25, K26, M23, M24, M25, M26, P23, P24, T23, T24, T25, T26, V23, V24, V25, V26, Y25, Y26, AA23, AA24, AC16, AC18, AC20, AD18, AD20, AD22	+3.3 V power supply for high speed outputs.
GND	36		C19, C21, C22, D19, D21, D22, E23, E24, G23, G24, H25, H26, L23, L24, N23, N24, P25, P26, U23, U24, W23, W24, Y23, Y24, AB25, AB26, AC19, AC21, AC22, AD16, AD19, AD21, AE19, AE21, AF19, AF21	Ground for high speed outputs.

Figure 6. S2018 Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VCC INPUT	VCC INPUT	GND INPUT	DIN13P	VCC CORE	DIN12P	VCC CORE	DIN11P	VCC CORE	DIN10P	VCC INPUT	DIN9P	VCC CORE	DIN8P	GND INPUT	TTLGND	DOUT8N	VCC	DOUT9N	VCC	DOUT10N	VCC	DOUT11N	GND INPUT	VCC	VCC
B	VCC INPUT	VCC INPUT	GND INPUT	DIN13N	VCC CORE	DIN12N	VCC CORE	DIN11N	VCC CORE	DIN10N	VCC INPUT	DIN9N	VCC CORE	DIN8N	GND INPUT	TTLGND	DOUT8P	VCC	DOUT9P	VCC	DOUT10P	VCC	DOUT11P	GND INPUT	VCC	VCC
C	GND INPUT	GND INPUT	VCC INPUT	GND INPUT	VCC CORE	GND CORE	VCC CORE	GND CORE	VCC CORE	GND CORE	VCC INPUT	GND INPUT	VCC CORE	GND CORE	VCC INPUT	TTLVCC	VCC CORE	VCC	GND	VCC	GND	GND	GND INPUT	VCC	GND INPUT	GND INPUT
D	VCC CORE	VCC CORE	GND INPUT	VCC INPUT	VCC CORE	GND CORE	VCC CORE	GND CORE	VCC CORE	GND CORE	VCC INPUT	GND INPUT	VCC CORE	GND CORE	VCC INPUT	TTLVCC	GND CORE	VCC	GND	VCC	GND	GND	VCC	GND INPUT	GND INPUT	GND INPUT
E	DIN14N	DIN14P	GND CORE	GND CORE																			GND	GND	DOUT12N	DOUT12P
F	VCC INPUT	VCC INPUT	GND INPUT	GND INPUT																			VCC	VCC	VCC	VCC
G	DIN15N	DIN15P	VCC CORE	VCC CORE																			GND	GND	DOUT13N	DOUT13P
H	GND CORE	GND CORE	GND CORE	GND CORE																			VCC	VCC	GND	GND
J	DIN16N	DIN16P	TTLGND	TTLGND																			TTLGND	TTLVCC	DOUT14N	DOUT14P
K	TTLVCC	TTLVCC	GND INPUT	GND INPUT																			VCC	VCC	VCC	VCC
L	IADDR0	IADDR1	GND INPUT	GND INPUT																			GND	GND	DOUT15N	DOUT15P
M	IADDR2	IADDR3	GND INPUT	GND INPUT																			VCC	VCC	VCC	VCC
N	CSN	IADDR4	CONFIGN	GND INPUT																			GND	GND	DOUT16N	DOUT16P
P	OADDR4	LOADN	TTLVCC	TTLGND																			VCC	VCC	GND	GND
R	OADDR2	OADDR3	GND INPUT	GND INPUT																			GND CORE	VCC CORE	DOUT0N	DOUT0P
T	OADDR0	OADDR1	GND INPUT	GND INPUT																			VCC	VCC	VCC	VCC
U	GND INPUT	GND INPUT	GND INPUT	GND INPUT																			GND	GND	DOUT1N	DOUT1P
V	DIN0N	DIN0P	VCC INPUT	VCC INPUT																			VCC	VCC	VCC	VCC
W	GND INPUT	GND INPUT	GND INPUT	GND INPUT																			GND	GND	DOUT2N	DOUT2P
Y	DIN1N	DIN1P	VCC CORE	VCC CORE																			GND	GND	VCC	VCC
AA	GND CORE	GND CORE	GND CORE	GND CORE																			VCC	VCC	DOUT3N	DOUT3P
AB	DIN2N	DIN2P	VCC CORE	GND CORE																			GND ADJUST	VCC ADJUST	GND	GND
AC	VCC INPUT	VCC INPUT	GND INPUT	VCC INPUT	VCC CORE	GND CORE	TTLVCC	TTLGND	VCC INPUT	GND INPUT	VCC CORE	GND CORE	VCC INPUT	TTLGND	GND CORE	VCC	TTLGND	VCC	GND	VCC	GND	GND	TTLVCC	GND INPUT	VADJUST-2	VADJUST-3
AD	GND INPUT	GND INPUT	VCC INPUT	GND INPUT	VCC CORE	GND CORE	TTLVCC	TTLGND	VCC INPUT	GND INPUT	VCC CORE	GND CORE	GND INPUT	TTLGND	GND CORE	GND	TTLGND	VCC	GND	VCC	GND	VCC	GND INPUT	TTLVCC	GND INPUT	GND INPUT
AE	VCC INPUT	VCC INPUT	GND INPUT	GND INPUT	DIN3P	GND CORE	DIN4P	TTLGND	DIN5P	GND INPUT	DIN6P	GND CORE	DIN7P	TTLVCC	VCC CORE	DOUT7N	TTLVCC	DOUT6N	GND	DOUT5N	GND	DOUT4N	VADJUST-1	GND INPUT	TTLVCC	GND INPUT
AF	VCC INPUT	VCC INPUT	GND INPUT	GND INPUT	DIN3N	GND CORE	DIN4N	TTLGND	DIN5N	GND INPUT	DIN6N	GND CORE	DIN7N	TTLVCC	VCC CORE	DOUT7P	TTLVCC	DOUT6P	GND	DOUT5P	GND	DOUT4P	VCSHIGH	GND INPUT	GND INPUT	TTLVCC

TB - 352 Pin SBGA

(Top View)

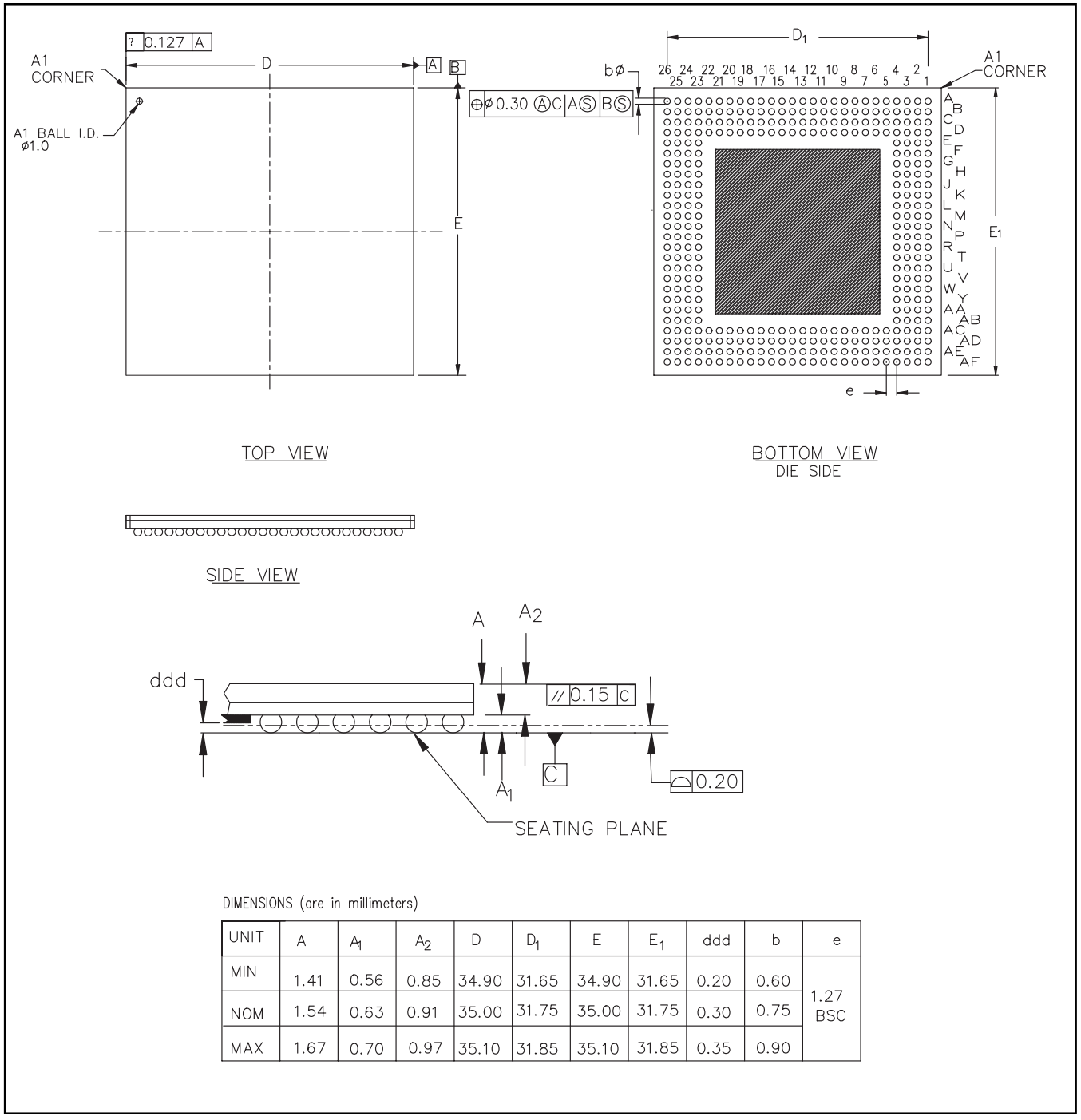
Figure 7. S2018 Pinout (Bottom View)

26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VCC	VCC	GND INPUT	DOUT11N	VCC	DOUT10N	VCC	DOUT9N	VCC	DOUT8N	TTLGND	GND INPUT	DIN8P	VCC CORE	DIN9P	VCC INPUT	DIN10P	VCC CORE	DIN11P	VCC CORE	DIN12P	VCC CORE	DIN13P	GND INPUT	VCC INPUT	VCC INPUT	A
VCC	VCC	GND INPUT	DOUT11P	VCC	DOUT10P	VCC	DOUT9P	VCC	DOUT8P	TTLGND	GND INPUT	DIN8N	VCC CORE	DIN9N	VCC INPUT	DIN10N	VCC CORE	DIN11N	VCC CORE	DIN12N	VCC CORE	DIN13N	GND INPUT	VCC INPUT	VCC INPUT	B
GND INPUT	GND INPUT	VCC	GND INPUT	GND	GND	VCC	GND	VCC	VCC CORE	TTLVCC	VCC INPUT	GND CORE	VCC CORE	GND INPUT	VCC INPUT	GND CORE	VCC CORE	GND CORE	VCC CORE	GND CORE	VCC CORE	GND INPUT	VCC INPUT	GND INPUT	GND INPUT	C
GND INPUT	GND INPUT	GND INPUT	VCC	GND	GND	VCC	GND	VCC	GND CORE	TTLVCC	VCC INPUT	GND CORE	VCC CORE	GND INPUT	VCC INPUT	GND CORE	VCC CORE	GND CORE	VCC CORE	GND CORE	VCC CORE	VCC INPUT	GND INPUT	VCC CORE	VCC CORE	D
DOUT12P	DOUT12N	GND	GND																			GND CORE	GND CORE	DIN14P	DIN14N	E
VCC	VCC	VCC	VCC																			GND INPUT	GND INPUT	VCC INPUT	VCC INPUT	F
DOUT13P	DOUT13N	GND	GND																			VCC CORE	VCC CORE	DIN15P	DIN15N	G
GND	GND	VCC	VCC																			GND CORE	GND CORE	GND CORE	GND CORE	H
DOUT14P	DOUT14N	TTLVCC	TTLGND																			TTLGND	TTLGND	DIN16P	DIN16N	J
VCC	VCC	VCC	VCC																			GND INPUT	GND INPUT	TTLVCC	TTLVCC	K
DOUT15P	DOUT15N	GND	GND																			GND INPUT	GND INPUT	IADDR1	IADDR0	L
VCC	VCC	VCC	VCC																			GND INPUT	GND INPUT	IADDR3	IADDR2	M
DOUT16P	DOUT16N	GND	GND																			GND INPUT	CONFIGN	IADDR4	CSN	N
GND	GND	VCC	VCC																			TTLGND	TTLVCC	LOADN	OADDR4	P
DOUT0P	DOUT0N	VCC CORE	GND CORE																			GND INPUT	GND INPUT	OADDR3	OADDR2	R
VCC	VCC	VCC	VCC																			GND INPUT	GND INPUT	OADDR1	OADDR0	T
DOUT1P	DOUT1N	GND	GND																			GND INPUT	GND INPUT	GND INPUT	GND INPUT	U
VCC	VCC	VCC	VCC																			VCC INPUT	VCC INPUT	DIN0P	DIN0N	V
DOUT2P	DOUT2N	GND	GND																			GND INPUT	GND INPUT	GND INPUT	GND INPUT	W
VCC	VCC	GND	GND																			VCC CORE	VCC CORE	DIN1P	DIN1N	Y
DOUT3P	DOUT3N	VCC	VCC																			GND CORE	GND CORE	GND CORE	GND CORE	AA
GND	GND	VCC ADJUST	GND ADJUST																			GND CORE	VCC CORE	DIN2P	DIN2N	AB
VADJUST-3	VADJUST-2	GND INPUT	TTLVCC	GND	GND	VCC	GND	VCC	TTLGND	VCC	GND CORE	TTLGND	VCC INPUT	GND CORE	VCC CORE	GND INPUT	VCC INPUT	TTLGND	TTLVCC	GND CORE	VCC CORE	VCC INPUT	GND INPUT	VCC INPUT	VCC INPUT	AC
GND INPUT	GND INPUT	TTLVCC	GND INPUT	VCC	GND	VCC	GND	VCC	TTLGND	GND	GND CORE	TTLGND	GND INPUT	GND CORE	VCC CORE	GND INPUT	VCC INPUT	TTLGND	TTLVCC	GND CORE	VCC CORE	GND INPUT	VCC INPUT	GND INPUT	GND INPUT	AD
GND INPUT	TTLVCC	GND INPUT	VADJUST-1	DOUT4N	GND	DOUT5N	GND	DOUT6N	TTLVCC	DOUT7N	VCC CORE	TTLVCC	DIN7P	GND CORE	DIN6P	GND INPUT	DIN5P	TTLGND	DIN4P	GND CORE	DIN3P	GND INPUT	GND INPUT	VCC INPUT	VCC INPUT	AE
TTLVCC	GND INPUT	GND INPUT	VCSHIGH	DOUT4P	GND	DOUT5P	GND	DOUT6P	TTLVCC	DOUT7P	VCC CORE	TTLVCC	DIN7N	GND CORE	DIN6N	GND INPUT	DIN5N	TTLGND	DIN4N	GND CORE	DIN3N	GND INPUT	GND INPUT	VCC INPUT	VCC INPUT	AF

TB - 352 Pin SBGA

(Bottom View)

Figure 8. 35 mm x 35 mm 352 Pin SBGA Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	ddd	b	e
MIN	1.41	0.56	0.85	34.90	31.65	34.90	31.65	0.20	0.60	1.27 BSC
NOM	1.54	0.63	0.91	35.00	31.75	35.00	31.75	0.30	0.75	
MAX	1.67	0.70	0.97	35.10	31.85	35.10	31.85	0.35	0.90	

THERMAL MANAGEMENT

The S2018 requires thermal management. AMCC recommends the HTS263NF-D heat sink available from

Chip Coolers
333 Strawberry Field Road
Warwick, RI 02886

Phone: 401-739-7600 or 800-227-0254
Fax: 401-732-6119
Web: www.chipcoolers.com

The NF option refers to 'No Fan'. The HTS263NF-D package outline drawing is provided in Figure 9.

Airflow requirement is determined by

$Pd = (T_{j\ max} - T_{a\ max}) / \theta_{ja}$, $\theta_{ja} = \theta_{jc} + \theta_{ca}$

where $T_{j\ max}$ is the maximum junction temperature

$T_{a\ max}$ is the maximum ambient temperature

θ_{ja} is the thermal dissipation coefficient from junction to ambient

θ_{jc} is the thermal dissipation coefficient from junction to case

θ_{ca} is the thermal dissipation coefficient from case to ambient (if a heat sink is used, this is θ_{sa} - sink to ambient)

Tables 7 and 8 show max package power vs. airlfow, calculated using the equation above with $T_{j\ max}$ = 125 ˚C and $T_{a\ max}$ = 70 ˚C. In order to successfully use the S2018, the max package power must exceed the specified max power dissipation of the device, which is determined by the output swing setting (See Table 10).

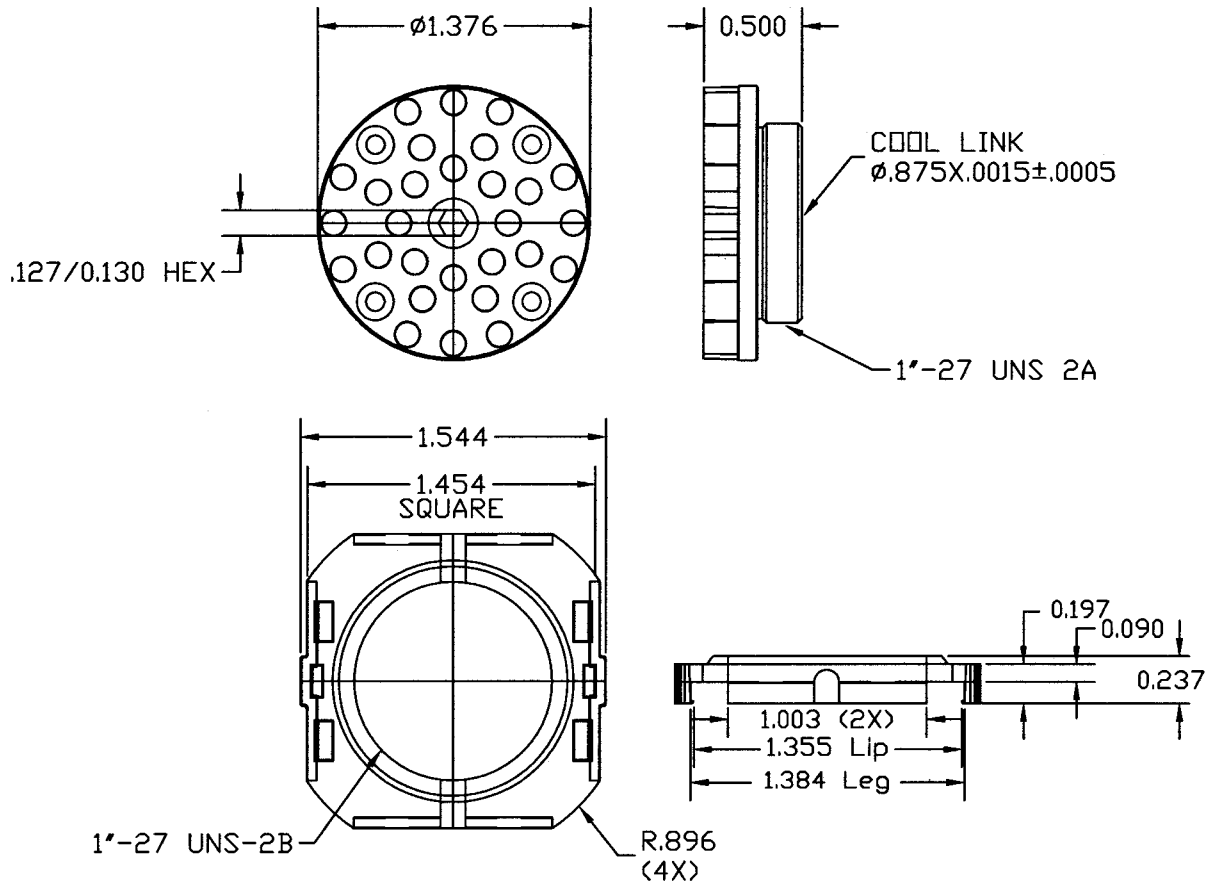
Table 7. S2018 Power Dissapation vs. Air Flow, No Heat Sink

Max Package Power (W)	Air Flow (LFPM)	θ_{ja} (˚C/W)	θ_{jc} (˚C/W)
3.44	0	16.0	0.72
3.79	100	14.5	0.72
4.40	200	12.5	0.72

Table 8. S2018 Power Dissapation vs. Air Flow, HTS263NF-D heat sink

Max Package Power (W)	Air Flow (LFPM)	θ_{ja} with HTS263NF-D Heat Sink (˚C/W)	HTS263NF-D θ_{sa} (˚C/W)
4.07	0	13.5	12.78
5.24	100	10.5	11.78
6.47	200	8.5	7.78

Figure 9. S2018 HTS263NF-D Heat Sink Outline Drawing



NOTE:

1. HEATSINK MATERIAL: ALUMINUM
2. MOUNTING CLIP MATERIAL: 50% GLASS FILLED PPA PLASTIC
3. HEATSINK FINISH: BLACK ANODIZE
4. THERMAL INTERFACE: COOL LINK
5. TOLERANCE: ±.005" UNLESS OTHERWISE NOTED.

Table 9. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on any Power Pin w.r.t. GND	-0.5		4	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
Voltage on any LVTTL Input Pin	-0.5		3.47	V
High Speed CML Output Source Current			30	mA

Electrostatic Discharge (ESD) Ratings

The S2018 is rated to the following ESD voltages based on the human body model:
1. All pins are rated at 100 V.

Table 10. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-40		70	˚C
Junction Temperature Under Bias			125	˚C
Voltage on any Power Pin w.r.t. GND	3.135	3.3	3.465	V
Voltage on any LVPECL Input Pin	V_{CC}-2		V_{CC}	V
Voltage on any LVTTL Input Pin	0		3.47	V
I_{CC} Supply Current (with 240 mV output swing)		0.89	1.14	A
I_{CC} Supply Current (with 440 mV output swing)		1.0	1.27	A
I_{CC} Supply Current (with 600 mV output swing)		1.09	1.49	A
I_{CC} Supply Current (with 780 mV output swing)		1.19	1.52	A
I_{CC} Supply Current (with 940 mV output swing)		1.28	1.62	A
I_{CC} Supply Current (with 1100 mV output swing)		1.37	1.73	A
I_{CC} Supply Current (with 1260 mV output swing)		1.45	1.80	A
Power Dissipation (with 240 mV output swing)		2.95	3.97	W
Power Dissipation (with 440 mV output swing)		3.29	4.41	W
Power Dissipation (with 600 mV output swing)		3.61	5.17	W
Power Dissipation (with 780 mV output swing)		3.92	5.27	W
Power Dissipation (with 940 mV output swing)		4.22	5.62	W
Power Dissipation (with 1100 mV output swing)		4.51	6.01	W
Power Dissipation (with 1260 mV output swing)		4.80	6.25	W

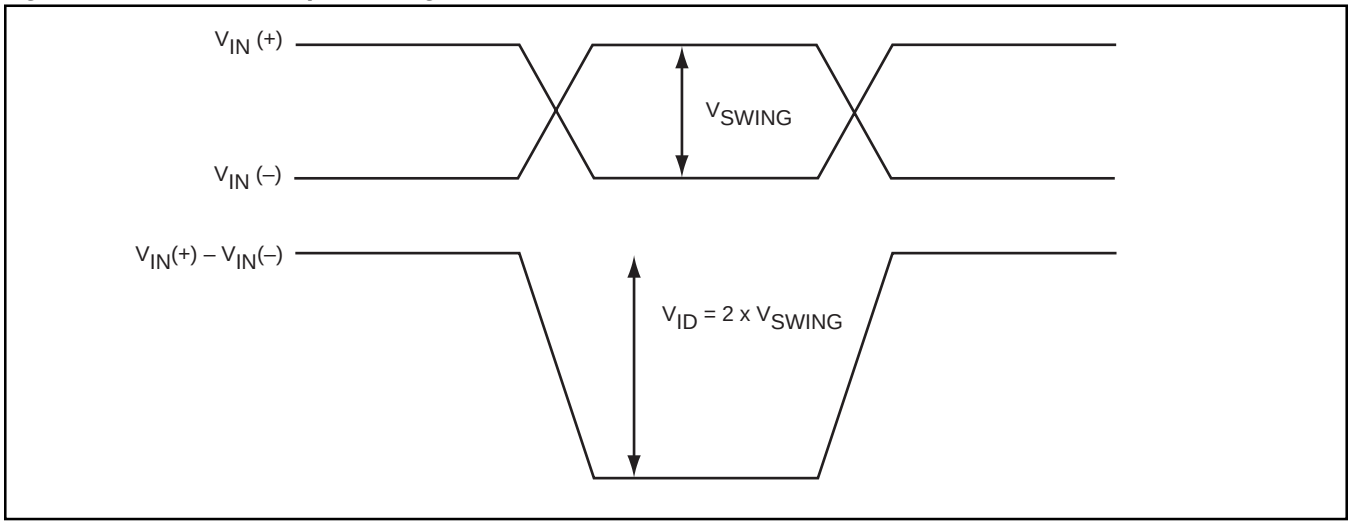
Table 11. Input and Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
LVTTL Inputs						
V_{IH}	Input High Voltage	2		V_{CC} +0.5	V	V_{CC} = Max
V_{IL}	Input Low Voltage	0		0.8	V	V_{CC} = Max
I_{IH}	Input High Current			50	µA	VIN = 2.4 V
I_{IL}	Input Low Current	-500			µA	VIN = 0.5 V
ΔV_{HYST}	Magnitude of hysteresis		120		mV	
LVPECL Inputs						
V_{ID}	Differential Input Voltage Swing	200		1400	mVpp	See Figure 10.
V_{BIAS}	Internal Voltage Bias Point for the Differential Inputs	V_{CC} -1.0	V_{CC} -0.84	V_{CC} -0.75	V	See Figure 10.
I_{IH}	Input High Current			15	mA	V_{ID}= Max
I_{IL}	Input Low Current	-15			mA	V_{ID} = Max
R_{DIFF}	Differential Input Impedance	80	100	120	Ω	
CML Outputs						
V_{OH}	CML Output High Voltage (with 240 mV output swing)	V_{CC} -0.20		V_{CC} -0.01	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with 240 mV output swing)	V_{CC} -0.35		V_{CC} -0.05	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OH}	CML Output High Voltage (with 440 mV output swing)	V_{CC} -0.24		V_{CC} -0.04	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with 440 mV output swing)	V_{CC} -0.50		V_{CC} -0.15	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OH}	CML Output High Voltage (with 600 mV output swing)	V_{CC} -0.29		V_{CC} -0.09	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with 600 mV output swing)	V_{CC} -0.65		V_{CC} -0.25	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OH}	CML Output High Voltage (with 780 mV output swing)	V_{CC} -0.36		V_{CC} -0.14	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with 780 mV output swing)	V_{CC} -0.80		V_{CC} -0.35	V	100 Ω line-to-line. (without AC coupling caps.)

Table 11. Input Output DC Characteristics (Continued)

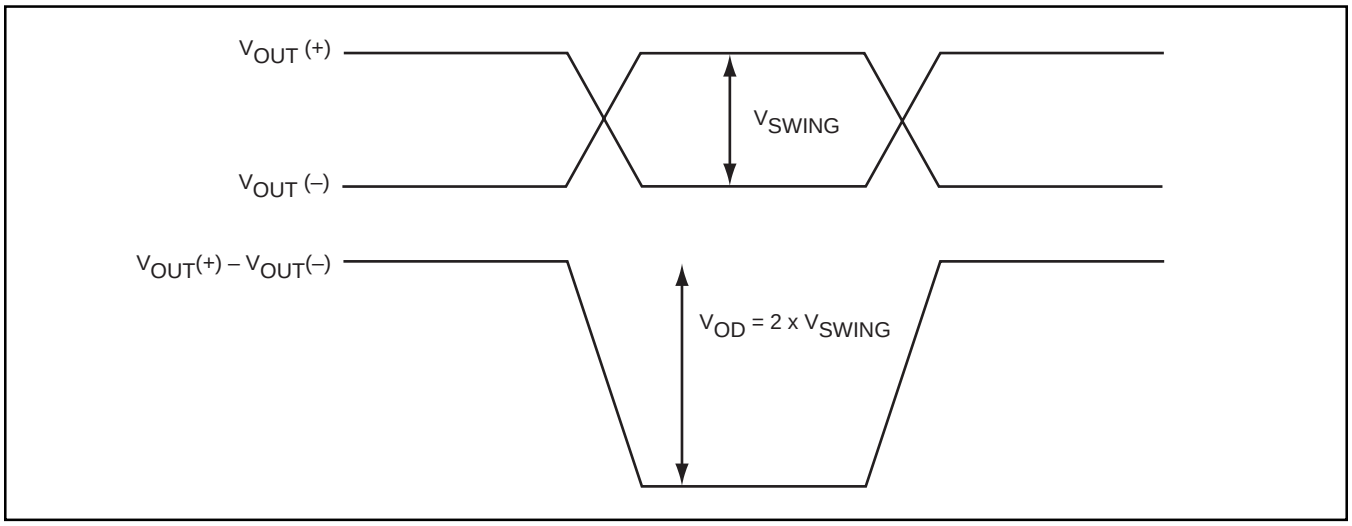
Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	CML Output High Voltage (with 940 mV output swing)	V_{CC} -0.42		V_{CC} -0.19	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with 940 mV output swing)	V_{CC} -1.00		V_{CC} -0.45	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OH}	CML Output High Voltage (with 1100 mV output swing)	V_{CC} -0.50		V_{CC} -0.20	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with 1100 mV output swing)	V_{CC} -1.15		V_{CC} -0.55	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OH}	CML Output High Voltage (with 1260 mV output swing)	V_{CC} -0.55		V_{CC} -0.21	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OL}	CML Output Low Voltage (with 1260 mV output swing)	V_{CC} -1.35		V_{CC} -0.65	V	100 Ω line-to-line. (without AC coupling caps.)
V_{OD}	CML Output Differential Voltage Swing	200	240	276	mVpp	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 11.
V_{OD}	CML Output Differential Voltage Swing	374	440	506	mVpp	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 11.
V_{OD}	CML Output Differential Voltage Swing	510	600	690	mVpp	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 11.
V_{OD}	CML Output Differential Voltage Swing	663	780	897	mVpp	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 11.
V_{OD}	CML Output Differential Voltage Swing	799	940	1081	mVpp	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 11.
V_{OD}	CML Output Differential Voltage Swing	935	1100	1265	mVpp	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 11.
V_{OD}	CML Output Differential Voltage Swing	1071	1260	1449	mVpp	100 Ω line-to-line. See Table 2 for output swing settings. See Figure 11.
R_O	Output Impedance (Single Ended)	50	60	70	Ω	

Figure 10. Differential Input Voltage



Note: $V_{IN}(+) – V_{IN}(-)$ is the algebraic difference of the input signals.

Figure 11. Differential Output Voltage



Note: $V_{OUT}(+) – V_{OUT}(-)$ is the algebraic difference of the input signals.

Figure 12. Differential CML Output to +3.3 V or +5 V PECL Input AC Coupled Termination

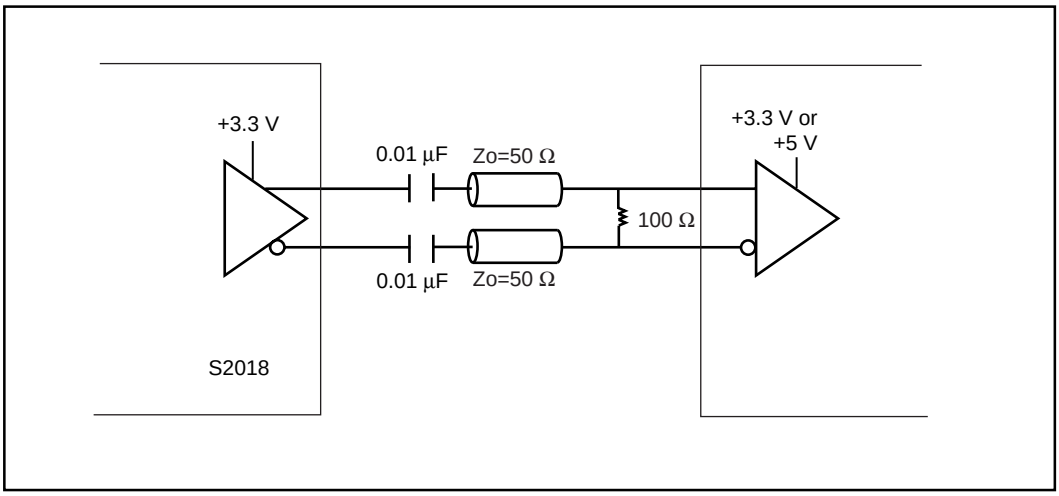
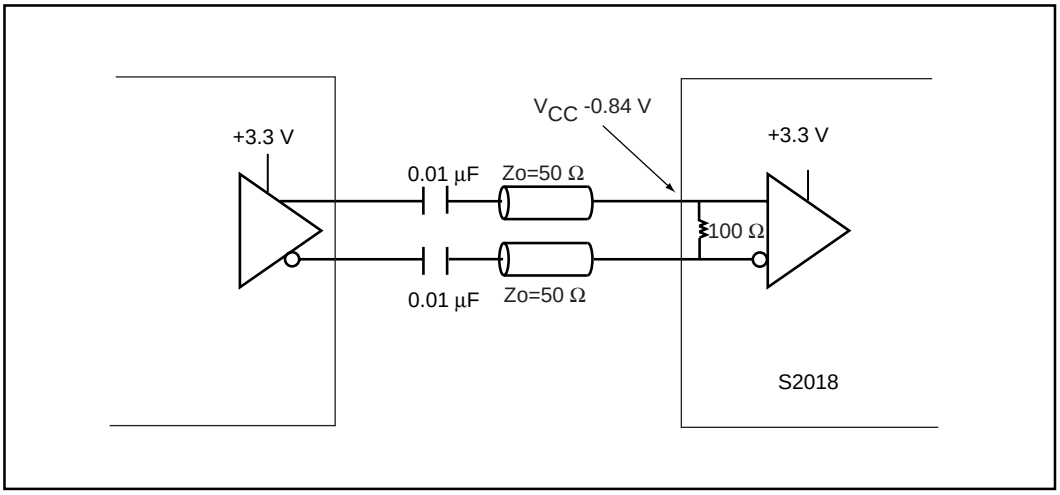
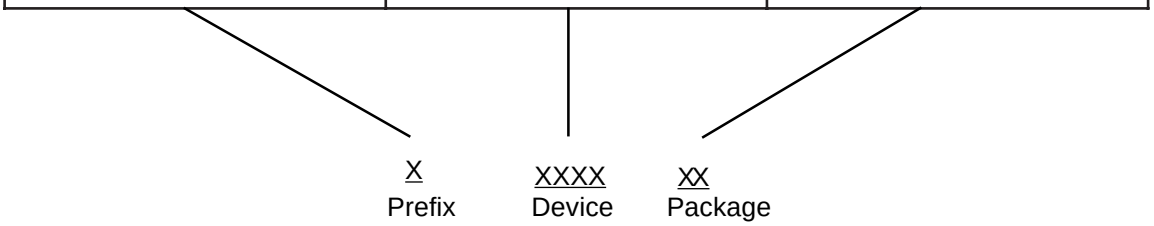


Figure 13. Differential LVPECL Inputs



Heat Sink Ordering Information

PREFIX	DEVICE	PACKAGE
S –Integrated Circuit	2018	TB – 352 SBGA



Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121
Phone: (858) 450-9333 • (800) 755-2622 • Fax: (858) 450-9885
http://www.amcc.com