

# MOS INTEGRATED CIRCUIT

## $\mu$ PD4482161, 4482181, 4482321, 4482361

### 8M-BIT CMOS SYNCHRONOUS FAST SRAM FLOW THROUGH OPERATION

#### Description

The  $\mu$ PD4482161 is a 524,288-word by 16-bit, the  $\mu$ PD4482181 is a 524,288-word by 18-bit, the  $\mu$ PD4482321 is a 262,144-word by 32-bit and the  $\mu$ PD4482361 is a 262,144-word by 36-bit synchronous static RAM fabricated with advanced CMOS technology using Full-CMOS six-transistor memory cell.

The  $\mu$ PD4482161,  $\mu$ PD4482181,  $\mu$ PD4482321 and  $\mu$ PD4482361 integrate unique synchronous peripheral circuitry, 2-bit burst counter and output buffer as well as SRAM core. All input registers are controlled by a positive edge of the single clock input (CLK).

The  $\mu$ PD4482161,  $\mu$ PD4482181,  $\mu$ PD4482321 and  $\mu$ PD4482361 are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration, such as cache and buffer memory.

ZZ has to be set LOW at the normal operation. When ZZ is set HIGH, the SRAM enters Power Down State ("Sleep"). In the "Sleep" state, the SRAM internal state is preserved. When ZZ is set LOW again, the SRAM resumes normal operation.

The  $\mu$ PD4482161,  $\mu$ PD4482181,  $\mu$ PD4482321 and  $\mu$ PD4482361 are packaged in 100-pin PLASTIC LQFP with a 1.4 mm package thickness for high density and low capacitive loading.

#### Features

- 3.3 V or 2.5 V core supply
- Synchronous operation
- ★ • Operating temperature :  $T_A = 0$  to  $70$  °C (-A65, -A75, -A85, -C75, -C85)  
 $T_A = -40$  to  $+85$  °C (-A65Y, -A75Y, -A85Y, -C75Y, -C85Y)
- Internally self-timed write control
- Burst read / write : Interleaved burst and linear burst sequence
- Fully registered inputs for flow through operation
- All registers triggered off positive clock edge
- 3.3 V or 2.5 V LVTTTL Compatible : All inputs and outputs
- Fast clock access time : 6.5 ns (133 MHz), 7.5 ns (117 MHz), 8.5 ns (100 MHz)
- Asynchronous output enable : /G
- Burst sequence selectable : MODE
- Sleep mode : ZZ (ZZ = Open or Low : Normal operation)
- Separate byte write enable : /BW1 to /BW4, /BWE ( $\mu$ PD4482321,  $\mu$ PD4482361)  
/BW1, /BW2, /BWE ( $\mu$ PD4482161,  $\mu$ PD4482181)
- Global write enable : /GW
- Three chip enables for easy depth expansion
- Common I/O using three state outputs

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★ Ordering Information

(1/2)

Part number	Access Time ns	Clock Frequency MHz	Core Supply Voltage V	I/O Interface	Operating Temperature °C	Package	
μPD4482161GF-A65	6.5	133	3.3 ± 0.165	3.3 V LVTTTL <sup>Note</sup>	0 to 70	100-pin PLASTIC LQFP (14 × 20)	
μPD4482161GF-A75	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482161GF-A85	8.5	100					
μPD4482181GF-A65	6.5	133		3.3 V LVTTTL <sup>Note</sup>			
μPD4482181GF-A75	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482181GF-A85	8.5	100					
μPD4482321GF-A65	6.5	133		3.3 V LVTTTL <sup>Note</sup>			
μPD4482321GF-A75	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482321GF-A85	8.5	100					
μPD4482361GF-A65	6.5	133		3.3 V LVTTTL <sup>Note</sup>			
μPD4482361GF-A75	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482361GF-A85	8.5	100					
μPD4482161GF-C75	7.5	117		2.5 ± 0.125			2.5 V LVTTTL
μPD4482161GF-C85	8.5	100					
μPD4482181GF-C75	7.5	117					
μPD4482181GF-C85	8.5	100					
μPD4482321GF-C75	7.5	117					
μPD4482321GF-C85	8.5	100					
μPD4482361GF-C75	7.5	117					
μPD4482361GF-C85	8.5	100					

**Note** Although 2.5V LVTTTL interface can also be used, a performance becomes equivalent to -A75 (117 MHz).

Part number	Access Time ns	Clock Frequency MHz	Core Supply Voltage V	I/O Interface	Operating Temperature °C	Package	
μPD4482161GF-A65Y	6.5	133	3.3 ± 0.165	3.3 V LVTTTL <sup>Note</sup>	-40 to +85	100-pin PLASTIC LQFP (14 × 20)	
μPD4482161GF-A75Y	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482161GF-A85Y	8.5	100					
μPD4482181GF-A65Y	6.5	133		3.3 V LVTTTL <sup>Note</sup>			
μPD4482181GF-A75Y	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482181GF-A85Y	8.5	100					
μPD4482321GF-A65Y	6.5	133		3.3 V LVTTTL <sup>Note</sup>			
μPD4482321GF-A75Y	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482321GF-A85Y	8.5	100					
μPD4482361GF-A65Y	6.5	133		3.3 V LVTTTL <sup>Note</sup>			
μPD4482361GF-A75Y	7.5	117		3.3 V or 2.5 V LVTTTL			
μPD4482361GF-A85Y	8.5	100					
μPD4482161GF-C75Y	7.5	117		2.5 ± 0.125			2.5 V LVTTTL
μPD4482161GF-C85Y	8.5	100					
μPD4482181GF-C75Y	7.5	117					
μPD4482181GF-C85Y	8.5	100					
μPD4482321GF-C75Y	7.5	117					
μPD4482321GF-C85Y	8.5	100					
μPD4482361GF-C75Y	7.5	117					
μPD4482361GF-C85Y	8.5	100					

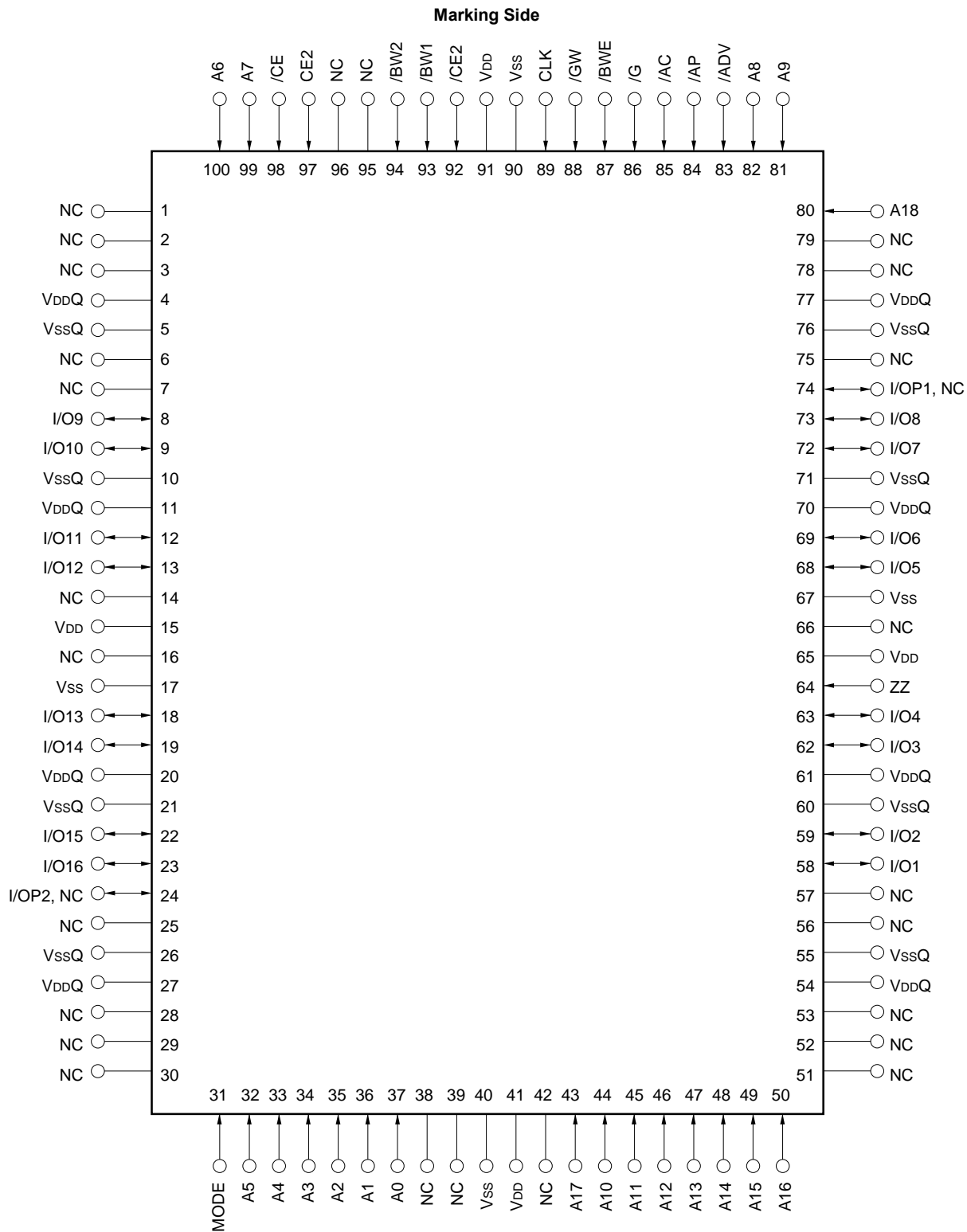
**Note** Although 2.5V LVTTTL interface can also be used, a performance becomes equivalent to -A75Y (117 MHz).

Pin Configurations

/xxx indicates active low signal.

100-pin PLASTIC LQFP (14 x 20)

[μPD4482161GF, μPD4482181GF]



Remark Refer to Package Drawing for the 1-pin index mark.

Pin Identification ( $\mu$ PD4482161GF,  $\mu$ PD4482181GF)

Symbol	Pin No.	Description
A0 to A18	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43, 80	Synchronous Address Input
I/O1 to I/O16	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC <sup>Note</sup>	74	Synchronous Data In (Parity),
I/OP2, NC <sup>Note</sup>	24	Synchronous / Asynchronous Data Out (Parity)
/ADV	83	Synchronous Burst Address Advance Input
/AP	84	Synchronous Address Status Processor Input
/AC	85	Synchronous Address Status Controller Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/BW1, /BW2, /BWE	93, 94, 87	Synchronous Byte Write Enable Input
/GW	88	Synchronous Global Write Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
MODE	31	Asynchronous Burst Sequence Select Input Do not change state during normal operation
ZZ	64	Asynchronous Power Down State Input
VDD	15, 41, 65, 91	Power Supply
VSS	17, 40, 67, 90	Ground
VDDQ	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
VSSQ	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 51, 52, 53, 56, 57, 66, 75, 78, 79, 95, 96	No Connection

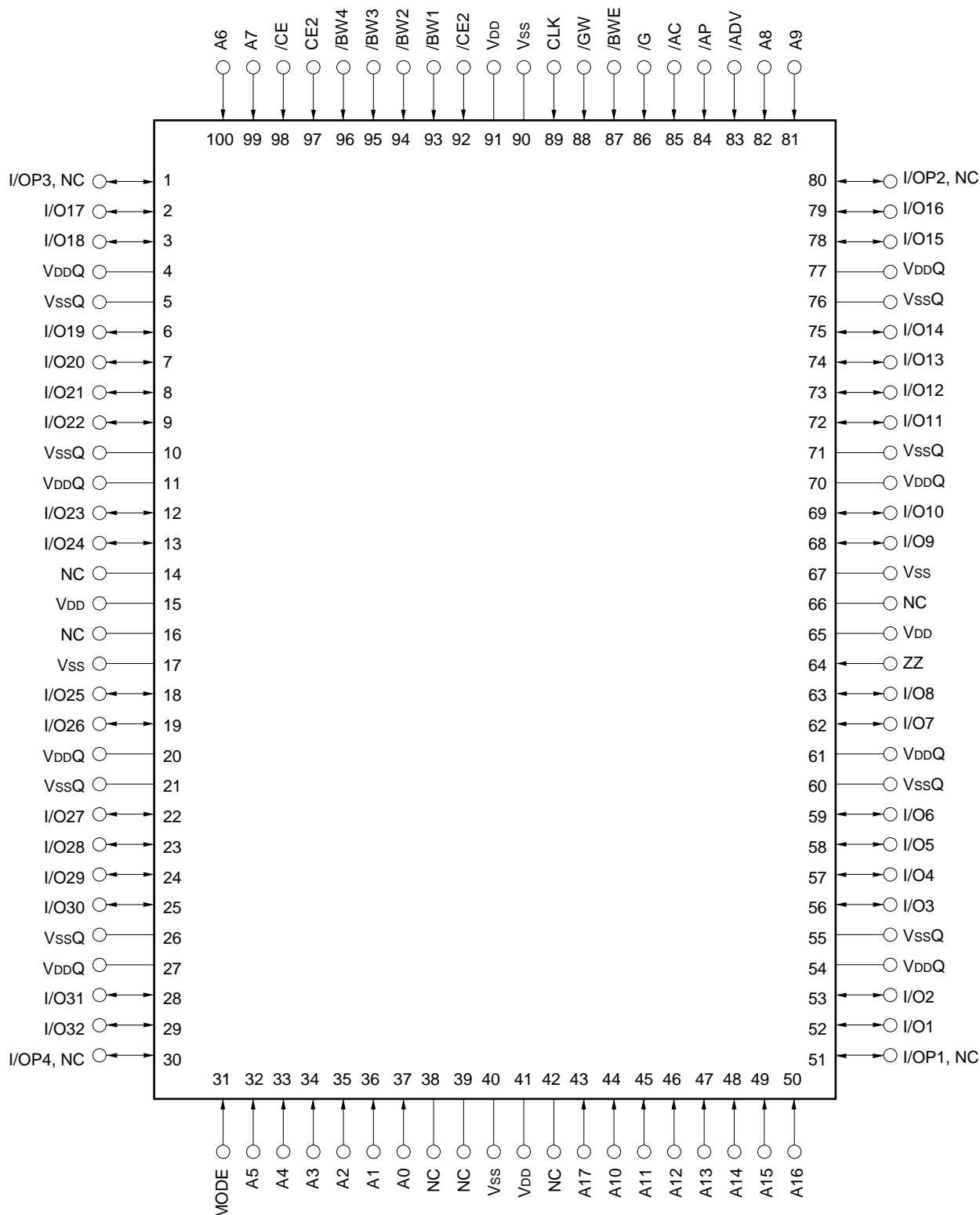
**Note** NC (No Connection) is used in the  $\mu$ PD4482161GF.

I/OP1 and I/OP2 are used in the  $\mu$ PD4482181GF.

100-pin PLASTIC LQFP (14 x 20)

[μPD4482321GF, μPD4482361GF]

Marking Side



Remark Refer to Package Drawing for the 1-pin index mark.

Pin Identification ( $\mu$ PD4482321GF,  $\mu$ PD4482361GF)

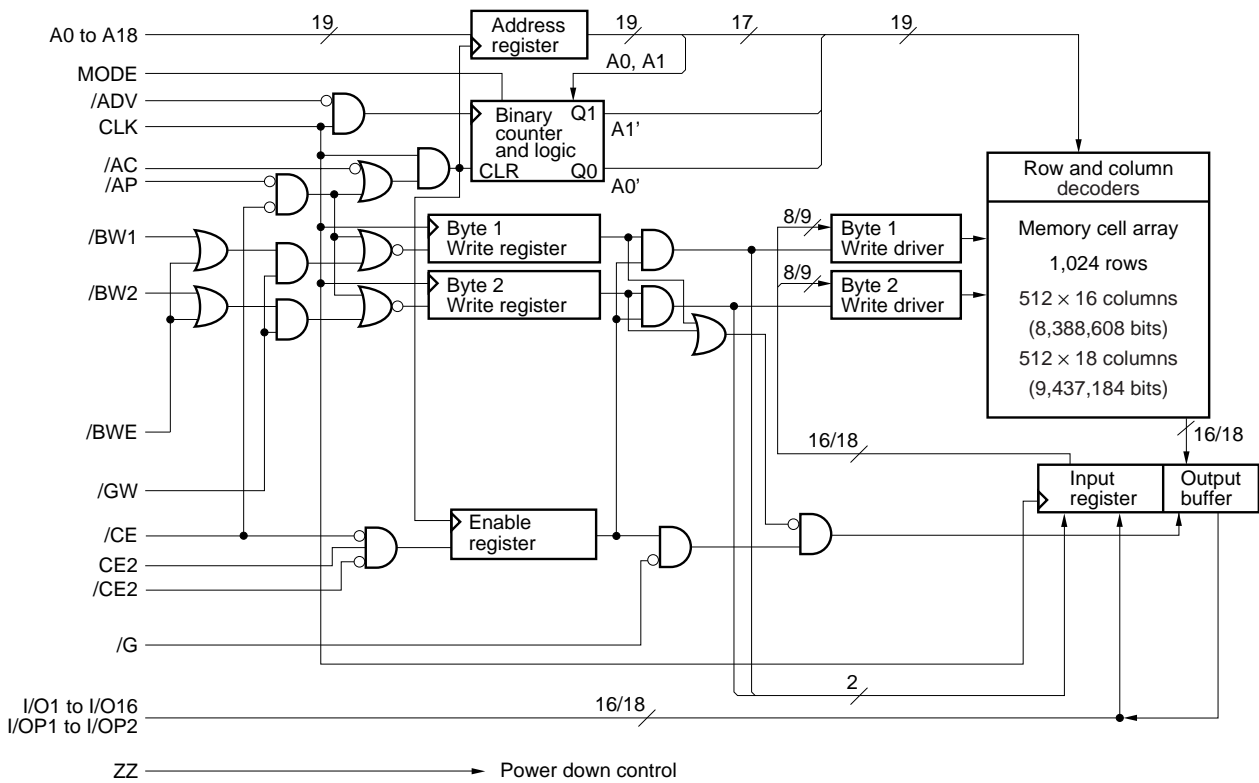
Symbol	Pin No.	Description
A0 to A17	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48, 49, 50, 43	Synchronous Address Input
I/O1 to I/O32	52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	Synchronous Data In, Synchronous / Asynchronous Data Out
I/OP1, NC <sup>Note</sup>	51	Synchronous Data In (Parity), Synchronous / Asynchronous Data Out (Parity)
I/OP2, NC <sup>Note</sup>	80	
I/OP3, NC <sup>Note</sup>	1	
I/OP4, NC <sup>Note</sup>	30	
/ADV	83	Synchronous Burst Address Advance Input
/AP	84	Synchronous Address Status Processor Input
/AC	85	Synchronous Address Status Controller Input
/CE, CE2, /CE2	98, 97, 92	Synchronous Chip Enable Input
/BW1 to /BW4, /BWE	93, 94, 95, 96, 87	Synchronous Byte Write Enable Input
/GW	88	Synchronous Global Write Input
/G	86	Asynchronous Output Enable Input
CLK	89	Clock Input
MODE	31	Asynchronous Burst Sequence Select Input Do not change state during normal operation
ZZ	64	Asynchronous Power Down State Input
V <sub>DD</sub>	15, 41, 65, 91	Power Supply
V <sub>SS</sub>	17, 40, 67, 90	Ground
V <sub>DDQ</sub>	4, 11, 20, 27, 54, 61, 70, 77	Output Buffer Power Supply
V <sub>SSQ</sub>	5, 10, 21, 26, 55, 60, 71, 76	Output Buffer Ground
NC	14, 16, 38, 39, 42, 66	No Connection

**Note** NC (No Connection) is used in the  $\mu$ PD4482321GF.

I/OP1 to I/OP4 are used in the  $\mu$ PD4482361GF.

**Block Diagrams**

[μPD4482161, μPD4482181]



**Burst Sequence**

[μPD4482161, μPD4482181]

**Interleaved Burst Sequence Table (MODE = VDD)**

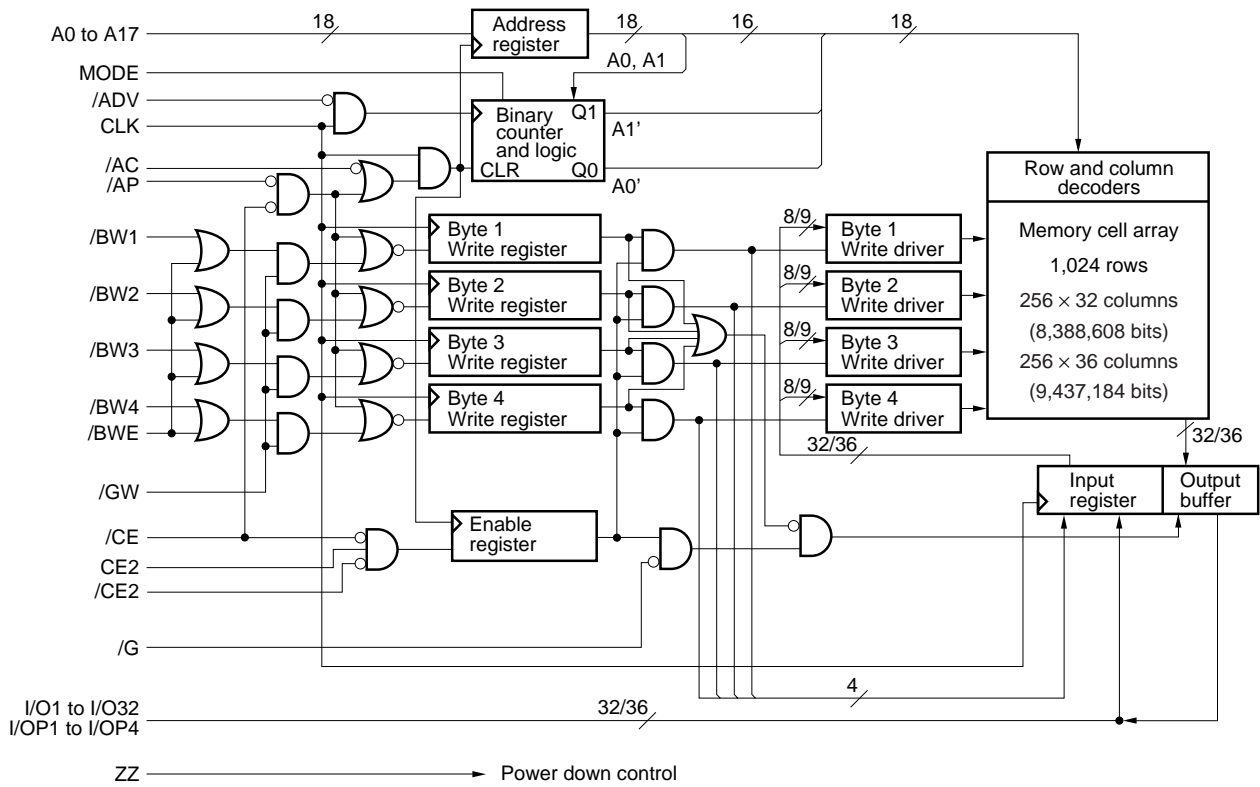
External Address	A18 to A2, A1, A0
1st Burst Address	A18 to A2, A1, /A0
2nd Burst Address	A18 to A2, /A1, A0
3rd Burst Address	A18 to A2, /A1, /A0

**Linear Burst Sequence Table (MODE = Vss)**

External Address	A18 to A2, 0, 0	A18 to A2, 0, 1	A18 to A2, 1, 0	A18 to A2, 1, 1
1st Burst Address	A18 to A2, 0, 1	A18 to A2, 1, 0	A18 to A2, 1, 1	A18 to A2, 0, 0
2nd Burst Address	A18 to A2, 1, 0	A18 to A2, 1, 1	A18 to A2, 0, 0	A18 to A2, 0, 1
3rd Burst Address	A18 to A2, 1, 1	A18 to A2, 0, 0	A18 to A2, 0, 1	A18 to A2, 1, 0



[μPD4482321, μPD4482361]



**Burst Sequence**

[μPD4482321, μPD4482361]

**Interleaved Burst Sequence Table (MODE = VDD)**

External Address	A17 to A2, A1, A0
1st Burst Address	A17 to A2, A1, /A0
2nd Burst Address	A17 to A2, /A1, A0
3rd Burst Address	A17 to A2, /A1, /A0

**Linear Burst Sequence Table (MODE = Vss)**

External Address	A17 to A2, 0, 0	A17 to A2, 0, 1	A17 to A2, 1, 0	A17 to A2, 1, 1
1st Burst Address	A17 to A2, 0, 1	A17 to A2, 1, 0	A17 to A2, 1, 1	A17 to A2, 0, 0
2nd Burst Address	A17 to A2, 1, 0	A17 to A2, 1, 1	A17 to A2, 0, 0	A17 to A2, 0, 1
3rd Burst Address	A17 to A2, 1, 1	A17 to A2, 0, 0	A17 to A2, 0, 1	A17 to A2, 1, 0

**Asynchronous Truth Table**

Operation	/G	I/O
Read Cycle	L	Dout
Read Cycle	H	High-Z
Write Cycle	×	High-Z, Din
Deselected	×	High-Z

**Remark** × : don't care

**Synchronous Truth Table**

Operation	/CE	CE2	/CE2	/AP	/AC	/ADV	/WRITE	CLK	Address
Deselected <sup>Note</sup>	H	×	×	×	L	×	×	L → H	None
Deselected <sup>Note</sup>	L	L	×	L	×	×	×	L → H	None
Deselected <sup>Note</sup>	L	×	H	L	×	×	×	L → H	None
Deselected <sup>Note</sup>	L	L	×	H	L	×	×	L → H	None
Deselected <sup>Note</sup>	L	×	H	H	L	×	×	L → H	None
Read Cycle / Begin Burst	L	H	L	L	×	×	×	L → H	External
Read Cycle / Begin Burst	L	H	L	H	L	×	H	L → H	External
Read Cycle / Continue Burst	×	×	×	H	H	L	H	L → H	Next
Read Cycle / Continue Burst	H	×	×	×	H	L	H	L → H	Next
Read Cycle / Suspend Burst	×	×	×	H	H	H	H	L → H	Current
Read Cycle / Suspend Burst	H	×	×	×	H	H	H	L → H	Current
Write Cycle / Begin Burst	L	H	L	H	L	×	L	L → H	External
Write Cycle / Continue Burst	×	×	×	H	H	L	L	L → H	Next
Write Cycle / Continue Burst	H	×	×	×	H	L	L	L → H	Next
Write Cycle / Suspend Burst	×	×	×	H	H	H	L	L → H	Current
Write Cycle / Suspend Burst	H	×	×	×	H	H	L	L → H	Current

**Note** Deselect status is held until new "Begin Burst" entry.

**Remarks 1.** × : don't care

**2.** /WRITE = L means any one or more byte write enables (/BW1, /BW2, /BW3 or /BW4) and /BWE are LOW or /GW is LOW.

/WRITE = H means the following two cases.

(1) /BWE and /GW are HIGH.

(2) /BW1 to /BW4 and /GW are HIGH, and /BWE is LOW.

**Partial Truth Table for Write Enables**

[μPD4482161, μPD4482181]

Operation	/GW	/BWE	/BW1	/BW2
Read Cycle	H	H	×	×
Read Cycle	H	L	H	H
Write Cycle / Byte 1 (I/O [1:8], I/OP1)	H	L	L	H
Write Cycle / Byte 2 (I/O [9:16], I/OP2)	H	L	H	L
Write Cycle / All Bytes	H	L	L	L
Write Cycle / All Bytes	L	×	×	×

**Remark** × : don't care

[μPD4482321, μPD4482361]

Operation	/GW	/BWE	/BW1	/BW2	/BW3	/BW4
Read Cycle	H	H	×	×	×	×
Read Cycle	H	L	H	H	H	H
Write Cycle / Byte 1 (I/O [1:8], I/OP1)	H	L	L	H	H	H
Write Cycle / Byte 2 (I/O [9:16], I/OP2)	H	L	H	L	H	H
Write Cycle / Byte 3 (I/O [17:24], I/OP3)	H	L	H	H	L	H
Write Cycle / Byte 4 (I/O [25:32], I/OP4)	H	L	H	H	H	L
Write Cycle / All Bytes	H	L	L	L	L	L
Write Cycle / All Bytes	L	×	×	×	×	×

**Remark** × : don't care

**ZZ (Sleep) Truth Table**

ZZ	Chip Status
≤ 0.2 V	Active
Open	Active
≥ V <sub>DD</sub> - 0.2 V	Sleep

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Notes
★ Supply voltage	V <sub>DD</sub>	-A65, -A75, -A85	-0.5		+4.0	V	
		-A65Y, -A75Y, -A85Y					
		-C75, -C85	-0.5		+3.0	V	
		-C75Y, -C85Y					
Output supply voltage	V <sub>DDQ</sub>		-0.5		V <sub>DD</sub>	V	
Input voltage	V <sub>IN</sub>		-0.5		V <sub>DD</sub> + 0.5	V	1, 2
Input / Output voltage	V <sub>I/O</sub>		-0.5		V <sub>DDQ</sub> + 0.5	V	1, 2
★ Operating ambient temperature	T <sub>A</sub>	-A65, -A75, -A85, -C75, -C85	0		70	°C	
		-A65Y, -A75Y, -A85Y, -C75Y, -C85Y	-40		+85		
Storage temperature	T <sub>stg</sub>		-55		+125	°C	

- Notes** 1. -2.0 V (MIN.)(Pulse width : 2 ns)  
 2. V<sub>DDQ</sub> + 2.3 V (MAX.)(Pulse width : 2 ns)

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions (1/2)**

Parameter	Symbol	Conditions	-A65, -A75, -A85 -A65Y, -A75Y, -A85Y			Unit
			MIN.	TYP.	MAX.	
Supply voltage	V <sub>DD</sub>		3.135	3.3	3.465	V
<b>2.5 V LVTTTL interface</b>						
Output supply voltage	V <sub>DDQ</sub>		2.375	2.5	2.9	V
High level input voltage	V <sub>IH</sub>		1.7		V <sub>DDQ</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>		+0.7	V
<b>3.3 V LVTTTL interface</b>						
Output supply voltage	V <sub>DDQ</sub>		3.135	3.3	3.465	V
High level input voltage	V <sub>IH</sub>		2.0		V <sub>DDQ</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>		+0.8	V

**Note** -0.8 V (MIN.)(Pulse width : 2 ns)

**Recommended DC Operating Conditions (2/2)**

Parameter	Symbol	Conditions	-C75, -C85 -C75Y, -C85Y			Unit
			MIN.	TYP.	MAX.	
Supply voltage	V <sub>DD</sub>		2.375	2.5	2.625	V
Output supply voltage	V <sub>DDQ</sub>		2.375	2.5	2.625	V
High level input voltage	V <sub>IH</sub>		1.7		V <sub>DDQ</sub> + 0.3	V
Low level input voltage	V <sub>IL</sub>		-0.3 <sup>Note</sup>		+0.7	V

**Note** -0.8 V (MIN.)(Pulse width : 2 ns)

**DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit	Note
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> (except ZZ, MODE) = 0 V to V <sub>DD</sub>	-2		+2	μA	
I/O leakage current	I <sub>LO</sub>	V <sub>I/O</sub> = 0 V to V <sub>DDQ</sub> , Outputs are disabled.	-2		+2	μA	
★ Operating supply current	I <sub>DD</sub>	Device selected, Cycle = MAX. V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA	-A65 -A65Y			250	mA
			-A75, -C75 -A75Y, -C75Y			225	
			-A85, -C85 -A85Y, -C85Y			200	
			I <sub>DD1</sub>	Suspend cycle, Cycle = MAX. /AC, /AP, /ADV, /GW, /BWEs ≥ V <sub>IH</sub> V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> , I <sub>I/O</sub> = 0 mA			
Standby supply current	I <sub>SB</sub>	Device deselected, Cycle = 0 MHz V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> , All inputs are static.			30	mA	
	I <sub>SB1</sub>	Device deselected, Cycle = 0 MHz V <sub>IN</sub> ≤ 0.2 V or V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2 V V <sub>I/O</sub> ≤ 0.2 V, All inputs are static.			15		
	I <sub>SB2</sub>	Device deselected, Cycle = MAX. V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub>			110		
Power down supply current	I <sub>SBZZ</sub>	ZZ ≥ V <sub>DD</sub> - 0.2 V, V <sub>I/O</sub> ≤ V <sub>DDQ</sub> + 0.2 V			15	mA	
<b>2.5 V LVTTTL interface</b>							
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0 mA	1.7			V	
		I <sub>OH</sub> = -1.0 mA	2.1				
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = +2.0 mA			0.7	V	
		I <sub>OL</sub> = +1.0 mA			0.4		
<b>3.3 V LVTTTL interface</b>							
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0 mA	2.4			V	
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = +8.0 mA			0.4	V	

**Capacitance (T<sub>A</sub> = 25 °C, f = 1 MHz)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0 V			6.0	pF
Input / Output capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V			8.0	pF
Clock input capacitance	C <sub>clk</sub>	V <sub>clk</sub> = 0 V			6.0	pF

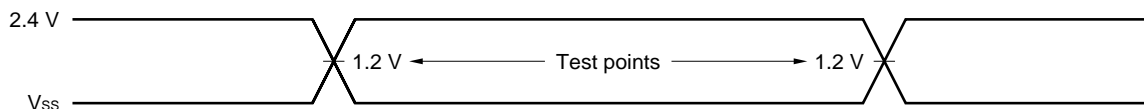
**Remark** These parameters are periodically sampled and not 100% tested.

**AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

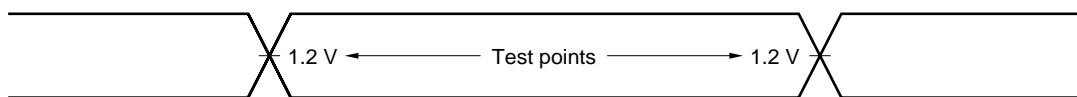
**AC Test Conditions**

**2.5 V LVTTTL interface**

**Input waveform (Rise / Fall time ≤ 2.4 ns)**

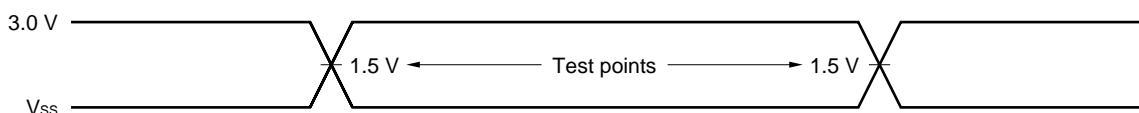


**Output waveform**

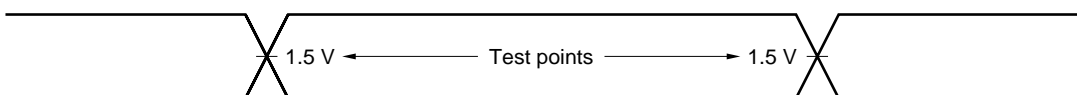


**3.3 V LVTTTL interface**

**Input waveform (Rise / Fall time ≤ 3.0 ns)**



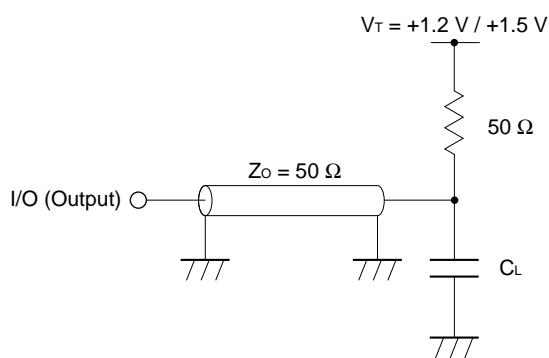
**Output waveform**



**Output load condition**

- CL : 30 pF
- 5 pF (TKHQX1, TKHQX2, TGLQX, TGHQZ, TKHQZ)

**External load at test**



**Remark**  $C_L$  includes capacitances of the probe and jig, and stray capacitances.

Read and Write Cycle (2.5 V LVTTTL Interface)

★

Parameter	Symbol		-A65, -A75, -C75 -A65Y, -A75Y, -C75Y (117 MHz)		-A85, -C85 -A85Y, -C85Y (100MHz)		Unit	Note
	Standard	Alias	MIN.	MAX.	MIN.	MAX.		
Cycle time	TKHKH	TCYC	8.6	–	10.0	–	ns	
Clock access time	TKHQV	TCD	–	7.5	–	8.5	ns	
Output enable access time	TGLQV	TOE	–	3.5	–	3.5	ns	
Clock high to output active	TKHQX1	TDC1	2.5	–	2.5	–	ns	
Clock high to output change	TKHQX2	TDC2	2.5	–	2.5	–	ns	
Output enable to output active	TGLQX	TOLZ	0	–	0	–	ns	
Output disable to output High-Z	TGHQZ	TOHZ	0	3.5	0	3.5	ns	
Clock high to output High-Z	TKHQZ	TCZ	2.5	5.0	2.5	5.0	ns	
Clock high pulse width	TKHKL	TCH	2.5	–	2.5	–	ns	
Clock low pulse width	TKLKH	TCL	2.5	–	2.5	–	ns	
Setup times	Address	TAVKH	TAS	1.5	–	2.0	–	ns
	Address status	TADSVKH	TSS					
	Data in	TDVKH	TDS					
	Write enable	TWVKH	TWS					
	Address advance	TADVVKH	–					
	Chip enable	TEVKH	–					
Hold times	Address	TKHAX	TAH	0.5	–	0.5	–	ns
	Address status	TKHADSX	TSH					
	Data in	TKHDX	TDH					
	Write enable	TKHWX	TWH					
	Address advance	TKHADVX	–					
	Chip enable	TKHEX	–					
Power down entry time	TZZE	TZZE	–	8.6	–	10.0	ns	
Power down recovery time	TZZR	TZZR	–	8.6	–	10.0	ns	

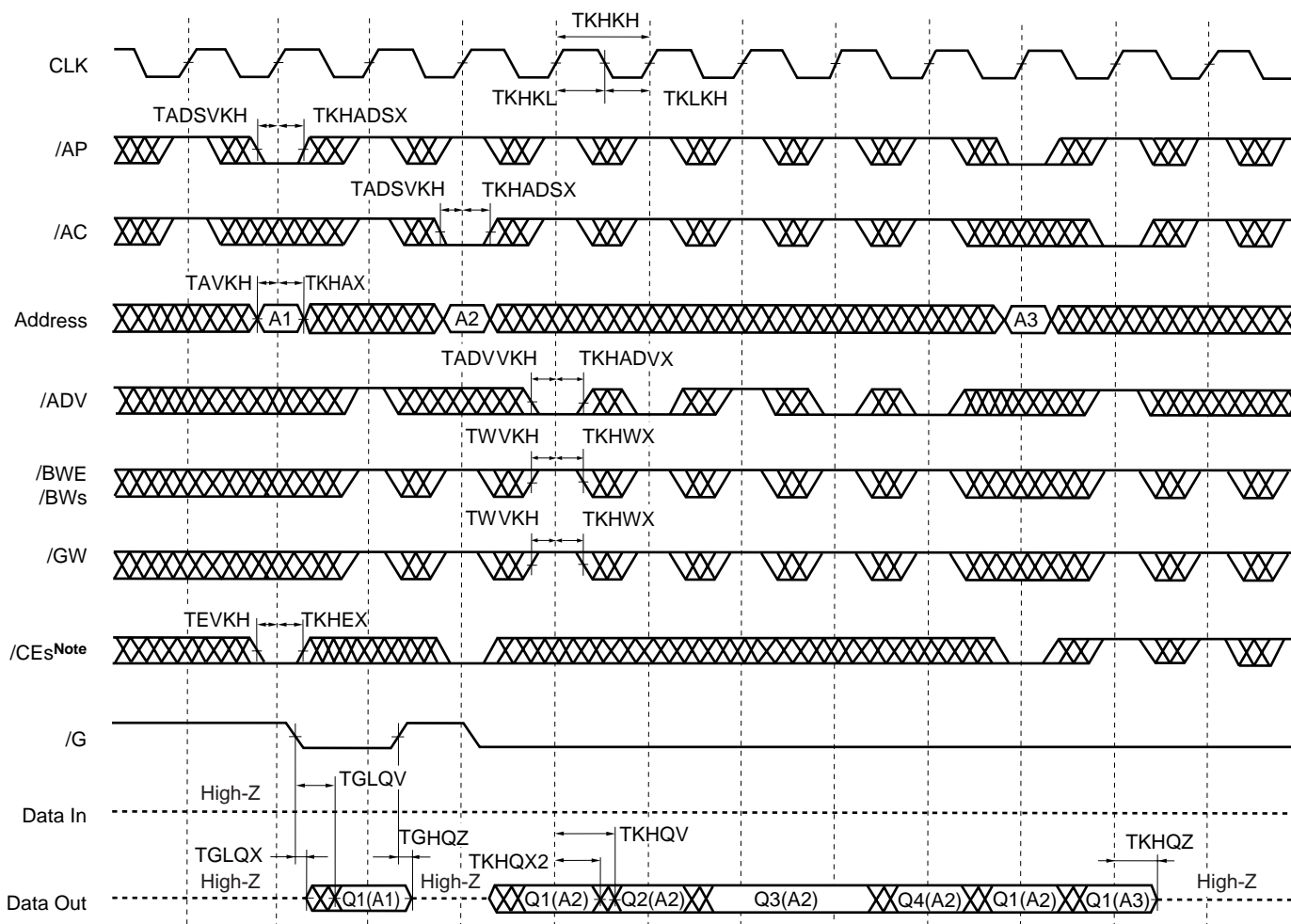
Read and Write Cycle (3.3 V LVTTTL Interface)

★

Parameter	Symbol		-A65 -A65Y (133 MHz)		-A75 -A75Y (117 MHz)		-A85 -A85Y (100MHz)		Unit	Note
	Standard	Alias	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Cycle time	TKHKH	TCYC	7.5	–	8.6	–	10.0	–	ns	
Clock access time	TKHQV	TCD	–	6.5	–	7.5	–	8.5	ns	
Output enable access time	TGLQV	TOE	–	3.5	–	3.5	–	3.5	ns	
Clock high to output active	TKHQX1	TDC1	2.5	–	2.5	–	2.5	–	ns	
Clock high to output change	TKHQX2	TDC2	2.5	–	2.5	–	2.5	–	ns	
Output enable to output active	TGLQX	TOLZ	0	–	0	–	0	–	ns	
Output disable to output High-Z	TGHQZ	TOHZ	0	3.5	0	3.5	0	3.5	ns	
Clock high to output High-Z	TKHQZ	TCZ	2.5	5.0	2.5	5.0	2.5	5.0	ns	
Clock high pulse width	TKHKL	TCH	2.5	–	2.5	–	2.5	–	ns	
Clock low pulse width	TKLKH	TCL	2.5	–	2.5	–	2.5	–	ns	
Setup times	Address	TAVKH	TAS	1.5	–	1.5	–	2.0	–	ns
	Address status	TADSVKH	TSS							
	Data in	TDVKH	TDS							
	Write enable	TWVKH	TWS							
	Address advance	TADVVKH	–							
	Chip enable	TEVKH	–							
Hold times	Address	TKHAX	TAH	0.5	–	0.5	–	0.5	–	ns
	Address status	TKHADSX	TSH							
	Data in	TKHDX	TDH							
	Write enable	TKHWX	TWH							
	Address advance	TKHADVX	–							
	Chip enable	TKHEX	–							
Power down entry time	TZZE	TZZE	–	7.5	–	8.6	–	10.0	ns	
Power down recovery time	TZZR	TZZR	–	7.5	–	8.6	–	10.0	ns	



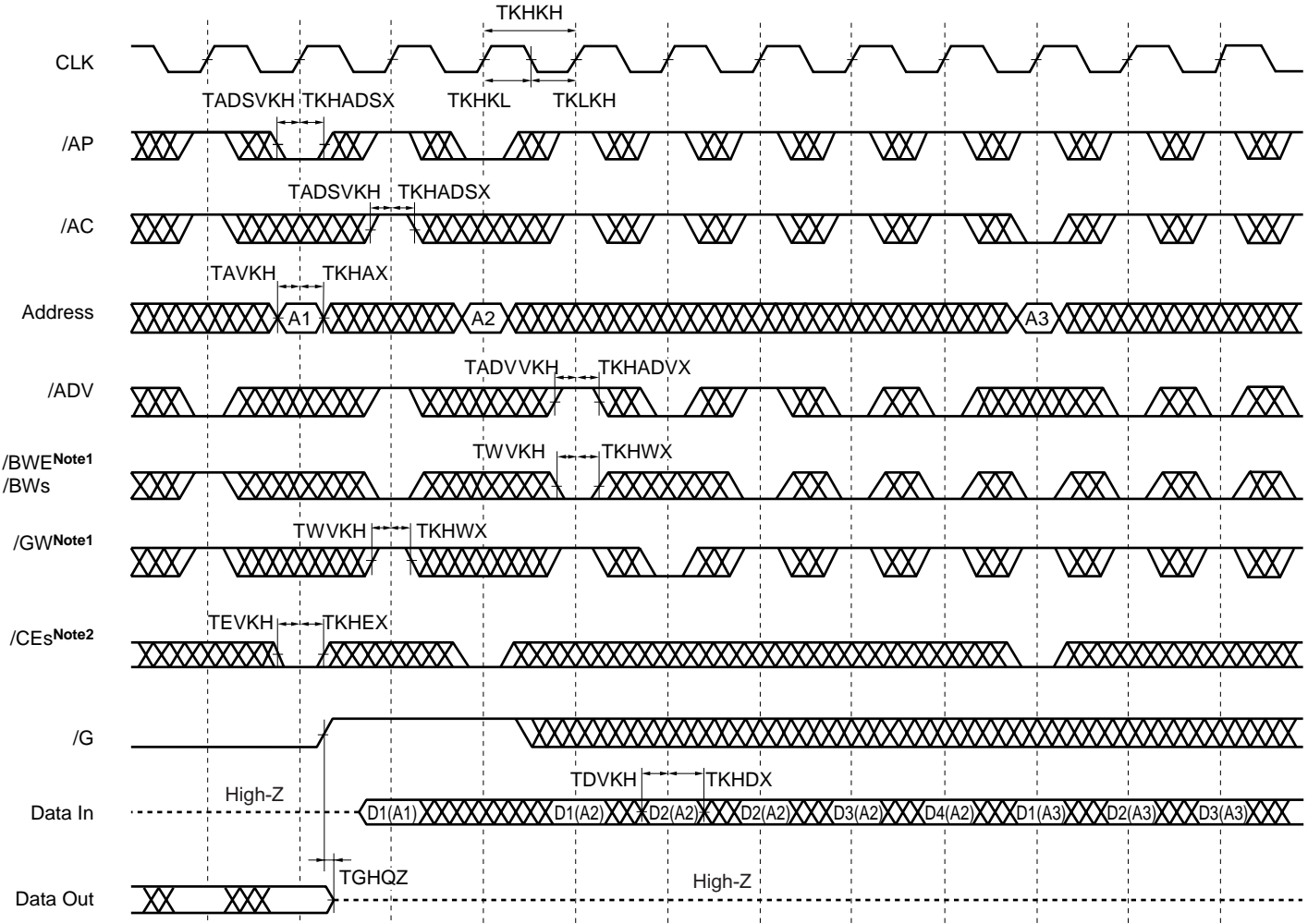
READ CYCLE



**Note** /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

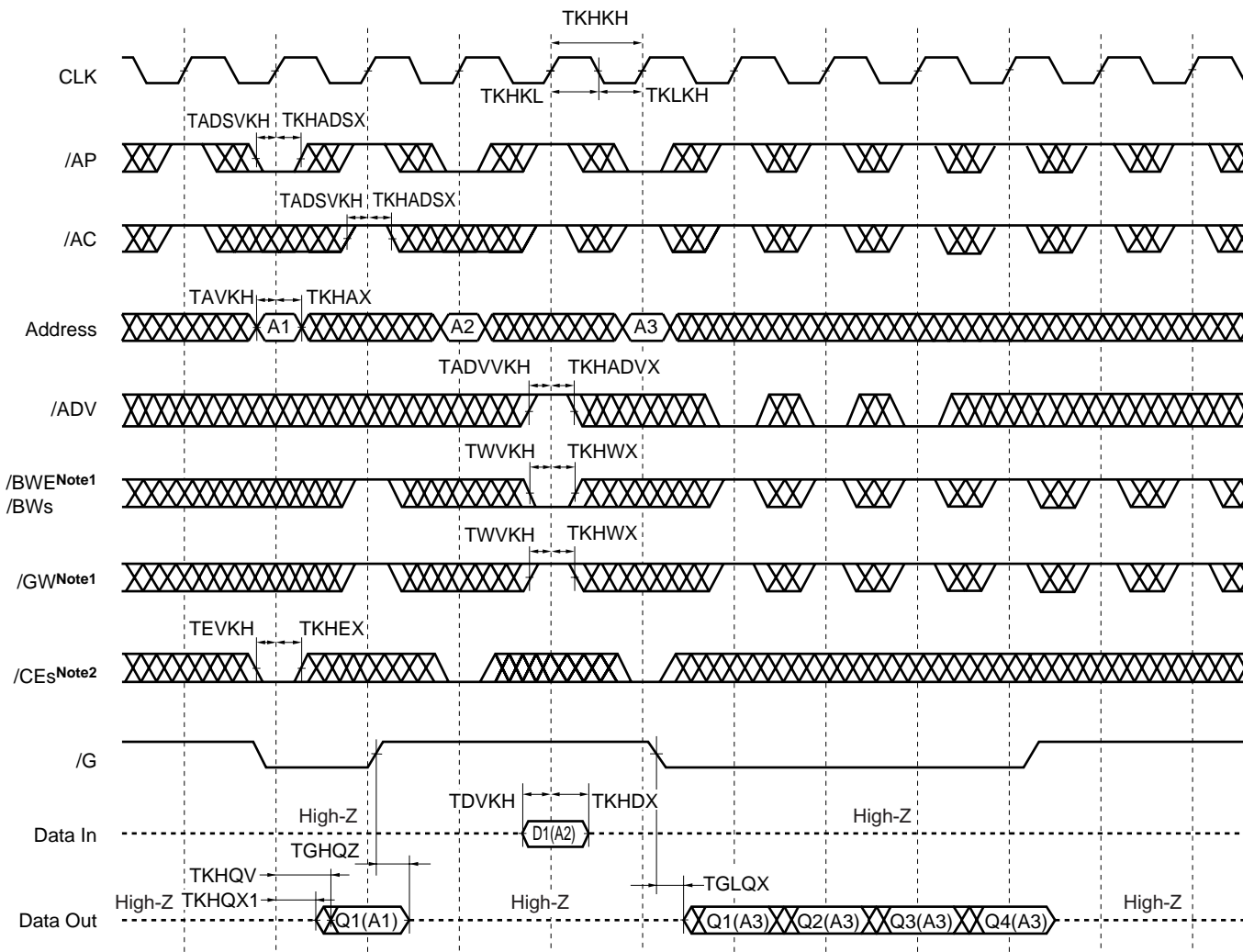
**Remark** Qn(A2) refers to output from address A2. Q1 to Q4 refer to outputs according to burst sequence.

WRITE CYCLE



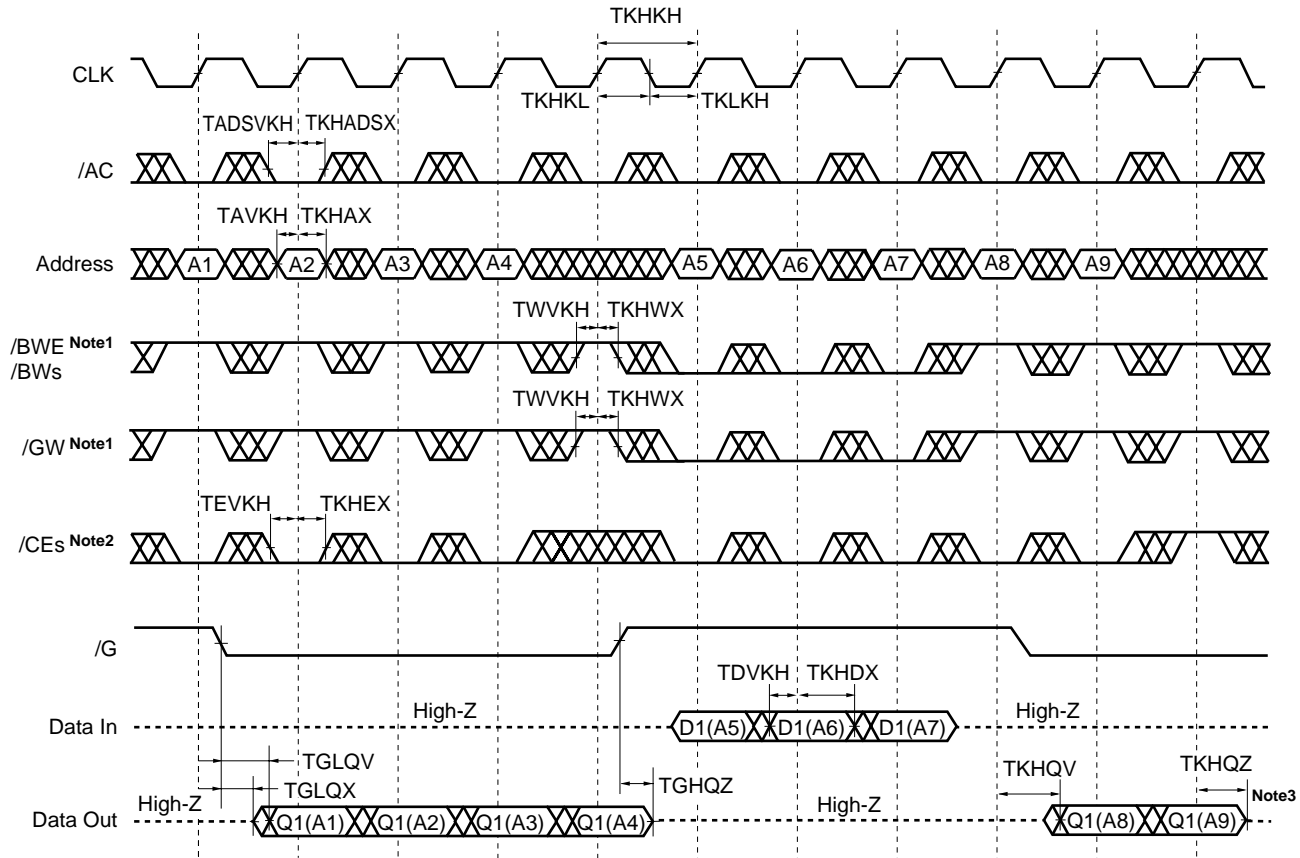
- Notes**
1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1 to /BW4 LOW.
  2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

READ / WRITE CYCLE



- Notes**
1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1 to /BW4 LOW.
  2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.

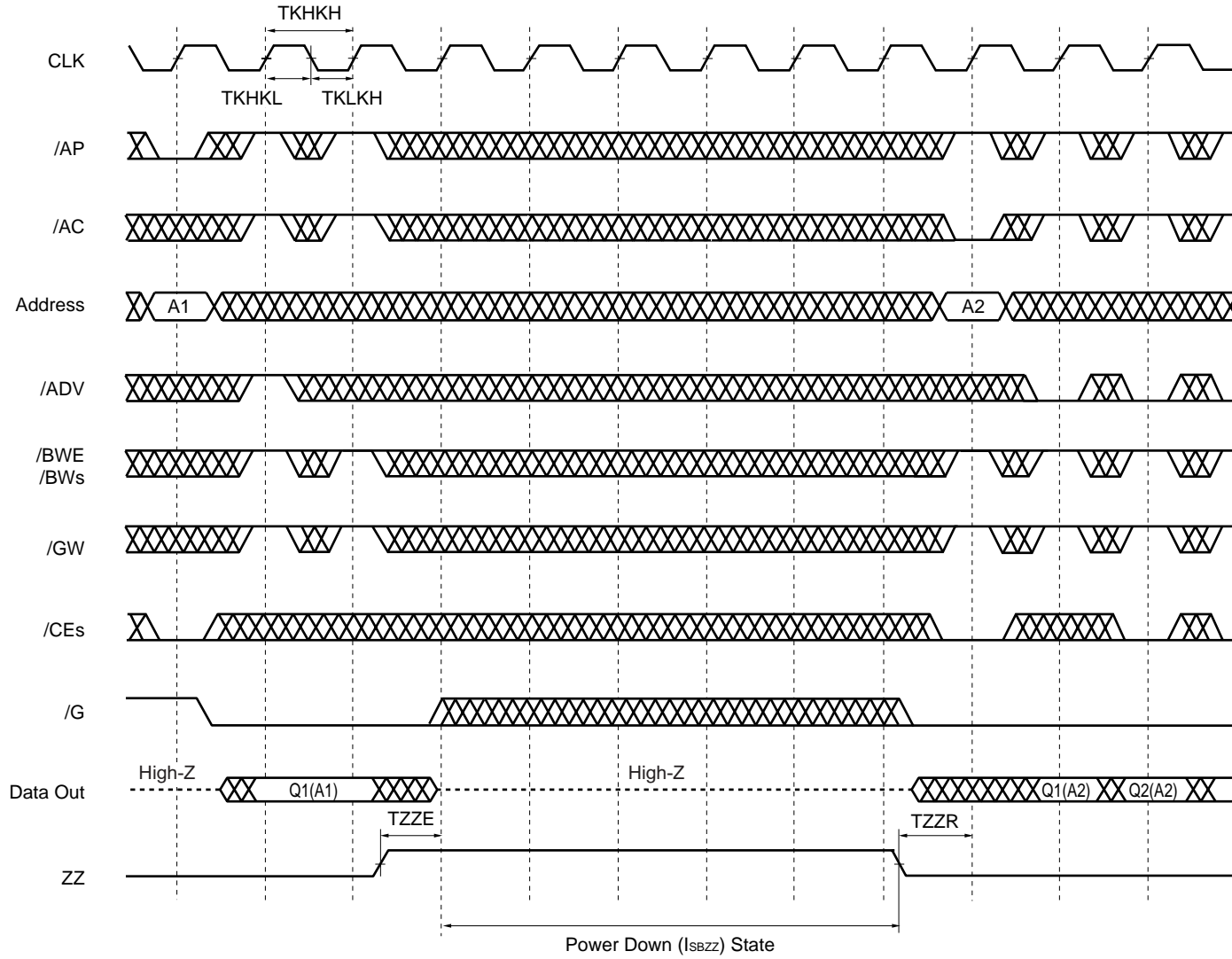
★ SINGLE READ / WRITE CYCLE



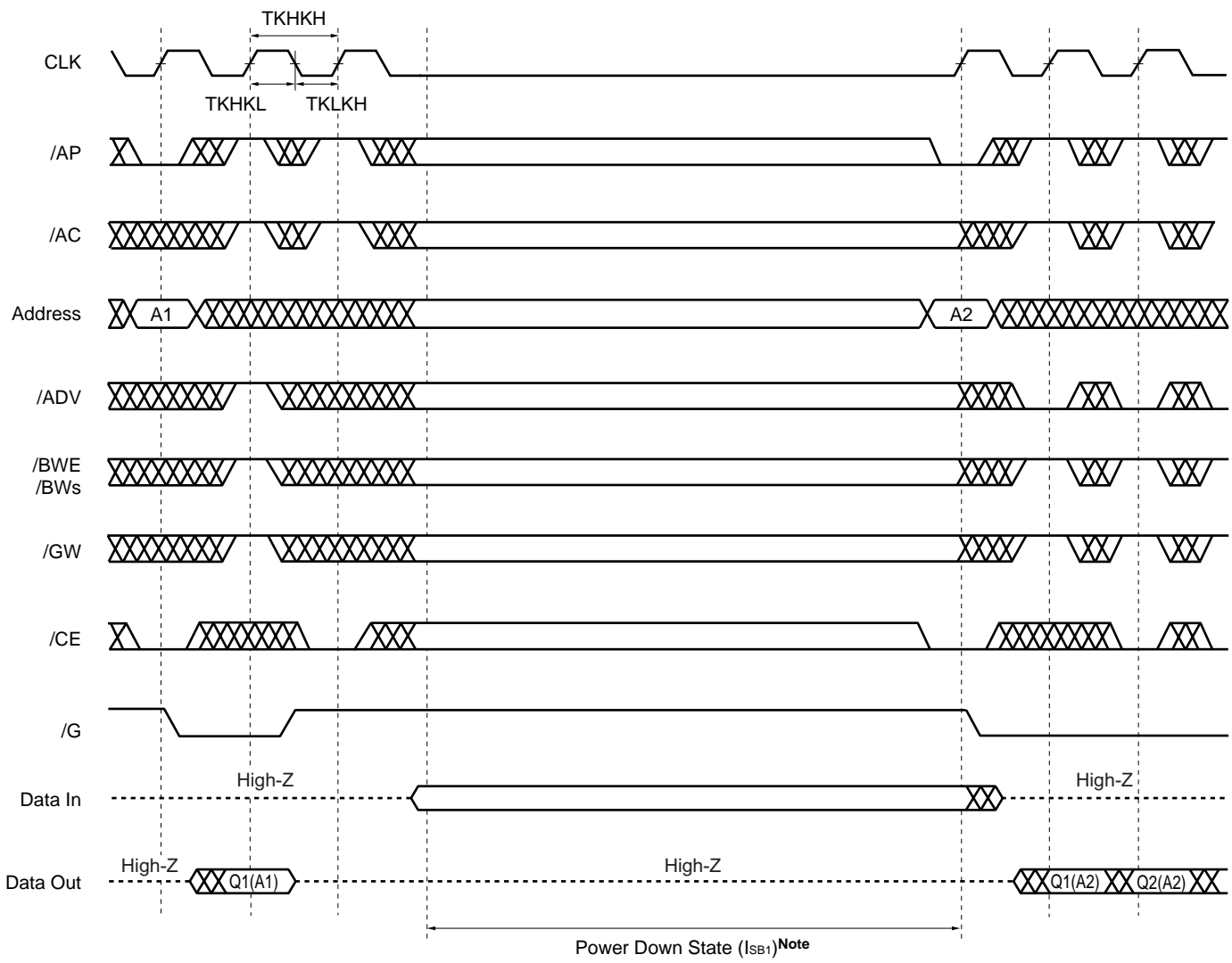
- Notes**
1. All bytes WRITE can be initiated by /GW LOW or /GW HIGH and /BWE, /BW1 to /BW4 LOW.
  2. /CEs refers to /CE, CE2 and /CE2. When /CEs is LOW, /CE and /CE2 are LOW and CE2 is HIGH. When /CEs is HIGH, /CE and /CE2 are HIGH and CE2 is LOW.
  3. Outputs are disabled within one clock cycle after deselect.

**Remark** /AP is HIGH and /ADV is don't care.

POWER DOWN (ZZ) CYCLE



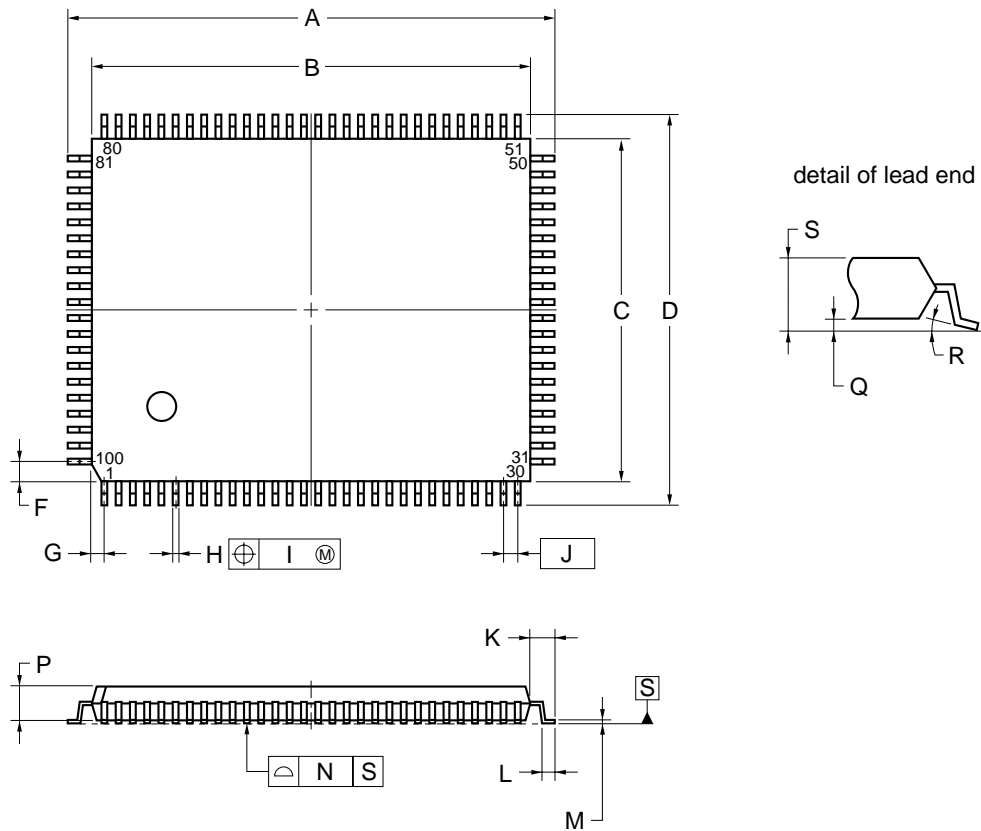
**STOP CLOCK CYCLE**



**Note**  $V_{IN} \leq 0.2V$  or  $V_{IN} \geq V_{DD} - 0.2V$ ,  $V_{IO} \leq 0.2V$

Package Drawing

100-PIN PLASTIC LQFP (14x20)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	14.0±0.2
D	16.0±0.2
F	0.825
G	0.575
H	0.32 <sup>+0.08</sup> <sub>-0.07</sub>
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	0.17 <sup>+0.06</sup> <sub>-0.05</sub>
N	0.10
P	1.4
Q	0.125±0.075
R	3° <sup>+7°</sup> <sub>-3°</sub>
S	1.7 MAX.

S100GF-65-8ET-1

**Recommended Soldering Condition**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD4482161, 4482181, 4482321 and 4482361.

**Types of Surface Mount Devices**

$\mu$ PD4482161GF : 100-pin PLASTIC LQFP (14 x 20)

$\mu$ PD4482181GF : 100-pin PLASTIC LQFP (14 x 20)

$\mu$ PD4482321GF : 100-pin PLASTIC LQFP (14 x 20)

$\mu$ PD4482361GF : 100-pin PLASTIC LQFP (14 x 20)



**Revision History**

Edition/ Date	Page		Type of revision	Location	Description  (Previous edition → This edition)
	This edition	Previous edition			
3rd edition/ Dec. 2002	Throughout	Throughout	Modification Addition	– –	Preliminary Data Sheet → Data Sheet Extended operating temperature products (T <sub>A</sub> = –40 to +85 °C)
	p.20	–	Addition	Timing Chart	SINGLE READ / WRITE CYCLE

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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