AS1716

Capacitive Sensor Interface

Datasheet

1 General Description

AS1716 is an analog front end specifically designed for unbiased Capacitive Sensors, as for instance Knock Sensors in Automotive, to be interfaced with Analog Digital Converters with Sample and Hold input stages.

The device provides differential inputs, a 1st order low pass filter to cutoff the high frequency noise components, differential to single ended conversion, programmable gain stage and a 2 pole low pass Multiple Feedback Filter.

The Knock Sensor is a Piezo Electric device that generates a voltage if it is stressed. It senses knock and transmits information to the electronic engine management control unit. This influences process control in the engine, for example timing and fuel injection until knock is eliminated.

The capacitive sensor is biased via resistors to a voltage level of $V_{DDA}/2$.

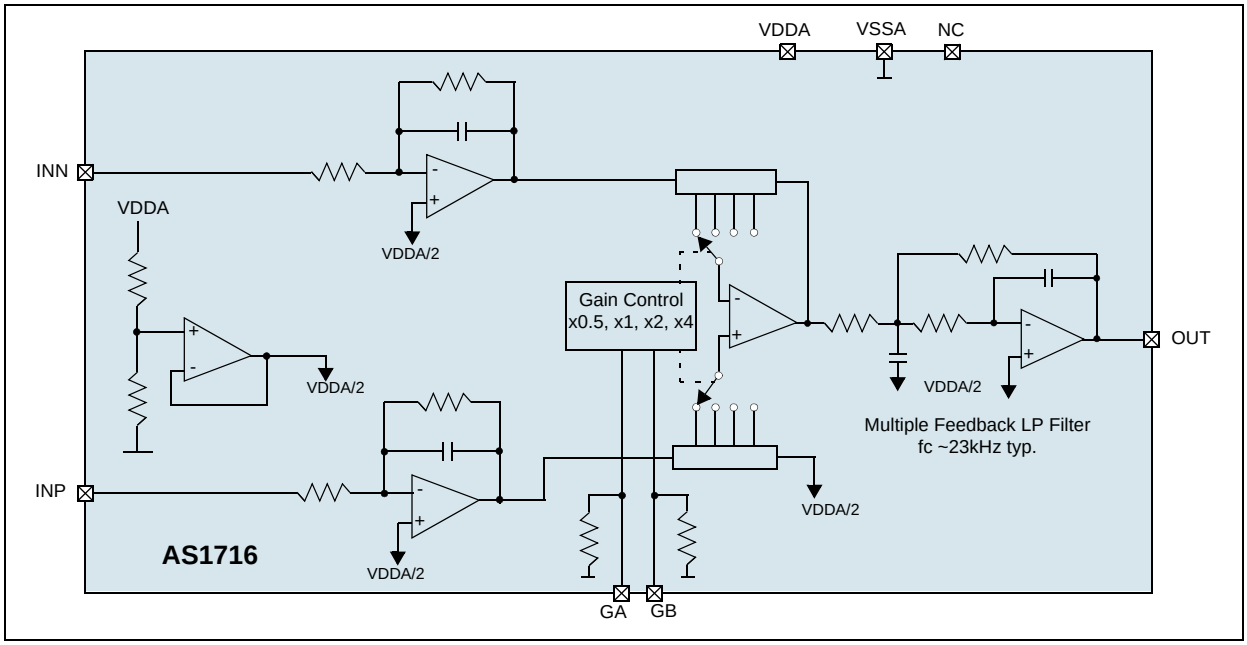
2 Key Features

- Differential input stage with wide input range
- Resistive sensor biasing ($V_{DDA}/2$)
- Programmable Gain (x0.5, x1, x2, x4)
- Internal 2nd order low pass Multiple Feedback Filter with a min. cut off frequency of 16kHz
- Single supply operation: 4.5V to 5.5V
- Operating Temperature range: -40°C to +125°C
- High CMRR: 55dB (min)
- EMC characterized by IEC 61967-4 (1Ω / 150Ω Method)
- EMC characterized by IEC 62132-4 (Direct Power Injection)
- Automotive qualified to AECQ100 for IC and PPAP level 3
- 8-pin SOIC Package

3 Applications

Analog front end for Capacitive Sensors to Analog to Digital Converters and DSP.

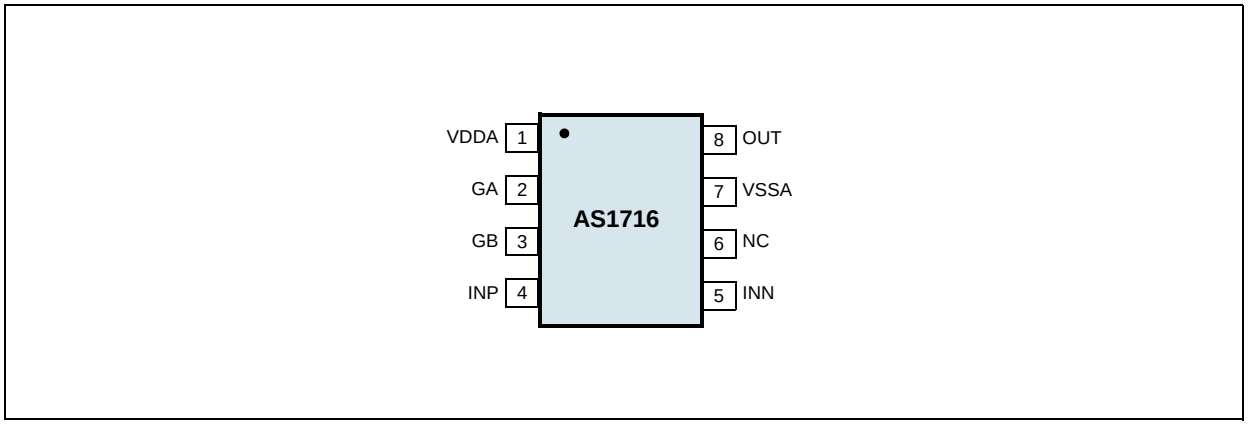
Figure 1. AS1716 Block Diagram



4 Pinout

Pin Assignment

Figure 2. Pin Assignments (Top View)



Pin Description

Table 1. Pin Description

Pin Name	Pin Number	Description
VDDA	1	**Positive Supply.**
GA	2	**Gain selection.** Internal pull-down of 100kΩ
GB	3	**Gain selection.** Internal pull-down of 100kΩ
INP	4	**Non-Inverting Input.**
INN	5	**Inverting Input.**
NC	6	**Not Connected.** Must be left unconnected in the application
VSSA	7	**Negative Supply.**
OUT	8	**Signal Output.**

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDDA, VSSA		+ 7.0	V	
GA, GB, OUT, INP, INN, NC	VSSA - 0.3	VDDA + 0.3	V	To get an overvoltage protection of up to +16V at the system level, apply external resistors (typ. 1kΩ) on the pins INP and INN.
ESD		±4	kV	*AEC-Q100-002,* @ T_A = +25ºC
Latchup Immunity	-100	+100	mA	*AEC-Q100-004,* @ T_A = +25ºC
Operating Temperature Range	-40	+125	ºC	
Junction Temperature		+150	ºC	
Storage Temperature Range	-65	+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

T_A = -40ºC to +125ºC, Parameters are measured at V_{DDA} = 4.5V to 5.5V, R_{LOAD} = 100Ω serial to C_{LOAD} = 10nF, T_A = +25ºC and are refering to VSSA, unless otherwise specified. Typical values are listed for reference only and will not be tested.

Table 3. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DC Electrical Characteristics						
V_{DDA}	Supply Voltage Range	@ pin VDDA	4.5	5	5.5	V
I_{DDA}	Supply Current	@ pin VDDA	3	4.5	9	mA
PSRR[1]	Power Supply Rejection Ratio				6	dB
V_{CM}	Common Mode input Range	@ pins INN, INP	V_{SSA}		V_{DDA}	V
CMRR	Common Mode Rejection Ratio		55			dB
R_{IN}	Differential Input Resistance	between pins INN and INP	70	100	130	kΩ
V_{REF}	Internal Common Mode Input Voltage	INP shorted to INN	V_{DDA}/2 -2%	V_{DDA}/2	V_{DDA}/2 +2%	V
V_{OFF}	Offset Voltage	Gain1, V_{INP} = V_{INN} @ V_{CM} = V_{DDA}/2, @ pin OUT	V_{REF} -10		V_{REF} +10	mV
V_{IL}	Logic Low (GA, GB)	@ pin GA and GB			1.2	V
V_{IH}	Logic High (GA, GB)	@ pin GA and GB	2.0			V
I_{LEAK}	Leakage Current (GA, GB)	V_{DDA} = 5V, Gain4		1		µA
V_{HYST}[1]	Hysteresis	@ pin GA and GB	100	200		mV
R_{PD}	Pull-Down Resistor	@ pin GA and GB	50	100	150	kΩ
Gain0.5	Overall gain 0.5	GA = GB = 1	0.5-10%	0.5	0.5+10%	
Gain1	Overall gain 1	GA = 1, GB = 0	1-10%	1	1+10%	
Gain2	Overall gain 2	GA = 0, GB = 1	2-5%	2	2+5%	
Gain4	Overall gain 4	GA = GB = 0, default setting	4-5%	4	4+5%	
R_L	External Serial Resistor	R_L serial to C_L (see Figure 13 on page 9)	100		1k	Ω
C_L	External Capacitive Load		0.01		10	nF
I_{SHORT+}	Positive Short Circuit Current	V_{OUT} is driven to V_{DDA} and V_{OUT} is connected to V_{SSA}		25		mA
I_{SHORT-}	Negative Short Circuit Current	V_{OUT} is driven to V_{SSA} and V_{OUT} is connected to V_{DDA}		25		mA
V_{OUT-L}	Output Range Low	@ pin VOUT		V_{SSA}+ 0.05		V
V_{OUT-H}	Output Range High	@ pin VOUT		V_{DDA}- 0.05		V

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
AC Electrical Characteristics						
f_C	Filter Cut-off Frequency	V_{DDA} = 4.5V, GA = GB = 0, INP-INN = $1V_{PP}$, f_{IN} = 16kHz and 29kHz	16	23	29	kHz
THD	Total Harmonic Distortion	V_{DDA} = 5V, f_{IN} = 1kHz, INP-INN = $8V_{PP}$, Gain0.5		80		dB
V_{NOISE}	RMS noise at OUT	Gain4, f_C = 50Hz - 23kHz			1	mV_{RMS}

1. Guaranteed by design

7 Typical Operating Characteristics

V_{DDA} = 5.0V, T_A = +25ºC (unless otherwise specified).

Figure 3. CMRR vs. Temperature; GA = GB = 0

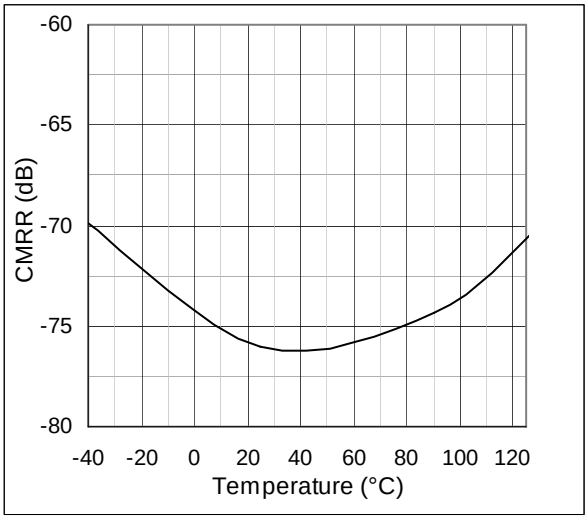


Figure 4. Supply Current vs. Temperature;

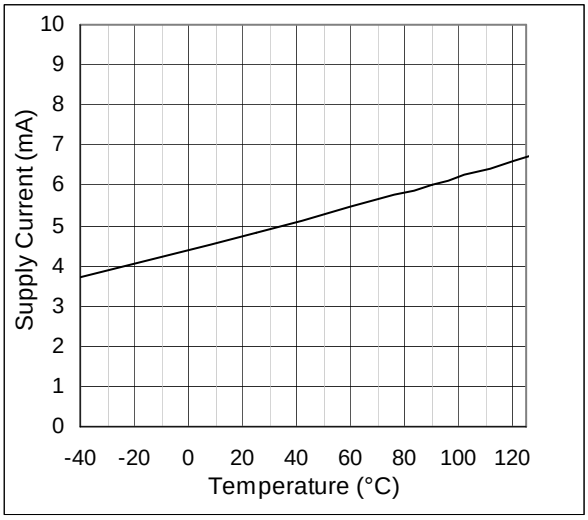


Figure 5. THD vs. Temperature

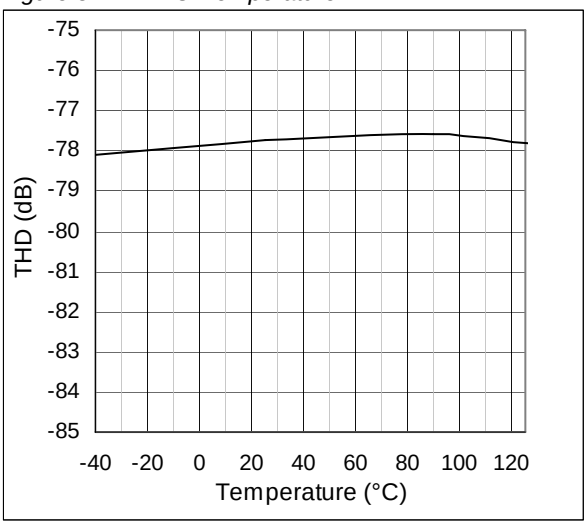


Figure 6. THD vs. Frequency

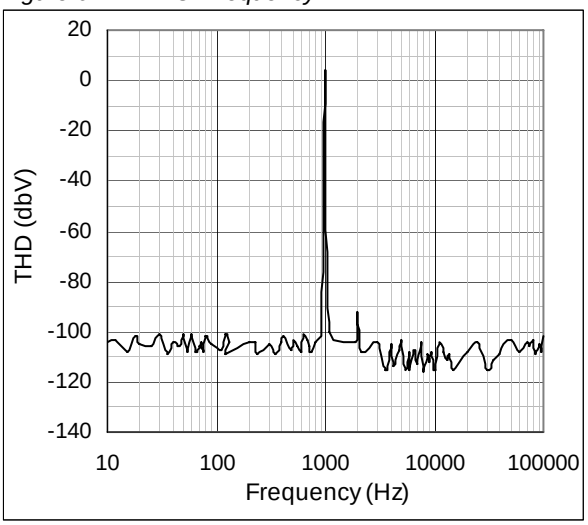


Figure 7. Transfer Characteristics

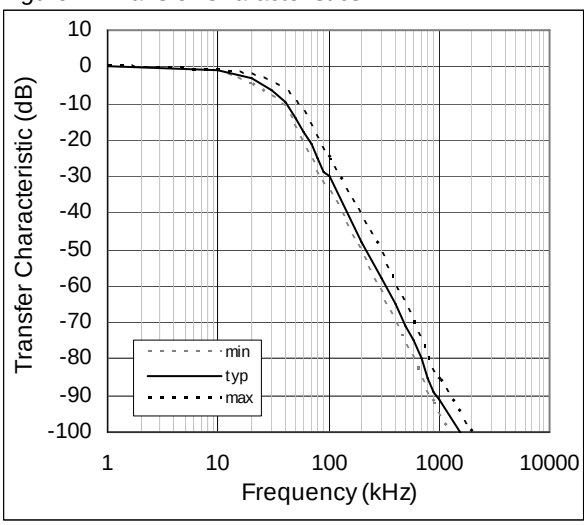
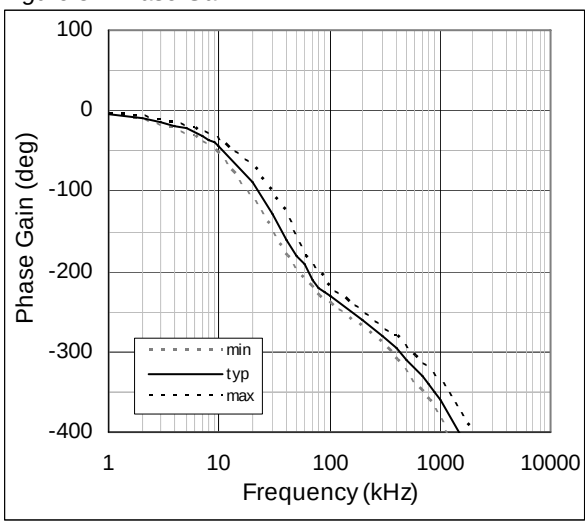


Figure 8. Phase Gain



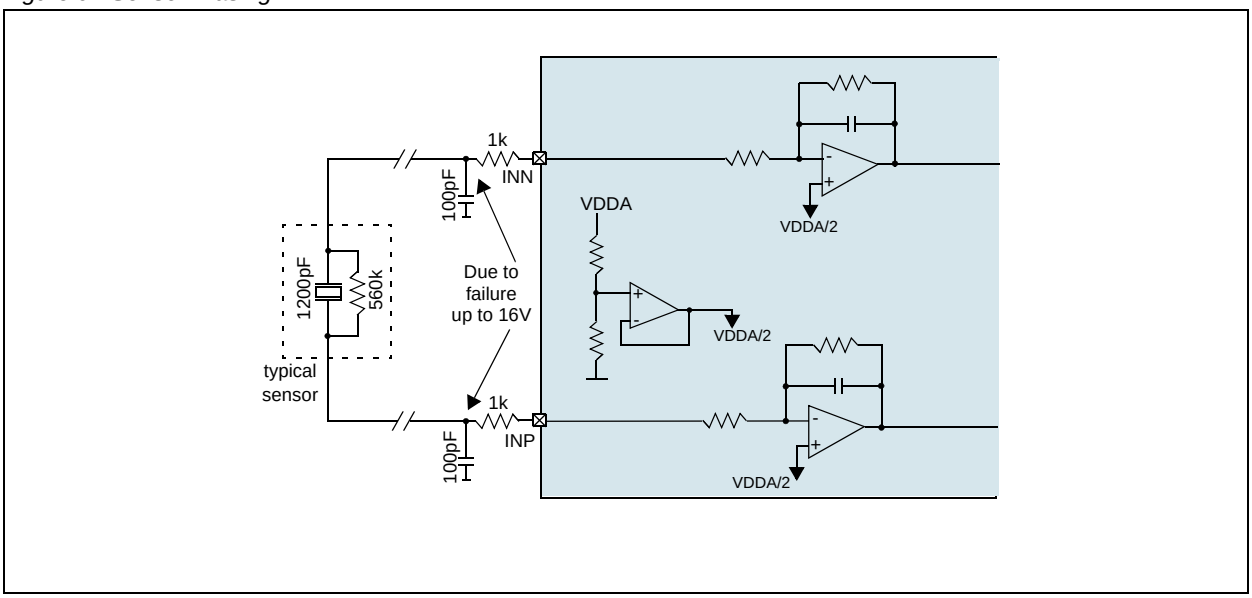
8 Detailed Description

Sensor Biasing and Input Protection Resistors

Due to the capacitive and differential nature of the knock sensor, the common mode voltage for the sensor must be set. This is ensured by the first amplifier, whose virtual ground is biasing the sensor via a of 50kΩ resistor.

Due to a failure, voltages up to 16V can occur on the input pins. In this case two external serial resistors of 1kΩ must be applied at the inputs. These resistors are limiting the current, when the on chip protection diode opens.

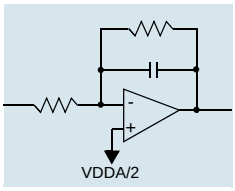
Figure 9. Sensor Biasing



Inverting Input Structure

The Input Strucutre is a first order low-pass filter and fulfills two main functions. First, it is used for biasing the sensor and second, the first order low-pass filter characteristic is used for noise suppression.

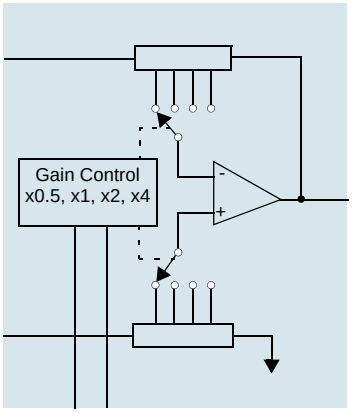
Figure 10. Input Buffer



Fully Differential to Single Ended Conversion

The Subtractor block converts the filtered differential sensor signal into a single ended signal. Further this block provides also the gain setting (see Section Gain Settings).

Figure 11. Subtractor Block



Gain Settings

By means of pins GA and GB, 4 gain settings (x0.5, x1, x2, x4) can be realized.

The default gain setting is 4, GA=0 and GB=0.

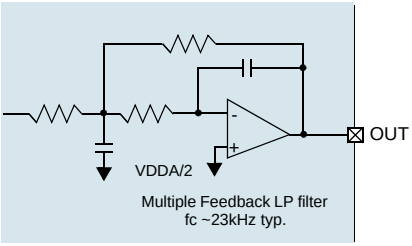
Table 4. Gain Settings

Gain	GA	GB
0.5	1	1
1	1	0
2	0	1
4	0	0

Multiple Feedback Filter

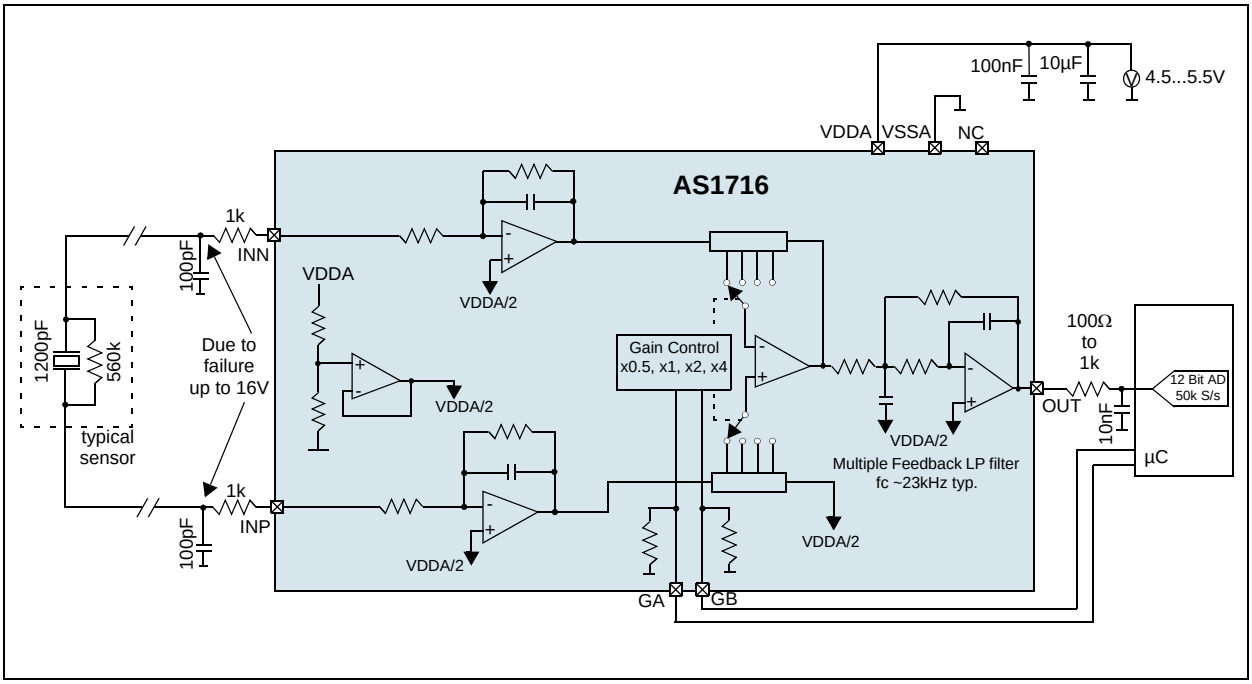
The Multiple Feedback Filter provides a second order low pass characteristics with a minimum cut-off frequency of 16kHz and a typical fc of 23kHz. The Multiple Feedback configuration is used to avoid aliasing, to filter out high frequency components. The Output is able to drive a resistor from 100Ω to 1kΩ serial to a 10nF capacitor.

Figure 12. Multiple Feedback Filter



9 Application Information

Figure 13. Application Diagram, minimal requirements



Values of the suggested external components are indicative and need to be characterized for each specific application.

Typical Piezo Sensor:

- Resistor from 500kΩ to 1MΩ
- Capacity from 900nF to 1.5µF

Typical wire equivalent circuit:

- Capacity to groung from 100pF to 400pF / meter
- Capacity between wires strongly depends on type of wires (twisted-pair strongly suggested)
- Resistance is typical 50mΩ / meter @ 20°C

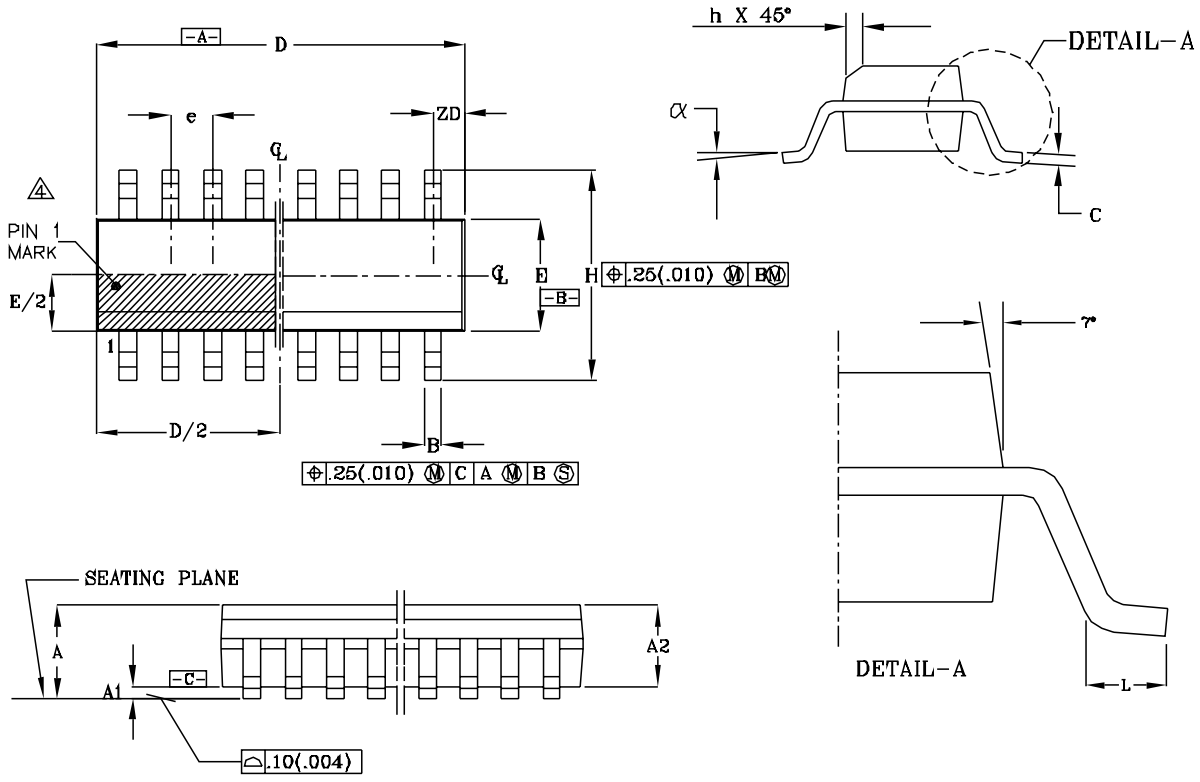
Layout rules

- Input Resistors and Capacitors at the inputs should be placed as close as possible to the stonger possible source of disturbances (i.e. the input connector).
- The input lines should be kept as short as possible and routed close to each other.
- The filter capacitor (100nF) on supply should be a ceramic type and placed as close as possible to the chip.
- VSSA and VDDA lines on PCB should have larger width than other signals to minimize resistance, especially if the 10µF capacitor is not very close to the chip.
- The output line should be kept as short as possible.

10 Package Drawings and Markings

The device is available in a 8-pin SOIC package.

Figure 14. 8-pin SOIC Package Dimensions



Notes:

1. Lead coplanarity should be 0 to 0.10mm (.004”) max.
2. Package surface finishing:
   - Top, matte (charmilles #18-30)
   - All sides, matte (charmilles +18-30)
   - Bottom, smooth or matte (charmilles +18-30)
3. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.25mm (.010”) per side.
4. Details of pin #1 mark are optional but must be located within the area indicated.

Symbol	Min	Max
A	1.52	1.72
A1	0.10	0.25
A2	1.37	1.57
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
α	0°	8°
ZD	0.53REF	

11 Ordering Information

The device is available as the standard product shown in Table 5.

Table 5. Ordering Information

Ordering Code	Marking	Description	Delivery Form	Package
AS1716A-ASOT	AS1716A	Capacitive Sensor Interface, 16kHz	Tape and Reel	8-pin SOIC

All devices are RoHS compliant and free of halogene substances.

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