FLEx36™ 3.3V 32K/64K/128K/256K/512 x 36 Synchronous Dual-Port RAM

Features

- **True dual-ported memory cells that allow simultaneous access of the same memory location**
- **Synchronous pipelined operation**
- **Family of 1-Mbit, 2-Mbit, 4-Mbit, 9-Mbit and 18-Mbit devices**
- **Pipelined output mode allows fast operation**
- **0.18-micron CMOS for optimum speed and power**
- **High-speed clock to data access**
- **3.3V low power**
  - **— Active as low as 225 mA (typ.)**
  - **— Standby as low as 55 mA (typ.)**
- **Mailbox function for message passing**
- **Global master reset**
- **Separate byte enables on both ports**
- **Commercial and industrial temperature ranges**
- **IEEE 1149.1-compatible JTAG boundary scan**
- **256-ball FBGA (1-mm pitch)**
- **Counter wrap around control**
  - **— Internal mask register controls counter wrap-around**
  - **— Counter-interrupt flags to indicate wrap-around**
  - **— Memory block retransmit operation**
- **Counter readback on address lines**
- **Mask register readback on address lines**
- **Dual Chip Enables on both ports for easy depth expansion**
- **Seamless migration to next-generation dual-port family**

Functional Description

The FLEx36 family includes 1-Mbit, 2-Mbit, 4-Mbit, 9-Mbit and 18-Mbit pipelined, synchronous, true dual-port static RAMs that are high-speed, low-power 3.3V CMOS. Two ports are provided, permitting independent, simultaneous access to any location in memory. A particular port can write to a certain location while another port is reading that location. The result of writing to the same location by more than one port at the same time is undefined. Registers on control, address, and data lines allow for minimal set-up and hold time.

During a Read operation, data is registered for decreased cycle time. Each port contains a burst counter on the input address register. After externally loading the counter with the initial address, the counter will increment the address internally (more details to follow). The internal Write pulse width is independent of the duration of the R/W input signal. The internal Write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE0}$ or LOW on CE1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. One cycle with chip enables asserted is required to reactivate the outputs.

Additional features include: readback of burst-counter internal address value on address lines, counter-mask registers to control the counter wrap-around, counter interrupt (CNTINT) flags, readback of mask register value on address lines, retransmit functionality, interrupt flags for message passing, JTAG for boundary scan, and asynchronous Master Reset (MRST).

The CYD18S36V devices in this family has limited features. Please see Address Counter and Mask Register Operations[19] on page 5 for details.

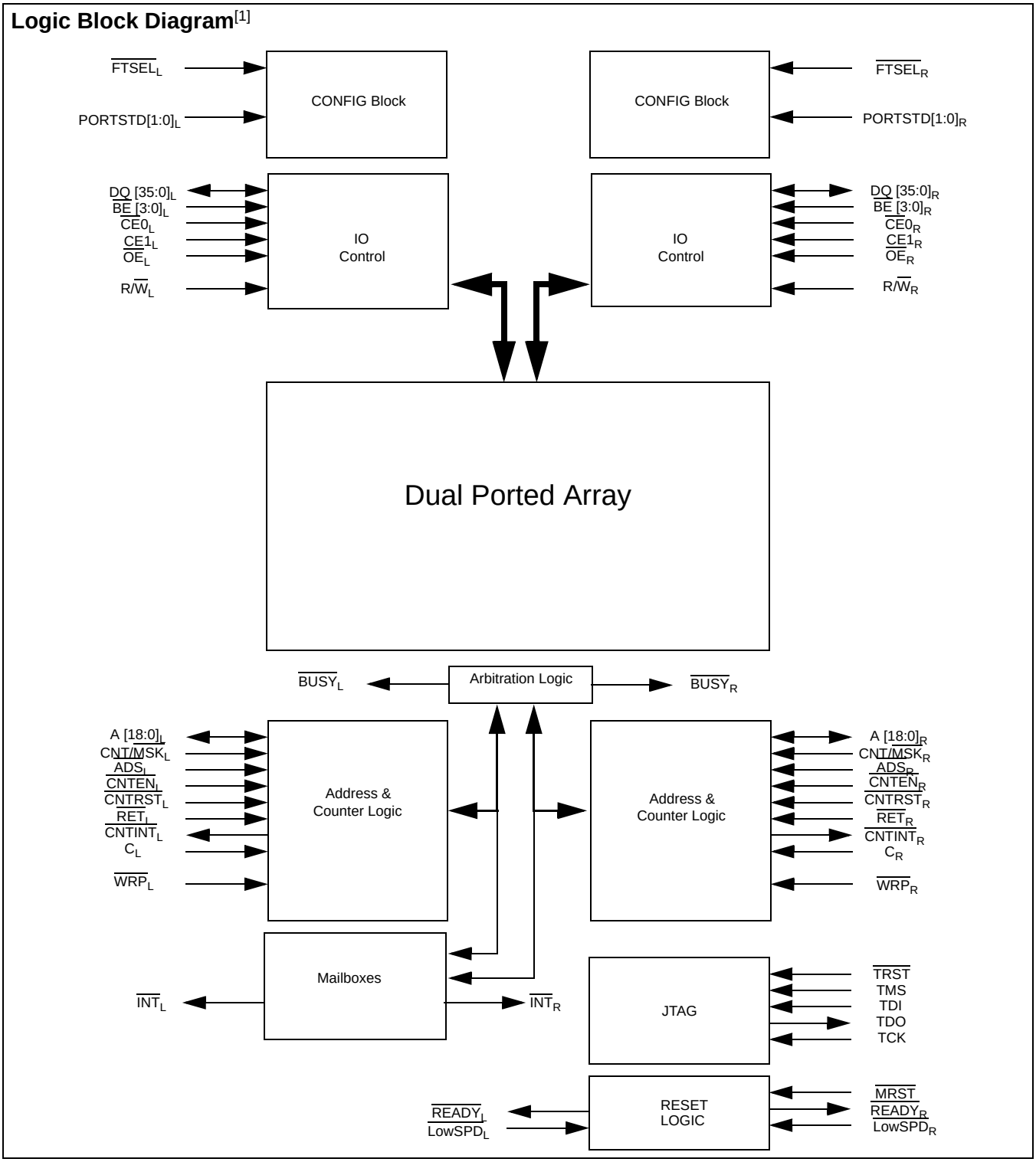
Seamless Migration to Next-Generation Dual-Port Family

Cypress offers a migration path for all devices in this family to the next-generation devices in the Dual-Port family with a compatible footprint. Please contact Cypress Sales for more details.

Table 1. Product Selection Guide

Density	1 Mbit (32K x 36)	2 Mbit (64K x 36)	4 Mbit (128K x 36)	9 Mbit (256K x 36)	18 Mbit (512K x 36)
Part Number	CYD01S36V	CYD02S36V	CYD04S36V	CYD09S36V	CYD18S36V
Max. Speed (MHz)	167	167	167	167	133
Max. Access Time – Clock to Data (ns)	4.0	4.0	4.0	4.0	5.0
Typical Operating Current (mA)	225	225	225	270	315
Package	256 FBGA (17 mm x 17 mm)	256 FBGA (17 mm x 17 mm)	256 FBGA (17 mm x 17 mm)	256 FBGA (17 mm x 17 mm)	256 FBGA (23 mm x 23 mm)

Logic Block Diagram[1]



Note:
1. 18-Mbit device has 19 address bits, 9-Mbit device has 18 address bits, 4-Mbit device has 17 address bits, 2-Mbit device has 16 address bits, and 1-Mbit device has 15 address bits.

Pin Configurations

256-ball FBGA
(Top View)
CYD01S36V/CYD02S36V/CYD04S36V/CYD09S36V/CYD18S36V

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	DQ32L	DQ30L	DQ28L	DQ26L	DQ24L	DQ22L	DQ20L	DQ18L	DQ18R	DQ20R	DQ22R	DQ24R	DQ26R	DQ28R	DQ30R	DQ32R
B	DQ33L	DQ31L	DQ29L	DQ27L	DQ25L	DQ23L	DQ21L	DQ19L	DQ19R	DQ21R	DQ23R	DQ25R	DQ27R	DQ29R	DQ31R	DQ33R
C	DQ34L	DQ35L	$\overline{\text{RET}}$L [2,3]	$\overline{\text{INT}}$L	NC [2,5]	NC [2,5]	REVL [2,4]	$\overline{\text{TRST}}$ [2,5]	$\overline{\text{MRST}}$	NC [2,5]	NC [2,5]	NC [2,5]	$\overline{\text{INT}}$R	$\overline{\text{RET}}$R [2,3]	DQ35R	DQ34R
D	A0L	A1L	$\overline{\text{WRP}}$L [2,3]	VREFL [2,4]	$\overline{\text{FTSEL}}$L [2,3]	$\overline{\text{LOWSPD}}$L [2,4]	VSS	VTTL	VTTL	VSS	$\overline{\text{LOWSPD}}$R [2,4]	$\overline{\text{FTSEL}}$R [2,3]	VREFL [2,4]	$\overline{\text{WRP}}$R [2,3]	A1R	A0R
E	A2L	A3L	$\overline{\text{CE0}}$L [11]	CE1L [10]	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	CE1R [10]	$\overline{\text{CE0}}$R [11]	A3R	A2R
F	A4L	A5L	$\overline{\text{CNTINT}}$L [12]	$\overline{\text{BE3}}$L	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE3}}$R	$\overline{\text{CNTINT}}$R [12]	A5R	A4R
G	A6L	A7L	$\overline{\text{BUSY}}$L [2,5]	$\overline{\text{BE2}}$L	REV_L [2,3]	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE2}}$R	$\overline{\text{BUSY}}$R [2,5]	A7R	A6R
H	A8L	A9L	CL	VTTL	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	VTTL	CR	A9R	A8R
J	A10L	A11L	VSS	PORTSTD1L[2,4]	VCORE	VSS	VSS	VSS	VSS	VSS	VSS	VCORE	PORTSTD1R[2,4]	VSS	A11R	A10R
K	A12L	A13L	$\overline{\text{OE}}$L	$\overline{\text{BE1}}$L	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE1}}$R	$\overline{\text{OE}}$R	A13R	A12R
L	A14L	A15L [6]	$\overline{\text{ADS}}$L [11]	$\overline{\text{BE0}}$L	VDDIOL	VSS	VSS	VSS	VSS	VSS	VSS	VDDIOR	$\overline{\text{BE0}}$R	$\overline{\text{ADS}}$R [11]	A15R [6]	A14R
M	A16L [7]	A17L [8]	R/$\overline{\text{W}}$L	REVL [2,4]	VDDIOL	VDDIOL	VDDIOL	VCORE	VCORE	VDDIOR	VDDIOR	VDDIOR	REVR [2,4]	R/$\overline{\text{W}}$R	A17R [8]	A16R [7]
N	A18L [9]	A19L [2,5]	CNT/$\overline{\text{MSK}}$L [10]	VREFL [2,4]	PortSTD0L [2,4]	$\overline{\text{READY}}$L [2,5]	REV_L [2,3]	VTTL	VTTL	REV_R [2,3]	$\overline{\text{READY}}$R [2,5]	PortSTD0R [2,4]	VREFR [2,4]	CNT/$\overline{\text{MSK}}$R [10]	A19R [2,5]	A18R [9]
P	DQ16L	DQ17L	$\overline{\text{CNTEN}}$L [11]	$\overline{\text{CNTRST}}$L [10]	NC [2,5]	NC [2,5]	TCK	TMS	TDO	TDI	NC [2,5]	NC [2,5]	$\overline{\text{CNTRST}}$R [10]	$\overline{\text{CNTEN}}$R [11]	DQ17R	DQ16R
R	DQ15L	DQ13L	DQ11L	DQ9L	DQ7L	DQ5L	DQ3L	DQ1L	DQ1R	DQ3R	DQ5R	DQ7R	DQ9R	DQ11R	DQ13R	DQ15R
T	DQ14L	DQ12L	DQ10L	DQ8L	DQ6L	DQ4L	DQ2L	DQ0L	DQ0R	DQ2R	DQ4R	DQ6R	DQ8R	DQ10R	DQ12R	DQ14R

Notes:
2. This ball will represent a next generation Dual-Port feature. For more information about this feature, contact Cypress Sales.
3. Connect this ball to VDDIO. For more information about this next generation Dual-Port feature contact Cypress Sales.
4. Connect this ball to VSS. For more information about this next generation Dual-Port feature, contact Cypress Sales.
5. Leave this ball unconnected. For more information about this feature, contact Cypress Sales.
6. Leave this ball unconnected for 32K x 36configuration.
7. Leave this ball unconnected for a 64K x 36, 32K x 36 configurations.
8. Leave this ball unconnected for a 128K x 36, 64K x 36 and 32K x 36 configurations.
9. Leave this ball unconnected for a 256K x 36, 128K x 36, 64K x 36, and 32K x 36 configurations.
10. These balls are not applicable for CYD18S36V device. They need to be tied to VDDIO.
11. These balls are not applicable for CYD18S36V device. They need to be tied to VSS.
12. These balls are not applicable for CYD18S36V device. They need to be no connected.

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{18L}	A_{0R}–A_{18R}	**Address Inputs**.
$\overline{BE}_{0L}$–$\overline{BE}_{3L}$	$\overline{BE}_{0R}$–$\overline{BE}_{3R}$	**Byte Enable Inputs**. Asserting these signals enables Read and Write operations to the corresponding bytes of the memory array.
$\overline{BUSY}_L$[2,5]	$\overline{BUSY}_R$[2,5]	**Port Busy Output**. When the collision is detected, a $\overline{BUSY}$ is asserted.
C_L	C_R	**Input Clock Signal**.
$\overline{CE0}_L$[11]	$\overline{CE0}_R$[11]	**Active Low Chip Enable Input**.
$CE1_L$[10]	$CE1_R$[10]	**Active High Chip Enable Input**.
DQ_{0L}–DQ_{35L}	DQ_{0R}–DQ_{35R}	**Data Bus Input/Output**.
$\overline{OE}_L$	$\overline{OE}_R$	**Output Enable Input**. This asynchronous signal must be asserted LOW to enable the DQ data pins during Read operations.
$\overline{INT}_L$	$\overline{INT}_R$	**Mailbox Interrupt Flag Output**. The mailbox permits communications between ports. The upper two memory locations can be used for message passing. $\overline{INT}_L$ is asserted LOW when the right port writes to the mailbox location of the left port, and vice versa. An interrupt to a port is deasserted HIGH when it reads the contents of its mailbox.
$\overline{LowSPD}_L$[2,4]	$\overline{LowSPD}_R$[2,4]	**Port Low Speed Select Input**.
$PORTSTD[1:0]_L$[2,4]	$PORTSTD[1:0]_R$[2,4]	**Port Address/Control/Data I/O Standard Select Inputs**.
$R/\overline{W}_L$	$R/\overline{W}_R$	**Read/Write Enable Input**. Assert this pin LOW to write to, or HIGH to Read from the dual port memory array.
$\overline{READY}_L$[2,5]	$\overline{READY}_R$[2,5]	**Port Ready Output**. This signal will be asserted when a port is ready for normal operation.
$CNT/\overline{MSK}_L$[10]	$CNT/\overline{MSK}_R$[10]	**Port Counter/Mask Select Input**. Counter control input.
$\overline{ADS}_L$[11]	$\overline{ADS}_R$[11]	**Port Counter Address Load Strobe Input**. Counter control input.
$\overline{CNTEN}_L$[11]	$\overline{CNTEN}_R$[11]	**Port Counter Enable Input**. Counter control input.
$\overline{CNTRST}_L$[10]	$\overline{CNTRST}_R$[10]	**Port Counter Reset Input**. Counter control input.
$\overline{CNTINT}_L$[12]	$\overline{CNTINT}_R$[12]	**Port Counter Interrupt Output**. This pin is asserted LOW when the unmasked portion of the counter is incremented to all “1s”.
$\overline{WRP}_L$[2,3]	$\overline{WRP}_R$[2,3]	**Port Counter Wrap Input**. The burst counter wrap control input.
$\overline{RET}_L$[2,3]	$\overline{RET}_R$[2,3]	**Port Counter Retransmit Input**. Counter control input.
$\overline{FTSEL}_L$[2,3]	$\overline{FTSEL}_R$[2,3]	**Flow-Through Select**. Use this pin to select Flow-Through mode. When is de-asserted, the device is in pipelined mode.
$VREF_L$[2,4]	$VREF_R$[2,4]	**Port External High-Speed IO Reference Input**.
V_{DDIOL}	V_{DDIOR}	**Port IO Power Supply**.
REV_L [2, 3, 4]	REV_R[2, 3, 4]	Reserved pins for future features.
$\overline{MRST}$		**Master Reset Input**. $\overline{MRST}$ is an asynchronous input signal and affects both ports. A maser reset operation is required at power-up.
$TRST$[2,5]		**JTAG Reset Input**.
TMS		**JTAG Test Mode Select Input**. It controls the advance of JTAG TAP state machine. State machine transitions occur on the rising edge of TCK.
TDI		**JTAG Test Data Input**. Data on the TDI input will be shifted serially into selected registers.
TCK		**JTAG Test Clock Input**.
TDO		**JTAG Test Data Output**. TDO transitions occur on the falling edge of TCK. TDO is normally three-stated except when captured data is shifted out of the JTAG TAP.
V_{SS}		**Ground Inputs**.

Pin Definitions (continued)

Left Port	Right Port	Description
V_{CORE}[13]		**Core Power Supply**.
V_{TTL}		**LVTTL Power Supply for JTAG IOs**

Master Reset

The FLEx36 family devices undergo a complete reset by taking its MRST input LOW. The MRST input can switch asynchronously to the clocks. An MRST initializes the internal burst counters to zero, and the counter mask registers to all ones (completely unmasked). MRST also forces the Mailbox Interrupt (INT) flags and the Counter Interrupt (CNTINT) flags HIGH. MRST must be performed on the FLEx36 family devices after power-up.

Mailbox Interrupts

The upper two memory locations may be used for message passing and permit communications between ports. *Table 2* shows the interrupt operation for both ports of CYD18S36V. The highest memory location, 7FFFF is the mailbox for the right port and 7FFFE is the mailbox for the left port. *Table 2* shows that in order to set the $\overline{INT}_R$ flag, a Write operation by the left port to address 7FFFF will assert $\overline{INT}_R$ LOW. At least one byte has to be active for a Write to generate an interrupt. A valid Read of the 7FFFF location by the right port will reset $\overline{INT}_R$ HIGH. At least one byte has to be active in order for a Read to reset the interrupt. When one port Writes to the other port's mailbox, the INT of the port that the mailbox belongs to is asserted LOW. The INT is reset when the owner (port) of the mailbox Reads the contents of the mailbox. The interrupt flag is set in a flow-thru mode (i.e., it follows the clock edge of the writing port). Also, the flag is reset in a flow-thru mode (i.e., it follows the clock edge of the reading port).

Each port can read the other port's mailbox without resetting the interrupt. And each port can write to its own mailbox without setting the interrupt. If an application does not require message passing, INT pins should be left open.

Address Counter and Mask Register Operations[19]

This section describes the features only apply to 1Mbit, 2 Mbit, 4 Mbit and 9 Mbit devices. It does not apply to 18Mbit device. Each port of these devices has a programmable burst address counter. The burst counter contains three registers: a counter register, a mask register, and a mirror register.

The **counter register** contains the address used to access the RAM array. It is changed only by the Counter Load, Increment, Counter Reset, and by master reset (MRST) operations.

The **mask register** value affects the Increment and Counter Reset operations by preventing the corresponding bits of the counter register from changing. It also affects the counter interrupt output ($\overline{CNTINT}$). The mask register is changed only by the Mask Load and Mask Reset operations, and by the MRST. The mask register defines the counting range of the counter register. It divides the counter register into two regions: zero or more "0s" in the most significant bits define the masked region, one or more "1s" in the least significant bits define the unmasked region. Bit 0 may also be "0," masking the least significant counter bit and causing the counter to increment by two instead of one.l

The mirror register is used to reload the counter register on increment operations (see "retransmit," below). It always contains the value last loaded into the counter register, and is changed only by the Counter Load, and Counter Reset operations, and by the MRST.

Table 3 summarizes the operation of these registers and the required input control signals. The MRST control signal is asynchronous. All the other control signals in *Table 3* (CNT/MSK, CNTRST, ADS, CNTEN) are synchronized to the port's CLK. All these counter and mask operations are independent of the port's chip enable inputs ($\overline{CE0}$ and CE1).

Table 2. Interrupt Operation Example [1, 14, 15, 16, 17, 18]

Function	Left Port				Right Port			
	$R/\overline{W}_L$	$\overline{CE}_L$	A_{0L-18L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	A_{0R-18R}	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	7FFFF	X	X	X	X	L
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	H	L	7FFFF	H
Set Left $\overline{INT}_L$ Flag	X	X	X	L	L	L	7FFFE	X
Reset Left $\overline{INT}_L$ Flag	H	L	7FFFE	H	X	X	X	X

Notes:
13. This family of Dual-Ports does not use V_{CORE}, and these pins are internally NC. The next generation Dual-Port family, the FLEx36-E™, will use V_{CORE} of 1.5V or 1.8V. Please contact local Cypress FAE for more information.
14. $\overline{CE}$ is internal signal. $\overline{CE}$ = LOW if $\overline{CE}_0$ = LOW and CE_1 = HIGH. For a single Read operation, CE only needs to be asserted once at the rising edge of the CLK and can be deasserted after that. Data will be out after the following CLK edge and will be three-stated after the next CLK edge.
15. $\overline{OE}$ is "Don't Care" for mailbox operation.
16. At least one of $\overline{BE0}$, $\overline{BE1}$, $\overline{BE2}$, or $\overline{BE3}$ must be LOW.
17. A17x is a NC for CYD04S36V, therefore the Interrupt Addresses are 1FFFF and 1FFFE. A17x and A16x are NC for CYD02S36V, therefore the Interrupt Addresses are FFFF and FFFE; A17x, A16x and A15x are NC for CYD01S36V, therefore the Interrupt Addresses are 7FFF and 7FFE.
18. "X" = "Don't Care," "H" = HIGH, "L" = LOW.
19. This section describes the CYD09S36V, CYD04S36V, CYD02S36V, and CYD01S36V which have 18, 17, 16 and 15 address bits.

Counter enable ($\overline{\text{CNTEN}}$) inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast, interleaved memory applications. A port's burst counter is loaded when the port's address strobe ($\overline{\text{ADS}}$) and $\overline{\text{CNTEN}}$ signals are LOW. When the port's $\overline{\text{CNTEN}}$ is asserted and the $\overline{\text{ADS}}$ is deasserted, the address counter will increment on each LOW to HIGH transition of that port's clock signal. This will Read/Write one word from/into each successive address location until $\overline{\text{CNTEN}}$ is deasserted. The counter can address the entire memory array, and will loop back to the start. Counter reset ($\overline{\text{CNTRST}}$) is used to reset the unmasked portion of the burst counter to 0s. A counter-mask register is used to control the counter wrap.

Counter Reset Operation

All unmasked bits of the counter and mirror registers are reset to "0." All masked bits remain unchanged. A Mask Reset followed by a Counter Reset will reset the counter and mirror registers to 00000, as will master reset ($\overline{\text{MRST}}$).

Counter Load Operation

The address counter and mirror registers are both loaded with the address value presented at the address lines.

Table 3. Address Counter and Counter-Mask Register Control Operation (Any Port) [18, 20]

CLK	$\overline{\text{MRST}}$	CNT/$\overline{\text{MSK}}$	$\overline{\text{CNTRST}}$	$\overline{\text{ADS}}$	$\overline{\text{CNTEN}}$	Operation	Description
X	L	X	X	X	X	Master Reset	Reset address counter to all 0s and mask register to all 1s.
⎍	H	H	L	X	X	Counter Reset	Reset counter unmasked portion to all 0s.
⎍	H	H	H	L	L	Counter Load	Load counter with external address value presented on address lines.
⎍	H	H	H	L	H	Counter Readback	Read out counter internal value on address lines.
⎍	H	H	H	H	L	Counter Increment	Internally increment address counter value.
⎍	H	H	H	H	H	Counter Hold	Constantly hold the address value for multiple clock cycles.
⎍	H	L	L	X	X	Mask Reset	Reset mask register to all 1s.
⎍	H	L	H	L	L	Mask Load	Load mask register with value presented on the address lines.
⎍	H	L	H	L	H	Mask Readback	Read out mask register value on address lines.
⎍	H	L	H	H	X	Reserved	Operation undefined

Notes:
20. Counter operation and mask register operation is independent of chip enables.

Counter Increment Operation

Once the address counter register is initially loaded with an external address, the counter can internally increment the address value, potentially addressing the entire memory array. Only the unmasked bits of the counter register are incremented. The corresponding bit in the mask register must be a “1” for a counter bit to change. The counter register is incremented by 1 if the least significant bit is unmasked, and by 2 if it is masked. If all unmasked bits are “1,” the next increment will wrap the counter back to the initially loaded value. If an Increment results in all the unmasked bits of the counter being “1s,” a counter interrupt flag ($\overline{\text{CNTINT}}$) is asserted. The next Increment will return the counter register to its initial value, which was stored in the mirror register. The counter address can instead be forced to loop to 00000 by externally connecting CNTINT to $\overline{\text{CNTRST}}$.[21] An increment that results in one or more of the unmasked bits of the counter being “0” will de-assert the counter interrupt flag. The example in *Figure 2* shows the counter mask register loaded with a mask value of 0003Fh unmasking the first 6 bits with bit “0” as the LSB and bit “16” as the MSB. The maximum value the mask register can be loaded with is 3FFFFh. Setting the mask register to this value allows the counter to access the entire memory space. The address counter is then loaded with an initial value of 8h. The base address bits (in this case, the 6th address through the 16th address) are loaded with an address value but do not increment once the counter is configured for increment operation. The counter address will start at address 8h. The counter will increment its internal address value till it reaches the mask register value of 3Fh. The counter wraps around the memory block to location 8h at the next count. CNTINT is issued when the counter reaches its maximum value.

Counter Hold Operation

The value of all three registers can be constantly maintained unchanged for an unlimited number of clock cycles. Such operation is useful in applications where wait states are needed, or when address is available a few cycles ahead of data in a shared bus interface.

Counter Interrupt

The counter interrupt ($\overline{\text{CNTINT}}$) is asserted LOW when an increment operation results in the unmasked portion of the counter register being all “1s.” It is deasserted HIGH when an Increment operation results in any other value. It is also de-asserted by Counter Reset, Counter Load, Mask Reset and Mask Load operations, and by $\overline{\text{MRST}}$.

Counter Readback Operation

The internal value of the counter register can be read out on the address lines. Readback is pipelined; the address will be valid t_{CA2} after the next rising edge of the port’s clock. If address readback occurs while the port is enabled ($\overline{\text{CE0}}$ LOW and CE1 HIGH), the data lines (DQs) will be three-stated. *Figure 1* shows a block diagram of the operation.

Retransmit

Retransmit is a feature that allows the Read of a block of memory more than once without the need to reload the initial address. This eliminates the need for external logic to store and route data. It also reduces the complexity of the system design and saves board space. An internal “mirror register” is used to store the initially loaded address counter value. When the counter unmasked portion reaches its maximum value set by the mask register, it wraps back to the initial value stored in this “mirror register.” If the counter is continuously configured in increment mode, it increments again to its maximum value and wraps back to the value initially stored into the “mirror register.” Thus, the repeated access of the same data is allowed without the need for any external logic.

Mask Reset Operation

The mask register is reset to all “1s,” which unmasks every bit of the counter. Master reset ($\overline{\text{MRST}}$) also resets the mask register to all “1s.”

Mask Load Operation

The mask register is loaded with the address value presented at the address lines. Not all values permit correct increment operations. Permitted values are of the form $2^n – 1$ or $2^n – 2$. From the most significant bit to the least significant bit, permitted values have zero or more “0s,” one or more “1s,” or one “0.” Thus 7FFFF, 003FE, and 00001 are permitted values, but 7F0FF, 003FC, and 00000 are not.

Mask Readback Operation

The internal value of the mask register can be read out on the address lines. Readback is pipelined; the address will be valid t_{CM2} after the next rising edge of the port’s clock. If mask readback occurs while the port is enabled ($\overline{\text{CE0}}$ LOW and CE1 HIGH), the data lines (DQs) will be three-stated. *Figure 1* shows a block diagram of the operation.

Counting by Two

When the least significant bit of the mask register is “0,” the counter increments by two. This may be used to connect the x36 devices as a 72-bit single port SRAM in which the counter of one port counts even addresses and the counter of the other port counts odd addresses. This even-odd address scheme stores one half of the 72-bit data in even memory locations, and the other half in odd memory locations.

Note:
21. $\overline{\text{CNTINT}}$ and $\overline{\text{CNTRST}}$ specs are guaranteed by design to operate properly at speed grade operating frequency when tied together.

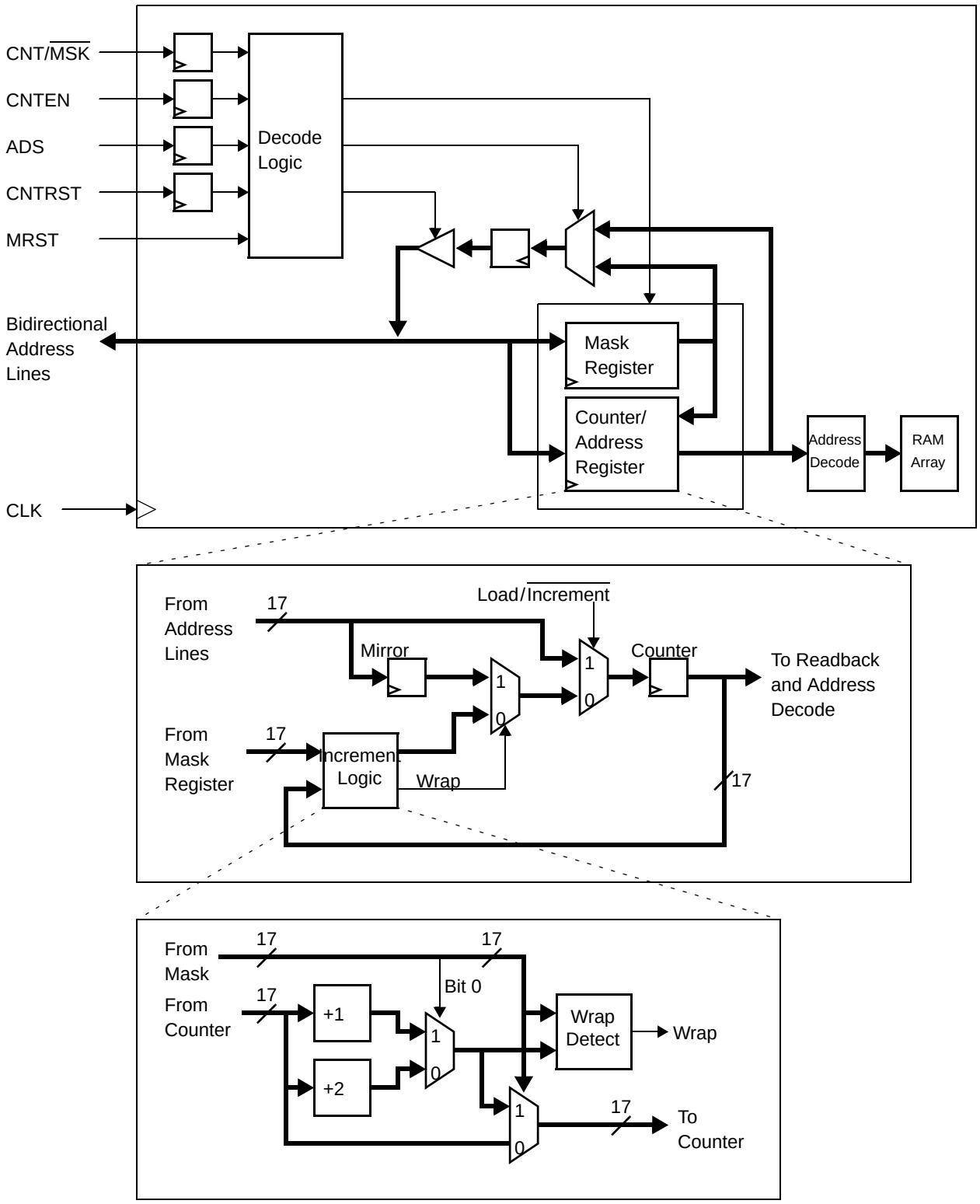


Figure 1. Counter, Mask, and Mirror Logic Block Diagram[1]

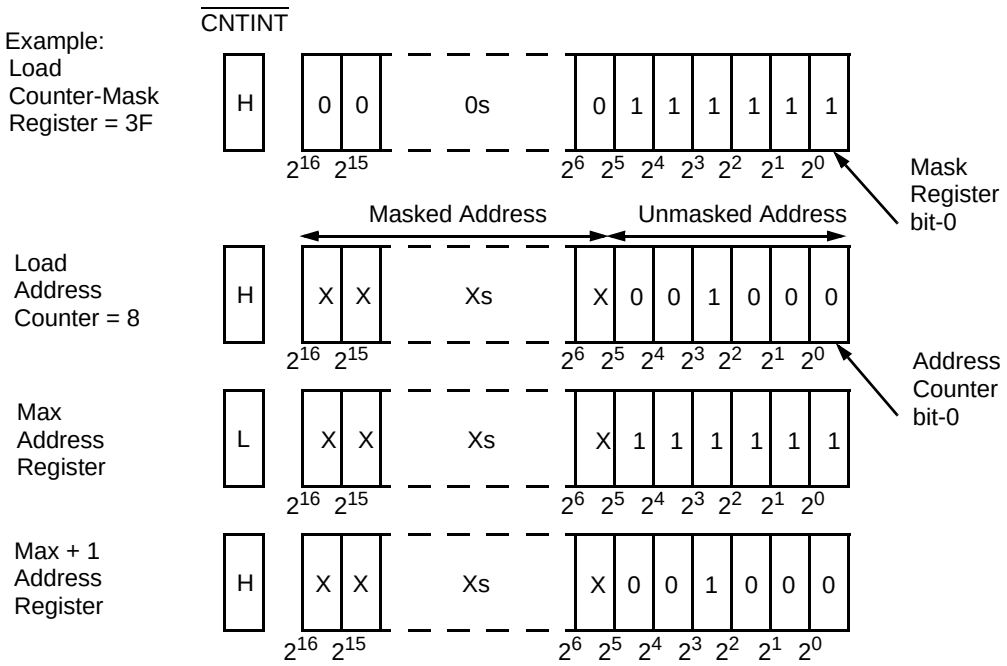


Figure 2. Programmable Counter-Mask Register Operation[1, 22]

IEEE 1149.1 Serial Boundary Scan (JTAG)[23]

The FLEx36 family devices incorporate an IEEE 1149.1 serial boundary scan test access port (TAP). The TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1-compliant TAPs. The TAP operates using JEDEC-standard 3.3V I/O logic levels. It is composed of three input connections and one output connection required by the test logic defined by the standard.

Performing a TAP Reset

A reset is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This reset does not affect the operation of the devices, and may be performed while the device is operating. An MRST must be performed on the devices after power-up.

Performing a Pause/Restart

When a SHIFT-DR PAUSE-DR SHIFT-DR is performed the scan chain will output the next bit in the chain twice. For example, if the value expected from the chain is 1010101, the device will output a 11010101. This extra bit will cause some testers to report an erroneous failure for the devices in a scan test. Therefore the tester should be configured to never enter the PAUSE-DR state.

Boundary Scan Hierarchy for 9-Mbit and 18-Mbit Devices

Internally, the devices have multiple DIEs. Each DIE contains all the circuitry required to support boundary scan testing. The circuitry includes the TAP, TAP controller, instruction register, and data registers. The circuity and operation of the DIE boundary scan are described in detail below.

The scan chain for 9-Mbit and 18-Mbit devices uses a hierarchical approach as shown in *Figure 3* and *Figure 4*. TMS and TCK are connected in parallel to each DIE to drive all 2- or 4-TAP controllers in unison. In many cases, each DIE will be supplied with the same instruction. In other cases, it might be useful to supply different instructions to each DIE. One example would be testing the device ID of one DIE while bypassing the rest.

Each pin of the devices is typically connected to multiple DIEs. For connectivity testing with the EXTEST instruction, it is desirable to check the internal connections between DIEs as well as the external connections to the package. This can be accomplished by merging the netlist of the devices with the netlist of the user's circuit board. To facilitate boundary scan testing of the devices, Cypress provides the BSDL file for each DIE, the internal netlist of the device, and a description of the device scan chain. The user can use these materials to easily integrate the devices into the board's boundary scan environment. Further information can be found in the Cypress application note *Using JTAG Boundary Scan For System in a Package (SIP) Dual-Port SRAMs*.

Notes:
22. The "X" in this diagram represents the counter upper bits.
23. Boundary scan is IEEE 1149.1-compatible. See "Performing a Pause/Restart" for deviation from strict 1149.1 compliance.

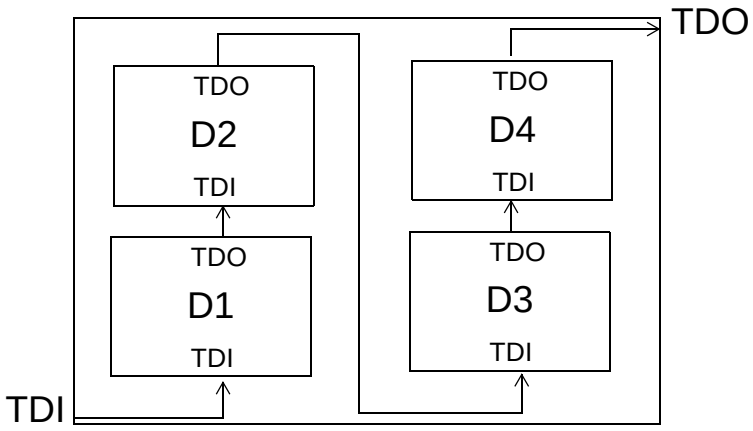


Figure 3. Scan Chain for 18-Mbit Device

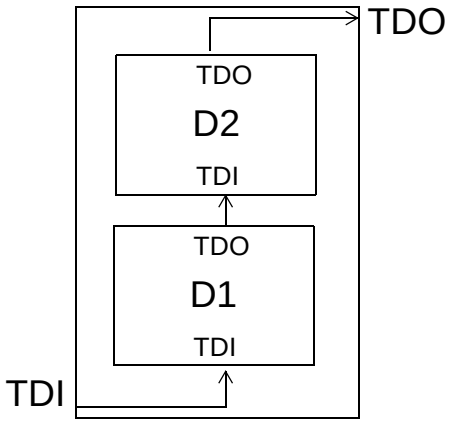


Figure 4. Scan Chain for 9-Mbit Device

Table 4. Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0h	Reserved for version number.
Cypress Device ID (27:12)	C002h	Defines Cypress part number for CYD04S36V, CYD09S36V and CYD18S36V
	C001h	Defines Cypress part number for CYD02S36V
	C092h	Defines Cypress part number for CYD01S36V
Cypress JEDEC ID (11:1)	034h	Allows unique identification of the DP family device vendor.
ID Register Presence (0)	1	Indicates the presence of an ID register.

Table 5. Scan Register Sizes

Register Name	Bit Size
Instruction	4
Bypass	1
Identification	32
Boundary Scan	n[24]

Note:
24. See details in the device BSDL files.

Table 6. Instruction Identification Codes

Instruction	Code	Description
EXTEST	0000	Captures the Input/Output ring contents. Places the BSR between the TDI and TDO.
BYPASS	1111	Places the BYR between TDI and TDO.
IDCODE	1011	Loads the IDR with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0111	Places BYR between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0100	Controls boundary to 1/0. Places BYR between TDI and TDO.
SAMPLE/PRELOAD	1000	Captures the input/output ring contents. Places BSR between TDI and TDO.
NBSRST	1100	Resets the non-boundary scan logic. Places BYR between TDI and TDO.
RESERVED	All other codes	Other combinations are reserved. Do not use other than the above.

Maximum Ratings[25]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with

Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential .....–0.5V to +4.6V

DC Voltage Applied to
Outputs in High-Z State.....–0.5V to V_{DD} +0.5V

DC Input Voltage.....–0.5V to V_{DD} + 0.5V[26]

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage.....> 2000V

(JEDEC JESD22-A114-2000B)

Latch-up Current.....> 200 mA

Operating Range

Range	Ambient Temperature	$V_{DDIO/VTTL}$	V_{CORE}[13]
Commercial	0°C to +70°C	3.3V±165 mV	1.8V±100 mV
Industrial	–40°C to +85°C	3.3V±165 mV	1.8V±100 mV

Electrical Characteristics Over the Operating Range

Parameter	Description		-167			-133			-100			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{DD} = Min., I_{OH}= –4.0 mA)		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{DD} = Min., I_{OL}= +4.0 mA)				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.0			2.0			2.0			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	–10		10	µA
I_{IX1}	Input Leakage Current Except TDI, TMS, $\overline{MRST}$		–10		10	–10		10	–10		10	µA
I_{IX2}	Input Leakage Current TDI, TMS, $\overline{MRST}$		–1.0		0.1	–1.0		0.1	–1.0		0.1	mA
I_{CC}	Operating Current for (V_{DD} = Max.,I_{OUT} = 0 mA), Outputs Disabled	CYD01S36V CYD02S36V/ CYD04S36V		225	300		225	300				mA
		CYD09S36V		450	600		370	540				
		CYD18S36V					410	580		315	450	
I_{SB1}[27]	Standby Current (Both Ports TTL Level) CE_L and $CE_R \geq V_{IH}$, f = f_{MAX}			90	115		90	115				mA
I_{SB2}[27]	Standby Current (One Port TTL Level) CE_L | $CE_R \geq V_{IH}$, f = f_{MAX}			160	210		160	210				mA
I_{SB3}[27]	Standby Current (Both Ports CMOS Level) CE_L and $CE_R \geq V_{DD}$ – 0.2V, f = 0			55	75		55	75				mA
I_{SB4}[27]	Standby Current (One Port CMOS Level) CE_L | $CE_R \geq V_{IH}$, f = f_{MAX}			160	210		160	210				mA
I_{SB5}	Operating Current (VDDIO = Max, Iout = 0 mA, f = 0) Outputs Disabled	CYD18S36V						75			75	mA
I_{CORE}[13]	Core Operating Current for (V_{DD} = Max., I_{OUT} = 0 mA), Outputs Disabled			0	0		0	0		0	0	mA

Capacitance [28]

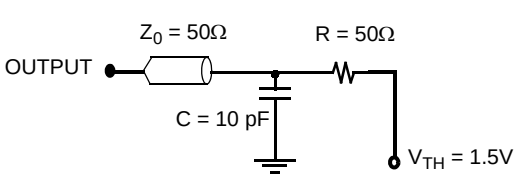
Part Number	Parameter	Description	Test Conditions	Max.	Unit
CYD01S36/ CYD02S36V/ CYD04S36V	C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V	13	pF
	C_{OUT}	Output Capacitance		10	pF
CYD09S36V	C_{IN}	Input Capacitance		22	pF
	C_{OUT}	Output Capacitance		10[29]	pF

Notes:
25. The voltage on any input or I/O pin can not exceed the power pin during power-up.
26. Pulse width < 20 ns.
27. I_{SB1}, I_{SB2}, I_{SB3} and I_{SB4} are not applicable for CYD18S36V because it cannot be powered down by using chip enable pins.
28. C_{OUT} also references $C_{I/O}$.
29. Except INT and CNTINT which are 20 pF.

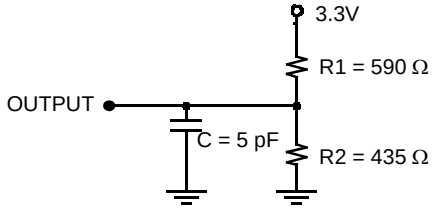
Capacitance (continued)[28]

Part Number	Parameter	Description	Test Conditions	Max.	Unit
CYD18S36V	C_{IN}	Input Capacitance		40	pF
	C_{OUT}	Output Capacitance		20	pF

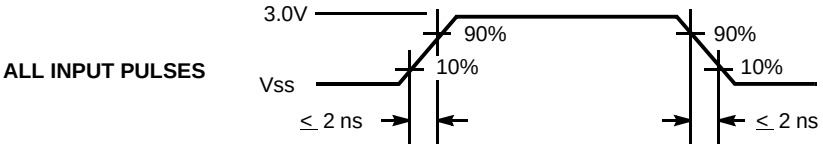
AC Test Load and Waveforms



(a) Normal Load (Load 1)



(b) Three-state Delay (Load 2)



Switching Characteristics Over the Operating Range

Parameter	Description	-167		-133				-100		Unit
		CYD01S36V CYD02S36V CYD04S36V CYD09S36V		CYD01S36V CYD02S36V CYD04S36V CYD09S36V		CYD18S36V		CYD18S36V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX2}	Maximum Operating Frequency		167		133		133		100	MHz
t_{CYC2}	Clock Cycle Time	6.0		7.5		7.5		10.0		ns
t_{CH2}	Clock HIGH Time	2.7		3.0		3.4		4.5		ns
t_{CL2}	Clock LOW Time	2.7		3.0		3.4		4.5		ns
t_R[30]	Clock Rise Time		2.0		2.0		2.0		3.0	ns
t_F[30]	Clock Fall Time		2.0		2.0		2.0		3.0	ns
t_{SA}	Address Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HA}	Address Hold Time	0.6		0.6		1.0		1.0		ns
t_{SB}	Byte Select Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HB}	Byte Select Hold Time	0.6		0.6		1.0		1.0		ns
t_{SC}	Chip Enable Set-up Time	2.3		2.5		NA		NA		ns
t_{HC}	Chip Enable Hold Time	0.6		0.6		NA		NA		ns
t_{SW}	R/$\overline{W}$ Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HW}	R/$\overline{W}$ Hold Time	0.6		0.6		1.0		1.0		ns
t_{SD}	Input Data Set-up Time	2.3		2.5		2.2		2.7		ns
t_{HD}	Input Data Hold Time	0.6		0.6		1.0		1.0		ns
t_{SAD}	$\overline{ADS}$ Set-up Time	2.3		2.5		NA		NA		ns
t_{HAD}	$\overline{ADS}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SCN}	$\overline{CNTEN}$ Set-up Time	2.3		2.5		NA		NA		ns
t_{HCN}	$\overline{CNTEN}$ Hold Time	0.6		0.6		NA		NA		ns

Note:
30. Except JTAG signals (t_r and t_f < 10 ns [max.]).

Switching Characteristics Over the Operating Range (continued)

Parameter	Description	-167		-133				-100		Unit
		CYD01S36V CYD02S36V CYD04S36V CYD09S36V		CYD01S36V CYD02S36V CYD04S36V CYD09S36V		CYD18S36V		CYD18S36V		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SRST}	$\overline{CNTRST}$ Set-up Time	2.3		2.5		NA		NA		ns
t_{HRST}	$\overline{CNTRST}$ Hold Time	0.6		0.6		NA		NA		ns
t_{SCM}	CNT/$\overline{MSK}$ Set-up Time	2.3		2.5		NA		NA		ns
t_{HCM}	CNT/$\overline{MSK}$ Hold Time	0.6		0.6		NA		NA		ns
t_{OE}	Output Enable to Data Valid		4.0		4.4		5.5		5.5	ns
t_{OLZ}[31, 32]	$\overline{OE}$ to Low Z	0		0		0		0		ns
t_{OHZ}[31, 32]	$\overline{OE}$ to High Z	0	4.0	0	4.4	0	5.5	0	5.5	ns
t_{CD2}	Clock to Data Valid		4.0		4.4		5.0		5.2	ns
t_{CA2}	Clock to Counter Address Valid		4.0		4.4		NA		NA	ns
t_{CM2}	Clock to Mask Register Readback Valid		4.0		4.4		NA		NA	ns
t_{DC}	Data Output Hold After Clock HIGH	1.0		1.0		1.0		1.0		ns
t_{CKHZ}[31, 32]	Clock HIGH to Output High Z	0	4.0	0	4.4	0	4.7	0	5.0	ns
t_{CKLZ}[31, 32]	Clock HIGH to Output Low Z	1.0	4.0	1.0	4.4	1.0	4.7	1.0	5.0	ns
t_{SINT}	Clock to $\overline{INT}$ Set Time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10.0	ns
t_{RINT}	Clock to $\overline{INT}$ Reset Time	0.5	6.7	0.5	7.5	0.5	7.5	0.5	10.0	ns
t_{SCINT}	Clock to $\overline{CNTINT}$ Set Time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
t_{RCINT}	Clock to $\overline{CNTINT}$ Reset time	0.5	5.0	0.5	5.7	NA	NA	NA	NA	ns
Port to Port Delays										
t_{CCS}	Clock to Clock Skew	5.2		6.0		5.7		8.0		ns
Master Reset Timing										
t_{RS}	Master Reset Pulse Width	5.0		5.0		5.0		5.0		cycles
t_{RS}	Master Reset Set-up Time	6.0		6.0		6.0		8.5		ns
t_{RSR}	Master Reset Recovery Time	5.0		5.0		5.0		5.0		cycles
t_{RSF}	Master Reset to Outputs Inactive		10.0		10.0		10.0		10.0	ns
t_{RSINT}	Master Reset to Counter and Mailbox Interrupt Flag Reset Time		10.0		10.0		NA		NA	ns

JTAG Timing

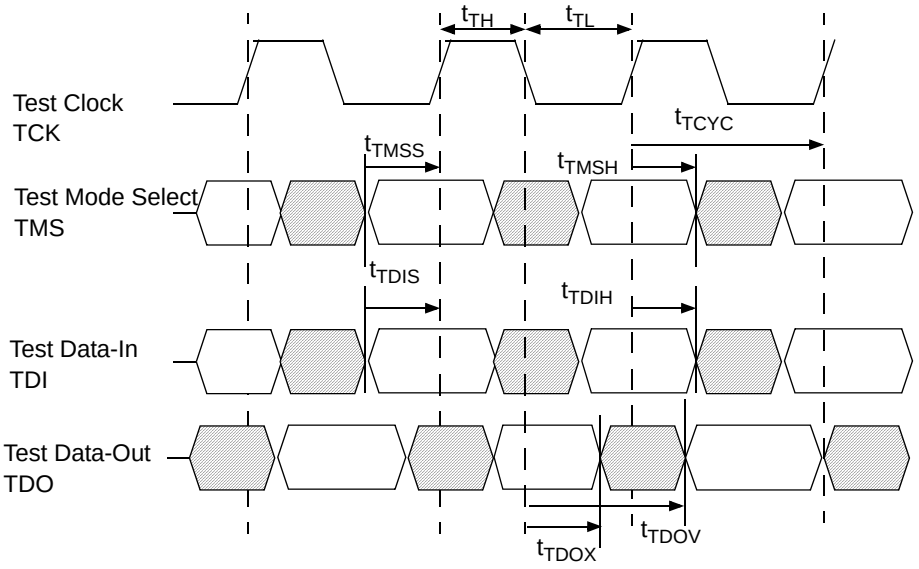
Parameter	Description	167/133/100		Unit
		Min.	Max.	
f_{JTAG}	Maximum JTAG TAP Controller Frequency		10	MHz
t_{TCYC}	TCK Clock Cycle Time	100		ns
t_{TH}	TCK Clock HIGH Time	40		ns
t_{TL}	TCK Clock LOW Time	40		ns
t_{TMSS}	TMS Set-up to TCK Clock Rise	10		ns
t_{TMSH}	TMS Hold After TCK Clock Rise	10		ns

Notes:
31. This parameter is guaranteed by design, but it is not production tested.
32. Test conditions used are Load 2.

JTAG Timing (continued)

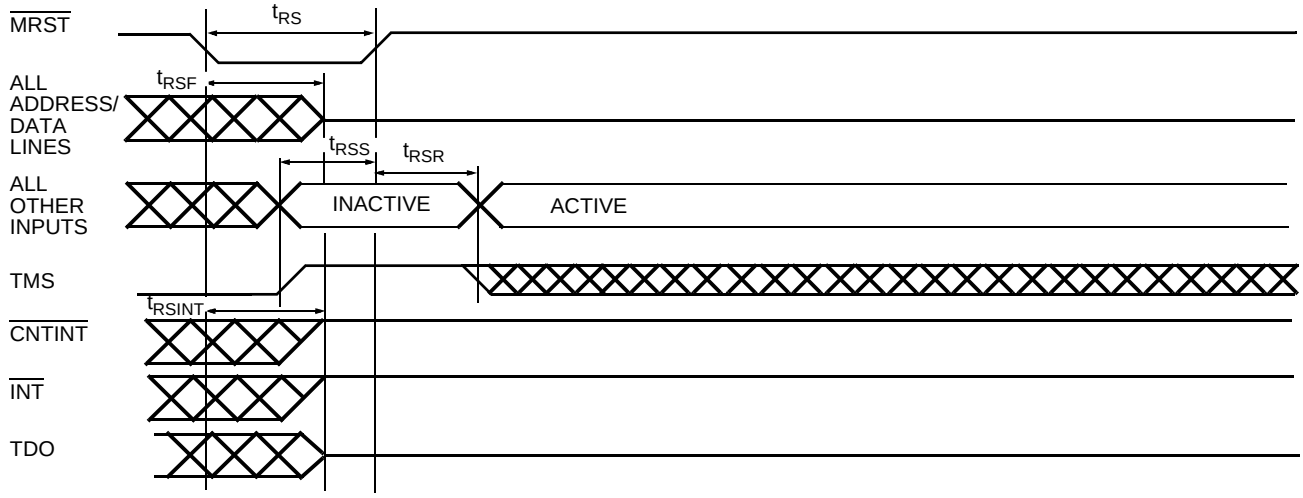
Parameter	Description	167/133/100		Unit
		Min.	Max.	
t_{TDIS}	TDI Set-up to TCK Clock Rise	10		ns
t_{TDIH}	TDI Hold After TCK Clock Rise	10		ns
t_{TDOV}	TCK Clock LOW to TDO Valid		30	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns

JTAG Switching Waveform



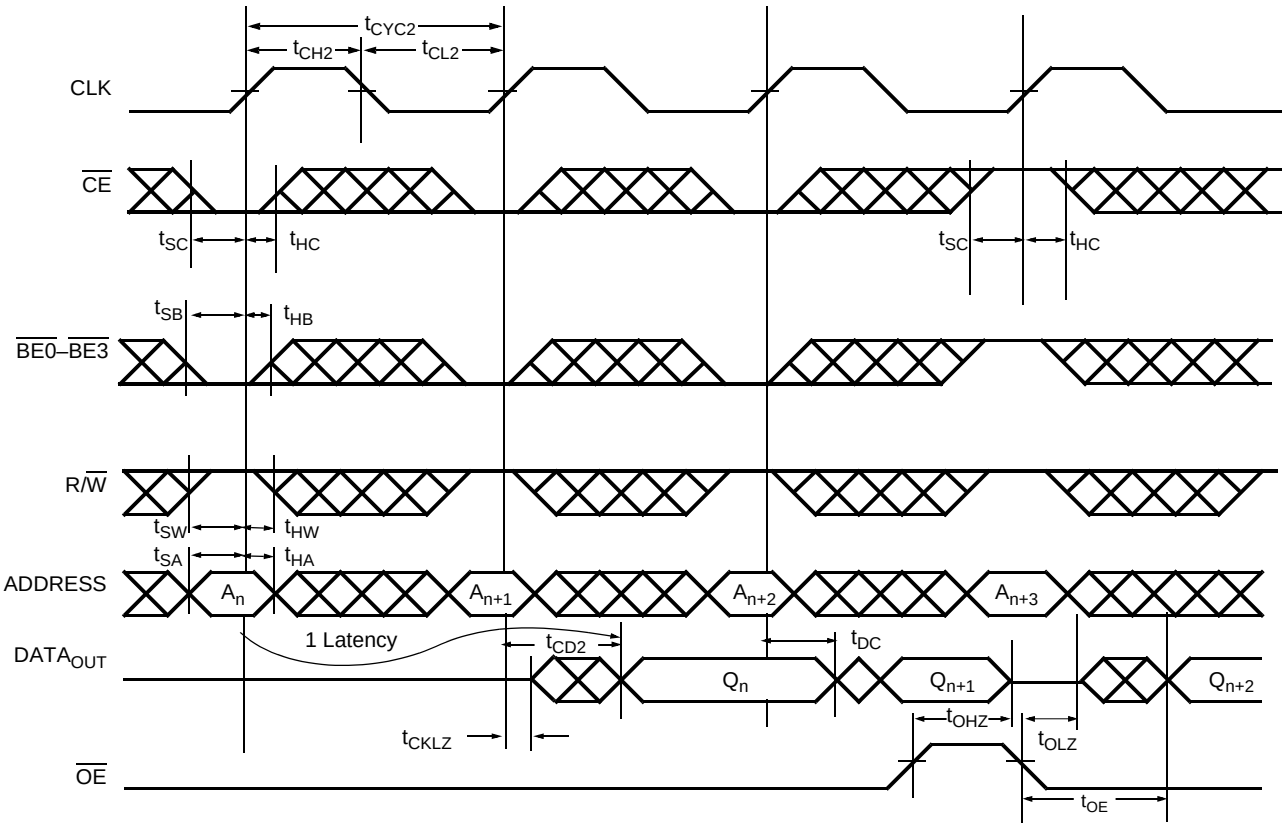
Switching Waveforms

Master Reset



Switching Waveforms (continued)

Read Cycle[14, 33, 34, 35, 36]

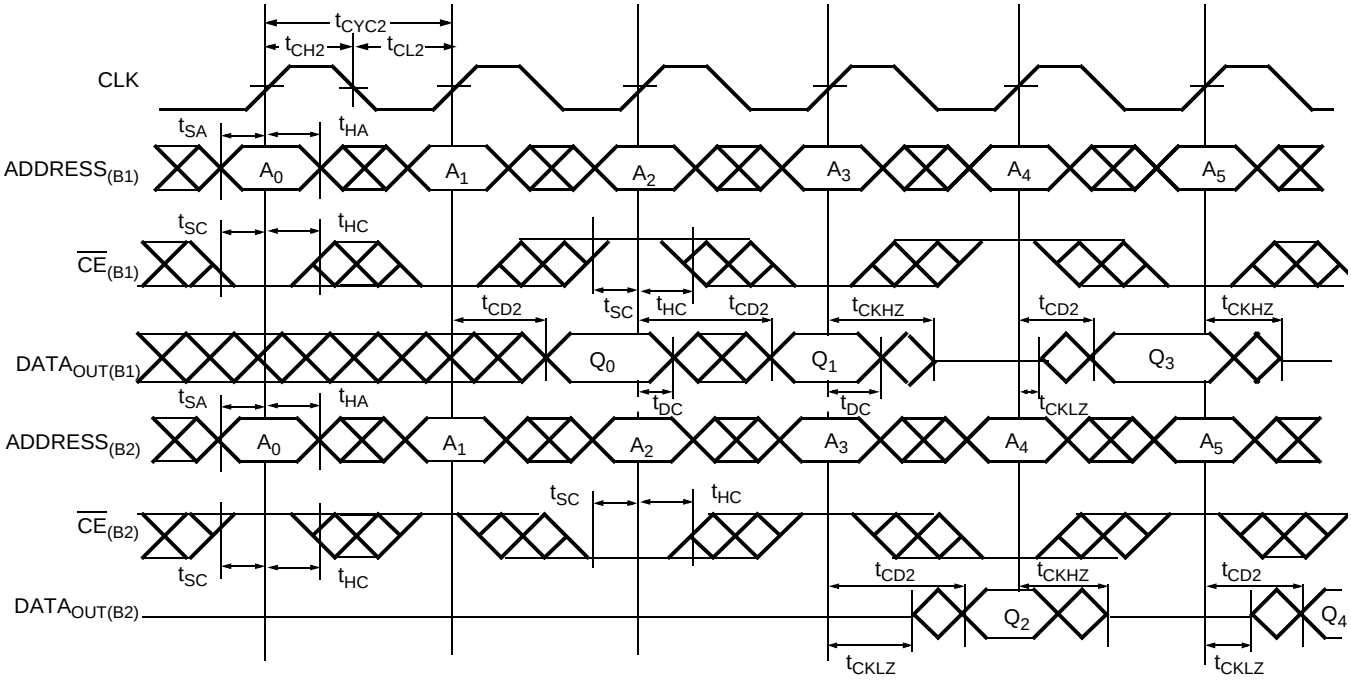


Notes:

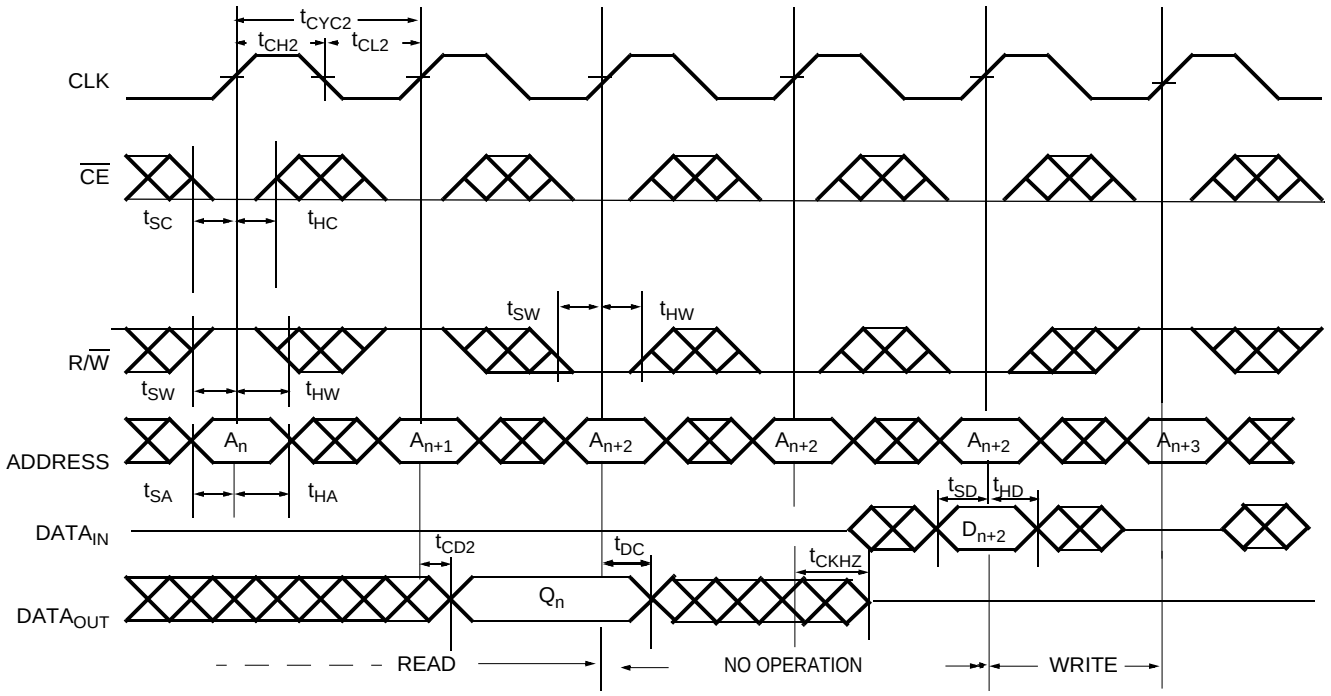
33. OE is asynchronously controlled; all other inputs (excluding MRST and JTAG) are synchronous to the rising clock edge.
34. ADS = CNTEN = LOW, and MRST = CNTRST = CNT/MSK = HIGH.
35. The output is disabled (high-impedance state) by CE = V_{IH} following the next rising edge of the clock.
36. Addresses do not have to be accessed sequentially since ADS = CNTEN = V_{IL} with CNT/MSK = V_{IH} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms (continued)

Bank Select Read[37, 38]



Read-to-Write-to-Read ($\overline{OE}$ = LOW)[36, 39, 40, 41, 42]

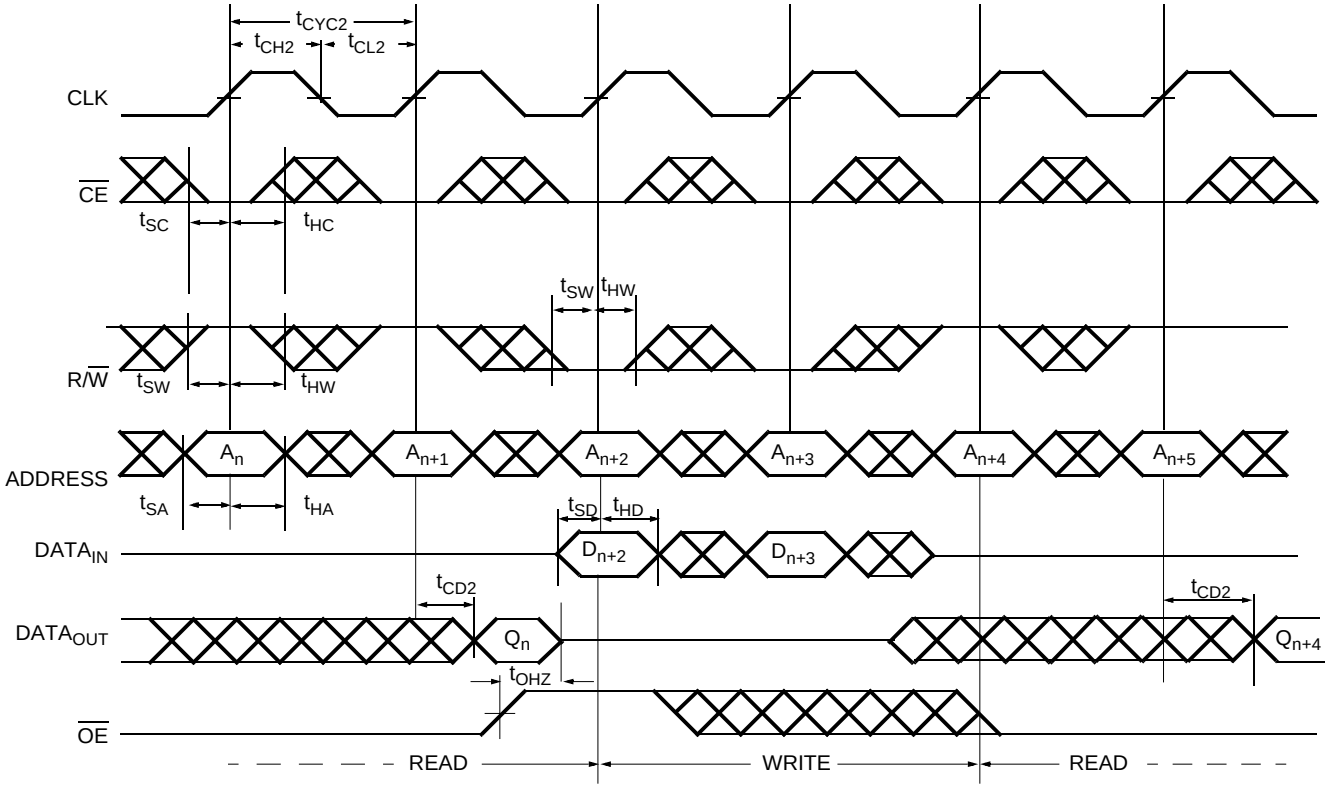


Notes:

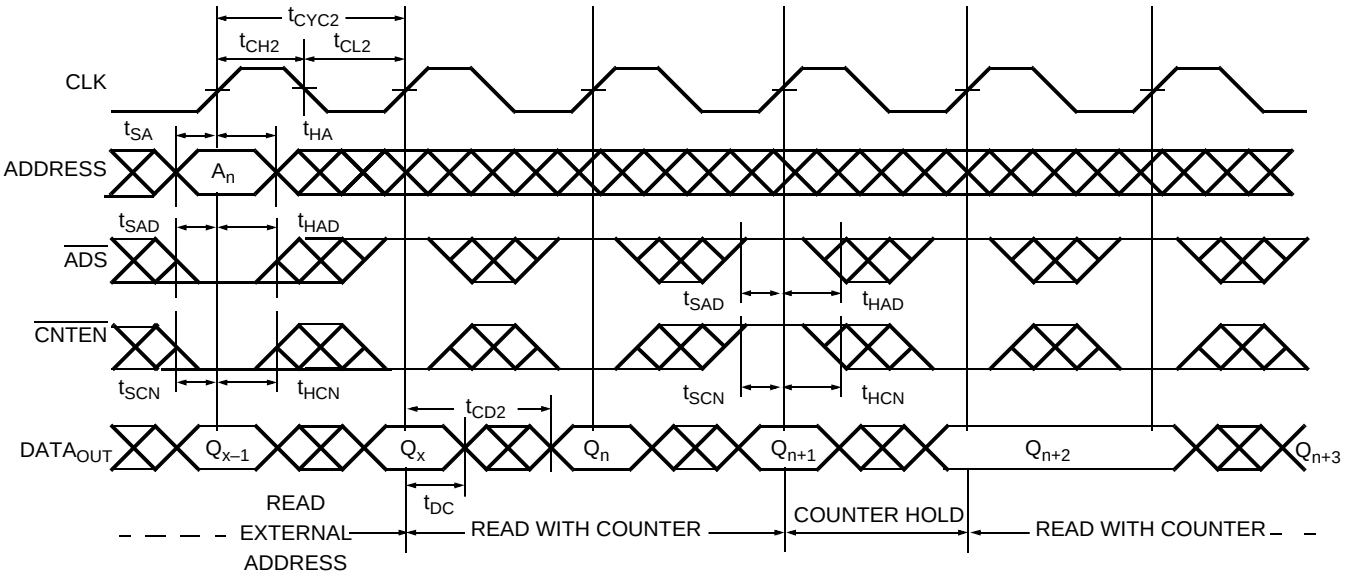
37. In this depth-expansion example, B1 represents Bank #1 and B2 is Bank #2; each bank consists of one Cypress FLEx36 device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
38. $\overline{ADS}$ = $\overline{CNTEN}$= $\overline{BE0}$ – $\overline{BE3}$ = $\overline{OE}$ = LOW; $\overline{MRST}$ = $\overline{CNTRST}$ = CNT/$\overline{MSK}$ = HIGH.
39. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
40. During "No Operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.
41. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
42. $\overline{CE_0}$ = $\overline{BE0}$ – $\overline{BE3}$ = R/$\overline{W}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH. When R/$\overline{W}$ first switches low, since OE = LOW, the Write operation cannot be completed (labelled as no operation). One clock cycle is required to three-state the I/O for the Write operation on the next rising edge of CLK.

Switching Waveforms (continued)

Read-to-Write-to-Read ($\overline{OE}$ Controlled)[36, 39, 41, 42]

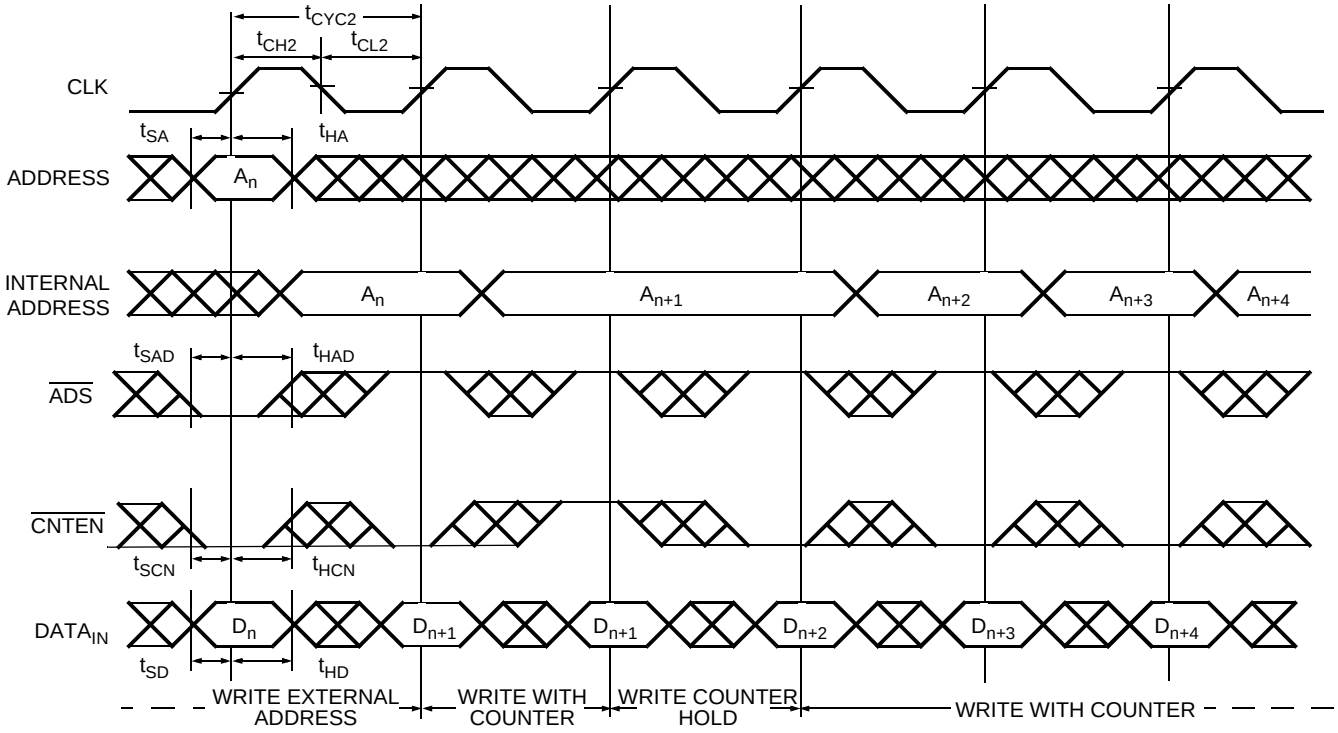


Read with Address Counter Advance[41]



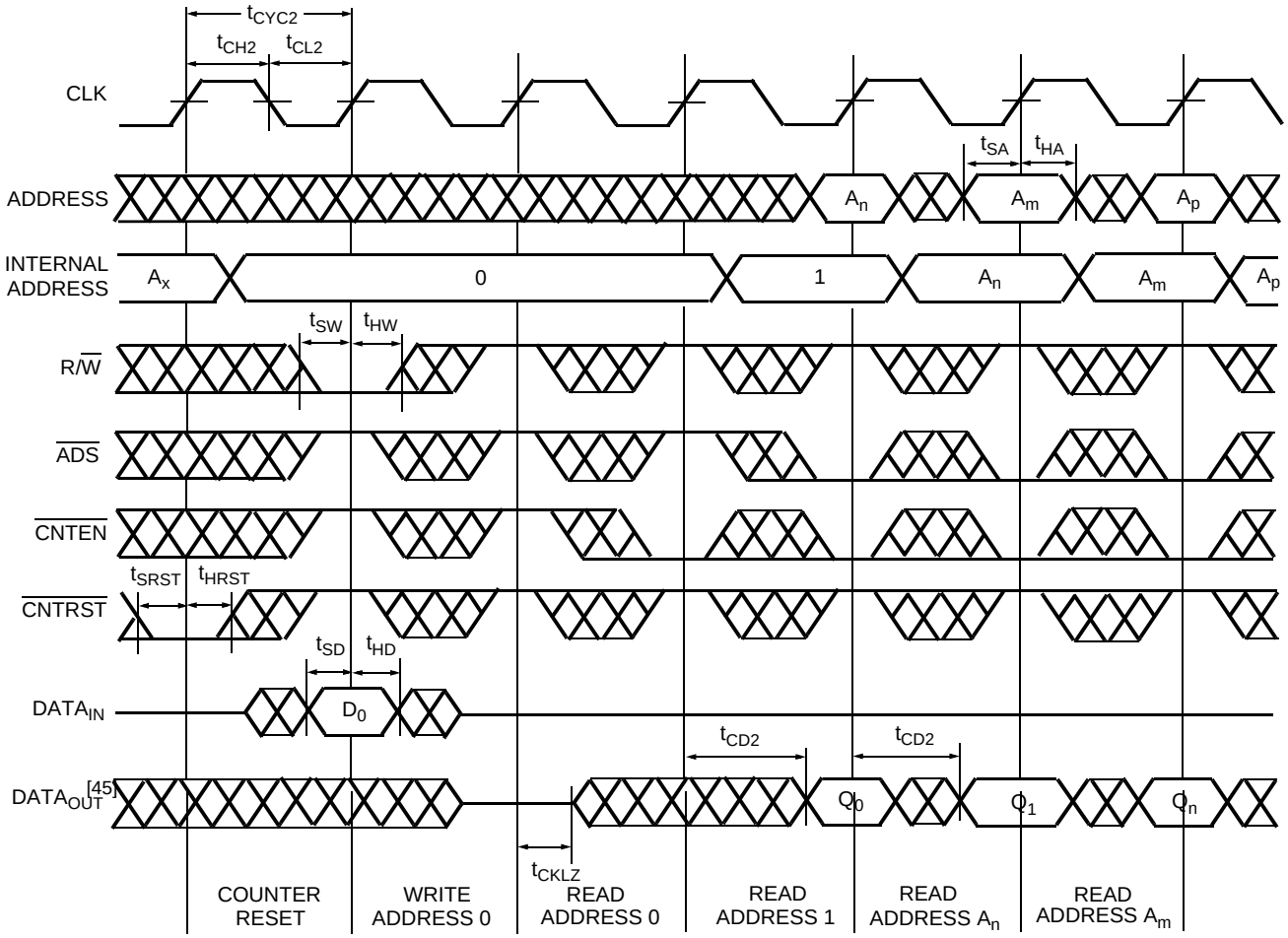
Switching Waveforms (continued)

Write with Address Counter Advance [42]



Switching Waveforms (continued)

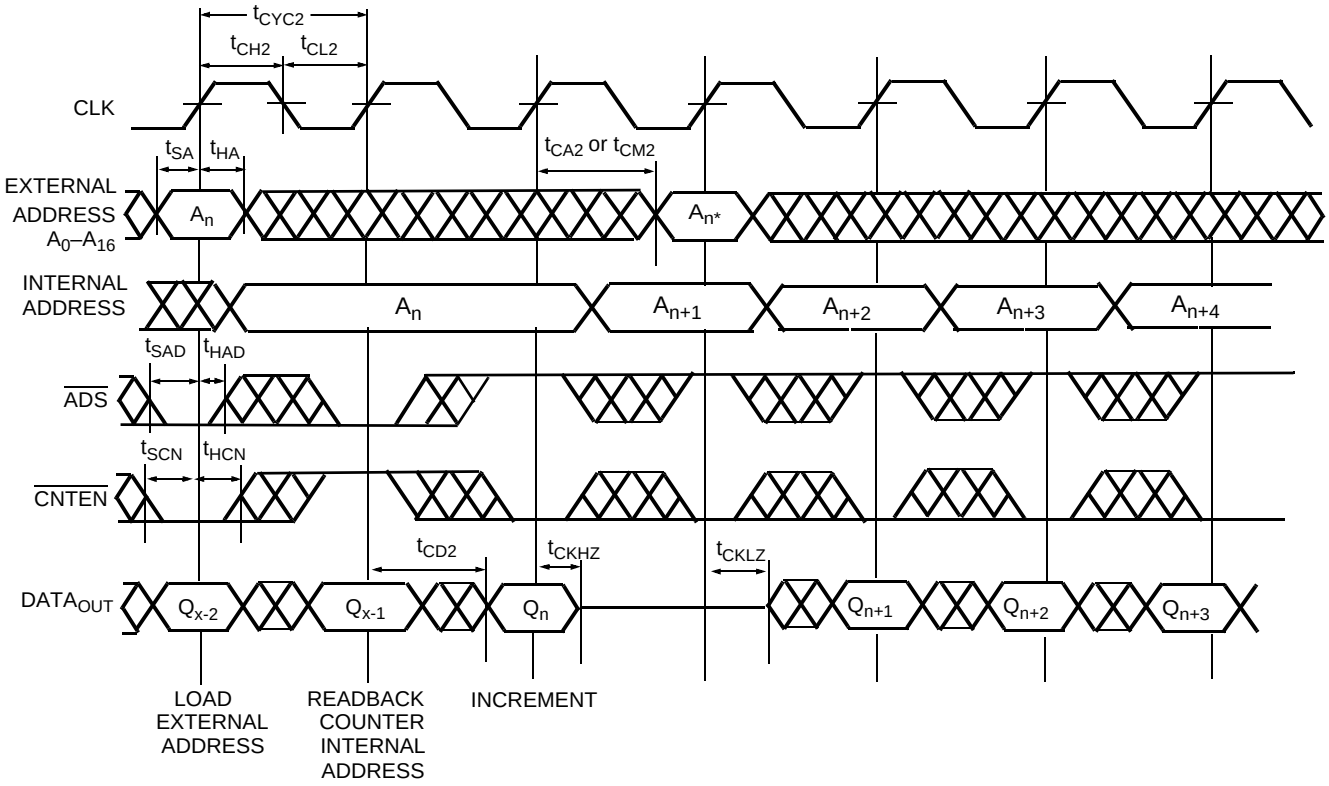
Counter Reset [43, 44]



Notes:
43. $\overline{CE_0}$ = $\overline{BE0}$ – $\overline{BE3}$ = LOW; CE_1 = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
44. No dead cycle exists during counter reset. A Read or Write cycle may be coincidental with the counter reset.
45. Retransmit happens if the counter remains in increment mode after it wraps to initially loaded value

Switching Waveforms (continued)

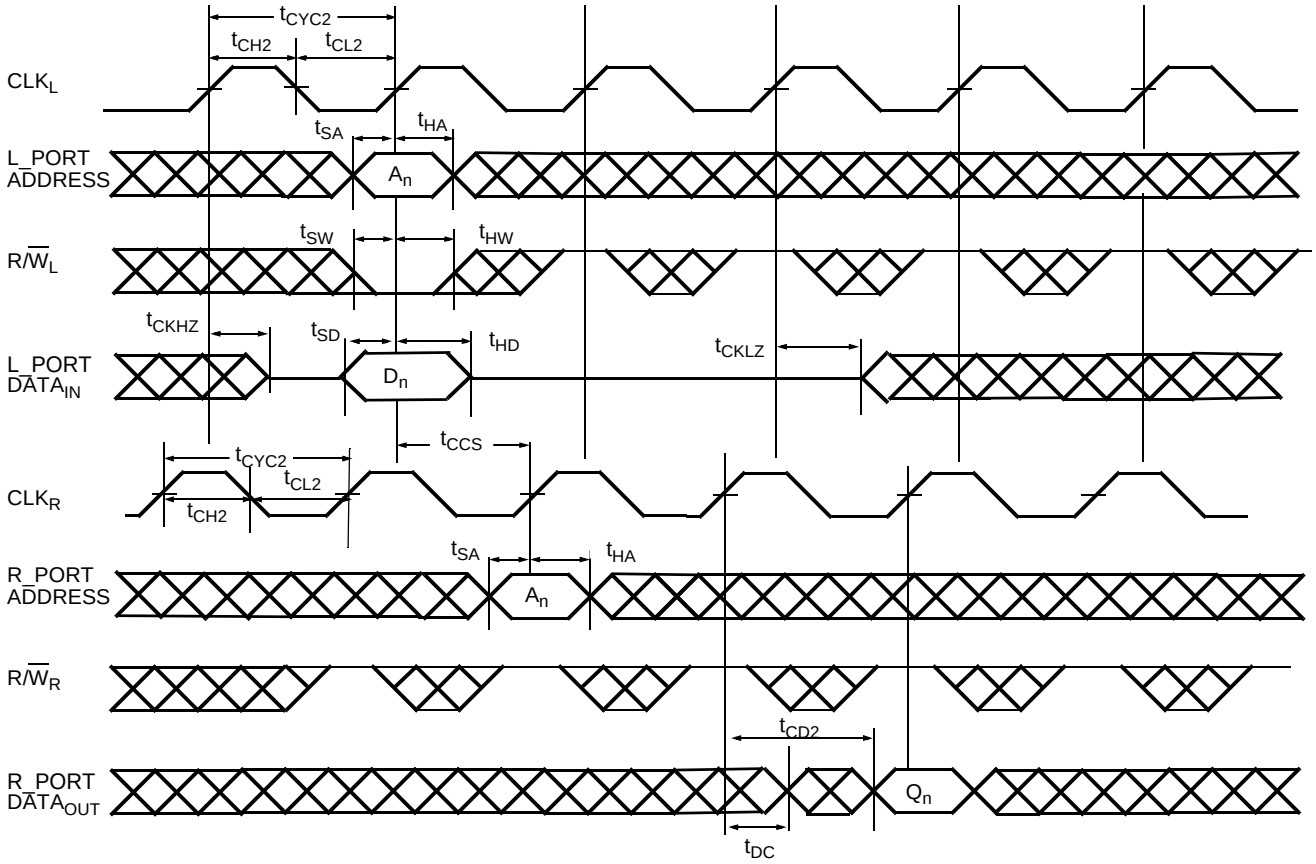
Readback State of Address Counter or Mask Register[46, 47, 48, 49]



Notes:
46. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
47. Address in output mode. Host must not be driving address bus after t_{CKLZ} in next clock cycle.
48. Address in input mode. Host can drive address bus after t_{CKHZ}.
49. An * is the internal value of the address counter (or the mask register depending on the CNT/$\overline{MSK}$ level) being Read out on the address lines.

Switching Waveforms (continued)

Left_Port (L_Port) Write to Right_Port (R_Port) Read[50, 51, 52]

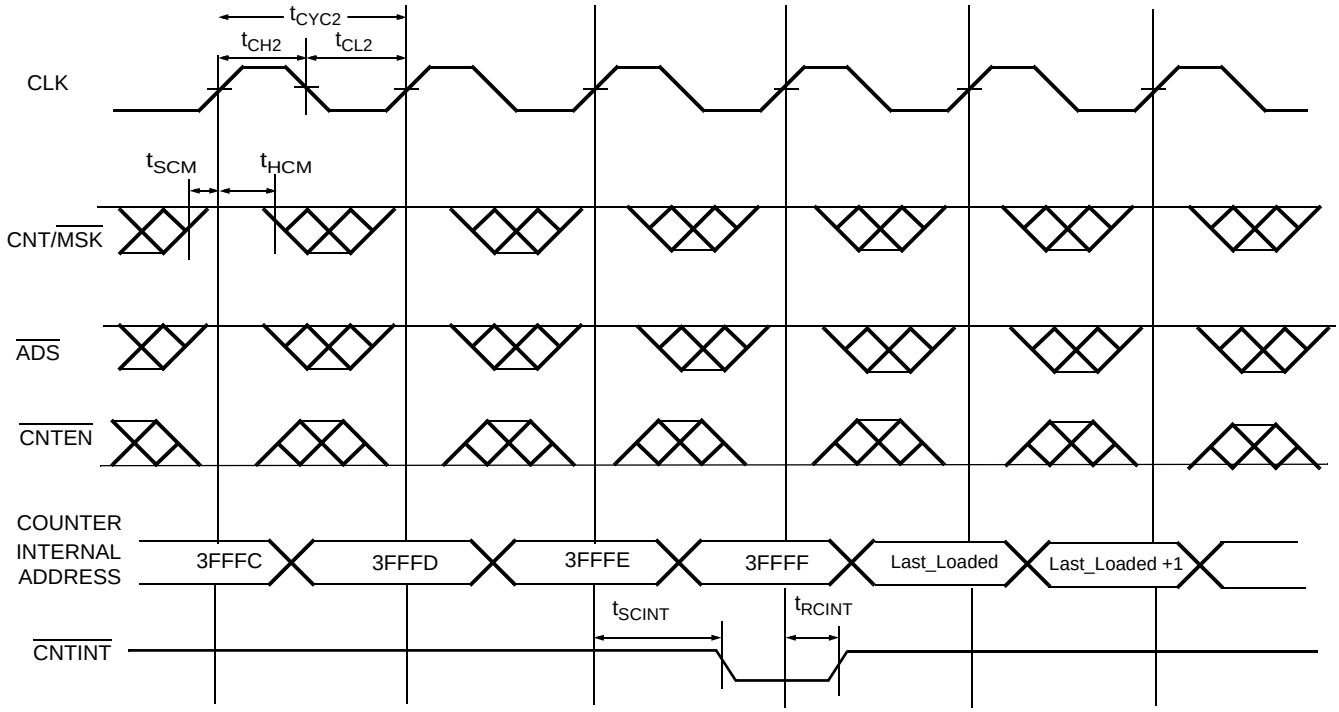


Notes:

50. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = $\overline{BE0}$ – $\overline{BE3}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
51. This timing is valid when one port is writing, and other port is reading the same location at the same time. If t_{CCS} is violated, indeterminate data will be Read out.
52. If t_{CCS} < minimum specified value, then R_Port will Read the most recent data (written by L_Port) only (2 * t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock. If $t_{CCS} \geq$ minimum specified value, then R_Port will Read the most recent data (written by L_Port) (t_{CYC2} + t_{CD2}) after the rising edge of R_Port's clock.

Switching Waveforms (continued)

Counter Interrupt and Retransmit[17, 45, 53, 54, 55, 56]



Notes:
53. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{BE0}$ – $\overline{BE3}$ = LOW; CE_1 = R/$\overline{W}$ = $\overline{CNTRST}$ = $\overline{MRST}$ = HIGH.
54. $\overline{CNTINT}$ is always driven.
55. CNTINT goes LOW when the unmasked portion of the address counter is incremented to the maximum value.
56. The mask register assumed to have the value of 3FFFFh.

Switching Waveforms (continued)

MailBox Interrupt Timing[57, 58, 59, 60, 61]

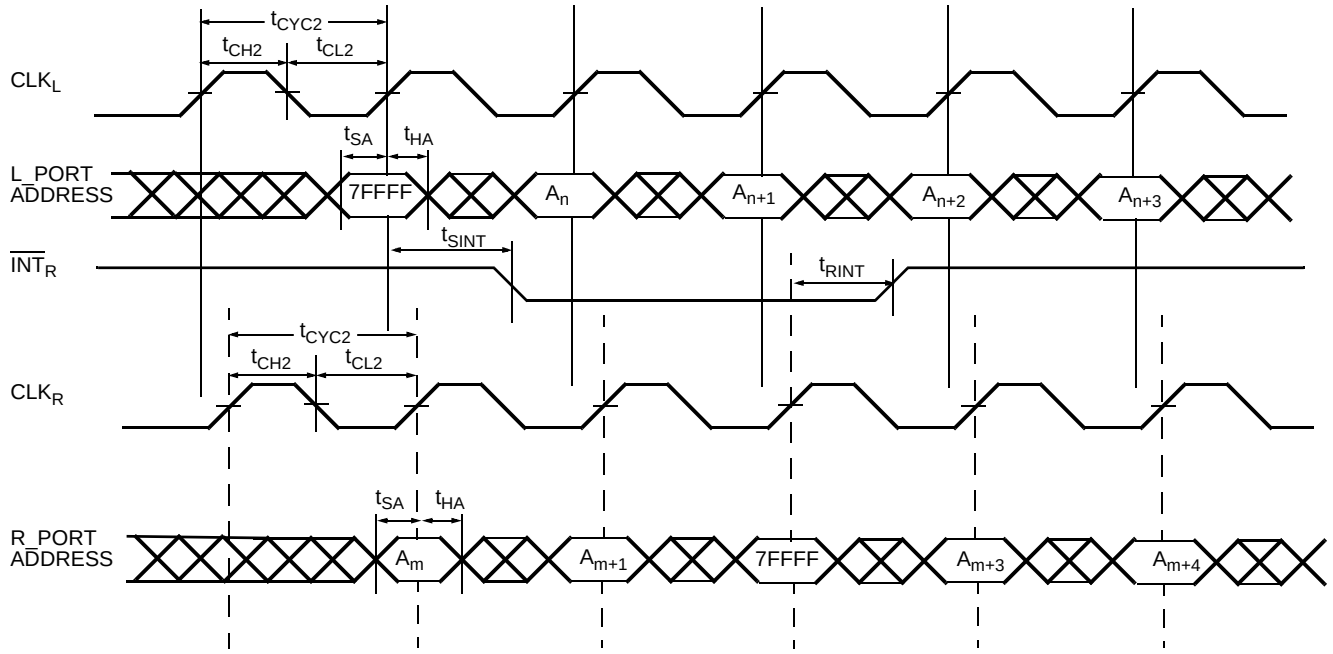


Table 7. Read/Write and Enable Operation (Any Port)[1, 18, 62, 63, 64]

Inputs					Outputs	
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	$DQ_0 - DQ_{35}$	Operation
X	↑	H	X	X	High-Z	Deselected
X	↑	X	L	X	High-Z	Deselected
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read
H	X	L	H	X	High-Z	Outputs Disabled

Notes:
57. $\overline{CE_0}$ = $\overline{OE}$ = $\overline{ADS}$ = $\overline{CNTEN}$ = LOW; CE_1 = $\overline{CNTRST}$ = $\overline{MRST}$ = CNT/$\overline{MSK}$ = HIGH.
58. Address “7FFFF” is the mailbox location for R_Port of the 9-Mbit device.
59. L_Port is configured for Write operation, and R_Port is configured for Read operation.
60. At least one byte enable ($\overline{BE0}$ – $\overline{BE3}$) is required to be active during interrupt operations.
61. Interrupt flag is set with respect to the rising edge of the Write clock, and is reset with respect to the rising edge of the Read clock.
62. $\overline{OE}$ is an asynchronous input signal.
63. When $\overline{CE}$ changes state, deselection and Read happen after one cycle of latency.
64. $\overline{CE_0}$ = $\overline{OE}$ = LOW; CE_1 = R/$\overline{W}$ = HIGH.

Ordering Information

512K × 36 (18-Mbit) 3.3V Synchronous CYD18S36V Dual-Port SRAM

Speed(MHz)	Ordering Code	Package Name	Package Type	Operating Range
133	CYD18S36V-133BBC	BB256B	256-ball Grid Array 23 mm × 23 mm with 1.0-mm pitch (BGA)	Commercial
	CYD18S36V-133BBI	BB256B	256-ball Grid Array 23 mm × 23 mm with 1.0-mm pitch (BGA)	Industrial
100	CYD18S36V-100BBC	BB256B	256-ball Grid Array 23 mm × 23 mm with 1.0-mm pitch (BGA)	Commercial
	CYD18S36V-100BBI	BB256B	256-ball Grid Array 23 mm × 23 mm with 1.0-mm pitch (BGA)	Industrial

256K × 36 (9-Mbit) 3.3V Synchronous CYD09S36V Dual-Port SRAM

Speed(MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CYD09S36V-167BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
133	CYD09S36V-133BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
	CYD09S36V-133BBI	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Industrial

128K × 36 (4-Mbit) 3.3V Synchronous CYD04S36V Dual-Port SRAM

Speed(MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CYD04S36V-167BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
133	CYD04S36V-133BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
	CYD04S36V-133BBI	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Industrial

64K × 36 (2-Mbit) 3.3V Synchronous CYD02S36V Dual-Port SRAM

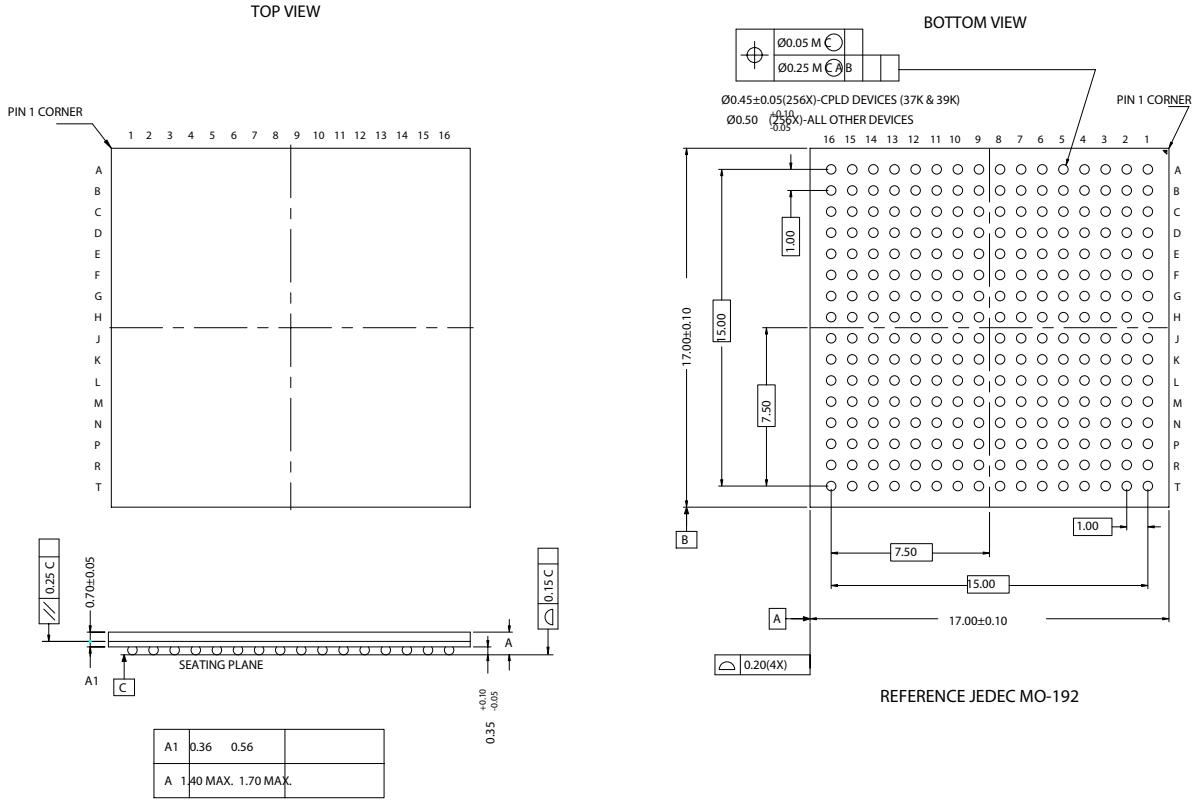
Speed(MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CYD02S36V-167BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
133	CYD02S36V-133BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
	CYD02S36V-133BBI	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Industrial

32K × 36 (1-Mbit) 3.3V Synchronous CYD01S36V Dual-Port SRAM

Speed(MHz)	Ordering Code	Package Name	Package Type	Operating Range
167	CYD01S36V-167BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
133	CYD01S36V-133BBC	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Commercial
	CYD01S36V-133BBI	BB256	256-ball Grid Array 17 mm × 17 mm with 1.0-mm pitch (BGA)	Industrial

Package Diagrams

256-Ball FBGA (17 x 17 mm) BB256



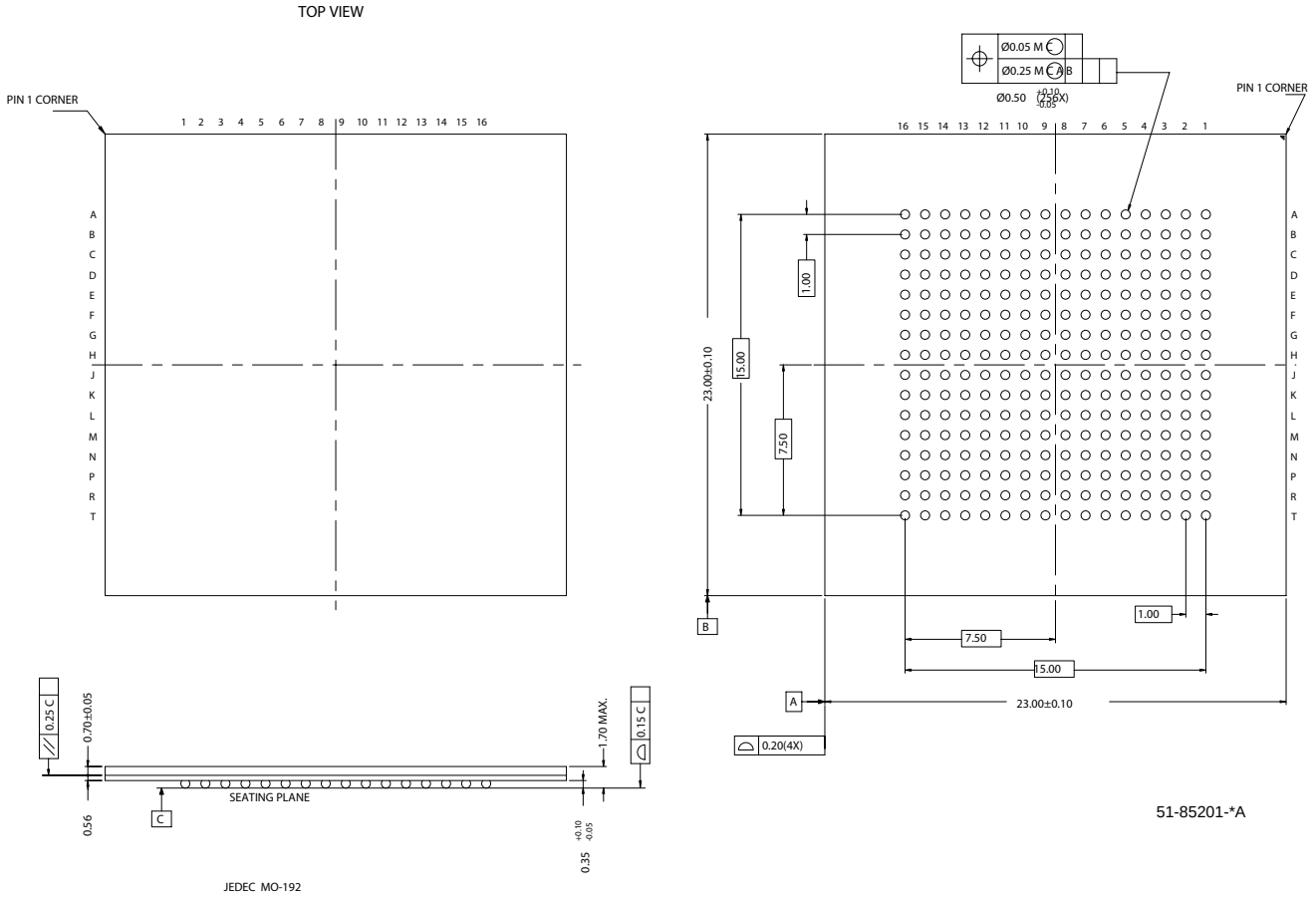
A1	0.36	0.56	
A	1.40 MAX.	1.70 MAX.	

REFERENCE JEDEC MO-192

51-85108-*F

Package Diagrams (continued)

256-ball FBGA (23 mm x 23 mm x 1.7 mm) BB256B



Document History Page

Document Title: FLEx36™ 3.3V 32K/64K/128K/256K/512 x 36 Synchronous Dual-Port RAM Document Number: 38-06076				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	232012	See ECN	WWZ	New data sheet
*A	244232	See ECN	WWZ	Changed pinout Changed FTSEL# to $\overline{\text{FTSEL}}$ in the block diagram
*B	313156	See ECN	YDT	Changed pinout D10 from NC to VSS to reflect test mode pin swap, C10 from rev[2,4] to VSS to reflect SC removal. Changed tRSCNTINT to tRSINT Added tRSINT to the master reset timing diagram Added CYD01S36V to data sheet Added I_{SB5} and changed I_{IX2}
*C	321033	See ECN	YDT	Added CYD18S36V-133BBI to the Ordering Information Section
*D	327338	See ECN	AEQ	Change Pinout C10 from VSS to NC[2,5] Change Pinout G5 from $VDDIO_L$ to REV_L[2,3]
*E	365315	See ECN	YDT	Added note for V_{CORE} Removed preliminary status