LH1531/M

64-Output LCD Common Driver LSI

DESCRIPTION

The LH1531/M is a 64-output common driver LSI suitable for driving middle or small size dot matrix LCD panels used in electronic organizer or PDA or pager. When combined with the LH1554 segment driver, a low power consuming LCD panel can be composed. Data input/output pins are bidirectional, four data shift directions are pin-selectable.

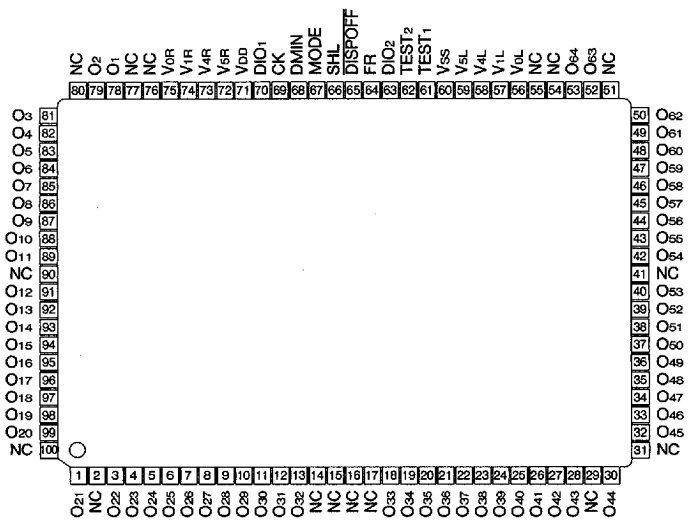
FEATURES

- Supply voltage for LCD drive
  : +10.0 to +30.0 V
- Number of LCD drive outputs : 64-output
- Supply voltage for the logic system
  : +2.5 to +5.5 V
- Low power consumption
- Low output impedance
- Shift clock frequency
  : 1.0 MHz (Max.) (V_{DD} = +5 V ±10%)
  0.5 MHz (Max.) (V_{DD} = +2.5 to +4.5 V)
- Built-in 64-bit bidirectional shift register (divisible into 32-bit×2)
- Shift register circuit reset function when $\overline{DISPOFF}$ active
- Available in a Single mode (64-bit shift register) or in a Dual mode (32-bit shift register×2)
  ① O_1 → O_{64} Single mode
  ② O_{64} → O_1 Single mode
  ③ O_1 → O_{32}, O_{33} → O_{64} Dual mode
  ④ O_{64} → O_{33}, O_{32} → O_1 Dual mode
- CMOS silicon gate process
- Supports-high resolution LCD panel when combined with the LH1554 segment driver
- Packages :
  LH1531 : Chip(84-PAD)
  LH1531M : 100-pin QFP(QFP0100-P-1420)

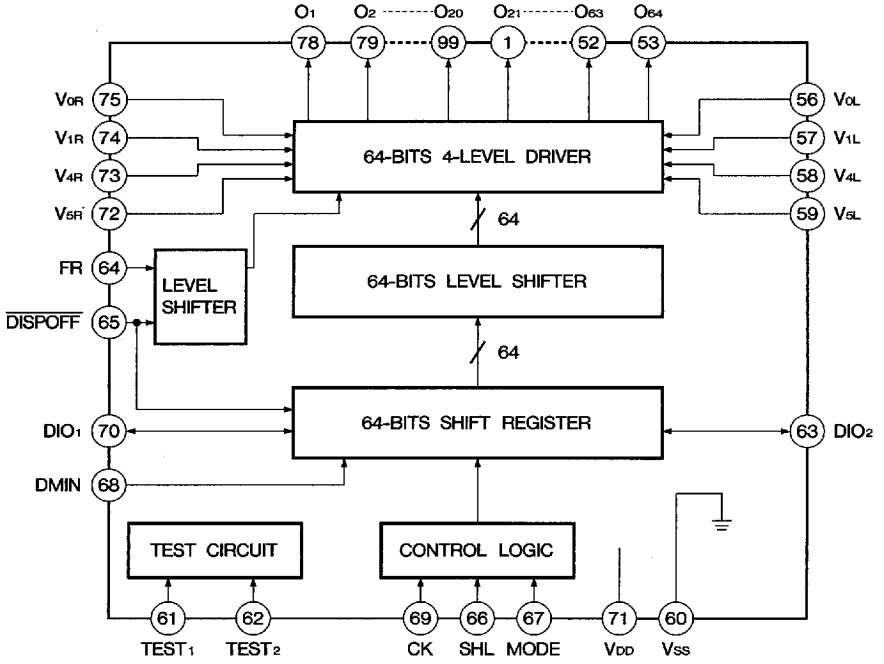
PIN CONNECTIONS

100-PIN QFP

TOP VIEW



BLOCK DIAGRAM



NOTE :
Pin numbers apply to 100-pin QFP.

FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Shift Register	Shifts data from the data input pin on the falling edge of the CK signal, based on the data shift direction and mode setting received from the control logic block.
Level Shifter	The logic voltage signal is level shifted to the LCD drive voltage level, and outputs to the driver block.
4-Level Driver	Drives the LCD drive output pins from the shift register data, selecting one of 4 levels (V_0, V_1, V_4, V_5) based on the FR and $\overline{DISPOFF}$ signals.
Control Logic	Controls the shift register's direction of data shift and mode setting in response to a SHL and MODE signal input.
Test Circuit	The circuit for the test. During normal operation, it doesn't act.

PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	O_{21}	O	LCD drive output
2	NC	–	
3 - 13	O_{22}-O_{32}	O	LCD drive output
14 - 17	NC	–	
18 - 28	O_{33}-O_{43}	O	LCD drive output
29	NC	–	
30	O_{44}	O	LCD drive output
31	NC	–	
32 - 40	O_{45}-O_{53}	O	LCD drive output
41	NC	–	
42 - 50	O_{54}-O_{62}	O	LCD drive output
51	NC	–	
52, 53	O_{63}, O_{64}	O	LCD drive output
54, 55	NC	–	
56	V_{0L}	–	Power supply for LCD drive
57	V_{1L}	–	Power supply for LCD drive
58	V_{4L}	–	Power supply for LCD drive
59	V_{5L}	–	Power supply for LCD drive
60	V_{SS}	–	Ground (0 V)
61	$TEST_1$	I	Test mode selection input
62	$TEST_2$	I	Test mode selection input
63	DIO_2	I/O	Data input/output for shift register
64	FR	I	AC-converting signal input for LCD drive waveform
65	$\overline{DISPOFF}$	I	Control input for deselect output level
66	SHL	I	Shift direction selection for shift register
67	MODE	I	Mode selection input
68	DMIN	I	Dual mode data input
69	CK	I	Shift clock input for shift register
70	DIO_1	I/O	Data input/output for shift register
71	V_{DD}	–	Power supply for logic system (+2.5 to +5.5 V)
72	V_{5R}	–	Power supply for LCD drive
73	V_{4R}	–	Power supply for LCD drive
74	V_{1R}	–	Power supply for LCD drive
75	V_{0R}	–	Power supply for LCD drive
76, 77	NC	–	
78, 79	O_1, O_2	O	LCD drive output
80	NC	–	
81 - 89	O_3-O_{11}	O	LCD drive output
90	NC	–	
91 - 99	O_{12}-O_{20}	O	LCD drive output
100	NC	–	

NOTE : Pin numbers apply to 100-pin QFP.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	−0.3 to +7.0	V	1, 2
Supply voltage (2)	V_O	V_{OL}, V_{OR}	−0.3 to +32.0	V	
	V_1	V_{1L}, V_{1R}	−0.3 to V_O+0.3	V	
	V_4	V_{4L}, V_{4R}	−0.3 to V_O+0.3	V	
	V_5	V_{5L}, V_{5R}	−0.3 to V_O+0.3	V	
Input voltage	V_I	DIO_1, DIO_2, DMIN, SHL MODE, CK, FR, $\overline{DISPOFF}$	−0.3 to V_{DD}+0.3	V	
Storage temperature	Tstg		−45 to +125	°C	

NOTES :

1. Ta=25°C
2. The maximum applicable voltage on any pin with respect to V_{SS} (0 V).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_O	V_{OL}, V_{OR}	+10.0		+30.0	V	
Operating temperature	Topr		−20		+85	°C	

NOTES :

1. Ensure that voltages are set such that $V_{SS} \leq V_5 < V_4 < V_1 < V_O$.
2. The applicable voltage on any pin with respect to Vss (0 V).

DC CHARACTERISTICS

($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ to $+5.5$ V, $V_O=+10.0$ to $+30.0$ V, Ta $=-20$ to $+85$°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input voltage	V_{IH}		DIO_1, DIO_2, CK, DMIN SHL, FR, $\overline{DISPOFF}$, MODE	0.8V_{DD}			V	
	V_{IL}					0.2V_{DD}	V	
Output voltage	V_{OH}	$I_{OH}=-0.4$ mA	DIO_1, DIO_2	$V_{DD}-0.4$			V	
	V_{OL}	$I_{OL}=+0.4$ mA				+0.4	V	
Input leakage current	I_{LI}	$V_{SS}\leq V_I\leq V_{DD}$	CK, SHL FR $\overline{DISPOFF}$ DMIN, MODE			±10.0	μA	
I/O leakage leak current	$I_{LI/O}$	$V_{SS}\leq V_I\leq V_{DD}$	DIO_1, DIO_2			±10.0	μA	
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5 V, $V_O=+30$ V	O_1-O_{64}			1.0	kΩ	
		$\lvert\Delta V_{ON}\rvert$ =0.5 V, $V_O=+20$ V				1.5	kΩ	
Stand-by current	I_{STB}		V_{SS}			50	μA	1
Supply current (1)	I_{DD}	$V_{DD}=+3.0$ V	V_{DD}			30.0	μA	2
		$V_{DD}=+5.0$ V				50.0	μA	
Supply current (2)	I_O	$V_{DD}=+3.0$ V	V_O			60.0	μA	
		$V_{DD}=+5.0$ V				100.0	μA	

NOTES :

1. $V_{DD}=+5.0$ V, $V_O=+30.0$ V, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$.
2. $V_{DD}=+5.0$ V, $V_O=+30.0$ V, $f_{CK}=10.2$ kHz, $f_{FR}=80$ Hz, case of 1/128 duty operation, no-load.

AC CHARACTERISTICS

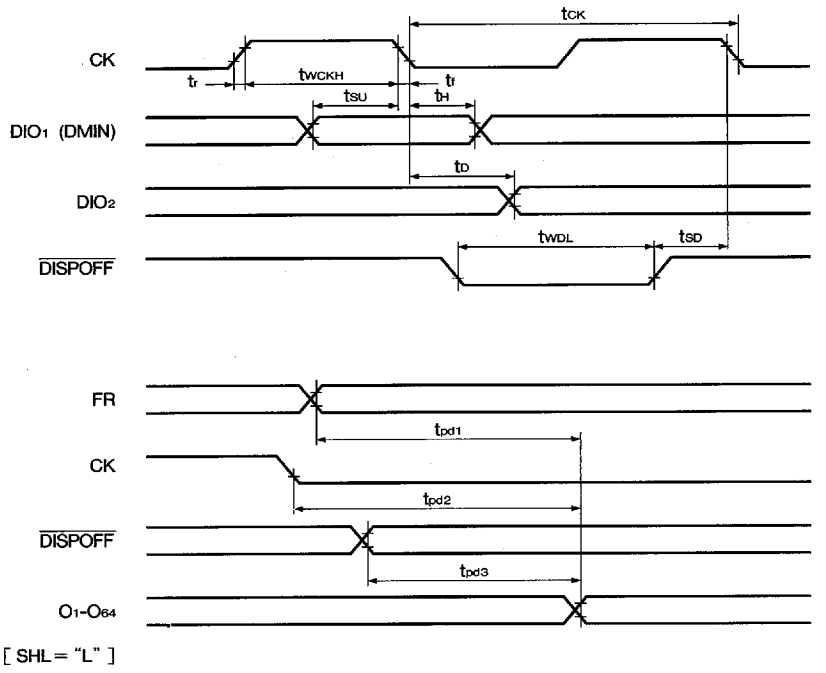
($V_{SS}=V_5=0$ V, $V_{DD}=+2.5$ to $+5.5$ V, $V_O=+10.0$ to $+30.0$ V, Ta $=-20$ to $+85$°C)

PARAMETER	SYMBOL	APPLICABE PINS	V_{DD}=2.5 to 4.5V		V_{DD}=4.5 to 5.5V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Shift clock period	t_{CK}	CK	2000		1000		ns
Shift clock "H" pulse width	t_{WCKH}		500		250		ns
Data setup time	t_{SU}	DIO_1 DIO_2	200		100		ns
Data hold time	t_H		200		100		ns
Input signal rise time	t_r	CK		40		20	ns
Input signal fall time	t_f			40		20	ns
$\overline{DISPOFF}$ removal time	t_{SD}	$\overline{DISPOFF}$	100		100		ns
$\overline{DISPOFF}$ "L" pulse width	t_{WDL}		1.2		1.2		μs
Output delay time (1) *	t_D	DIO_1, DIO_2		400		200	ns
Output delay time (2) *	t_{pd1}, t_{pd2}	O_1 - O_{64}		2.4		1.2	μs
Output delay time (3) *	t_{pd3}			2.4		1.2	μs

NOTE :

* Condition $C_L=15$ pF

TIMING DIAGRAMS



PIN FUNCTION

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin connects to +2.5 to +5.5V
V_{SS}	Ground pin connects to 0 V
V_{OR}, V_{OL} V_{1R}, V_{1L} V_{4R}, V_{4L} V_{5R}, V_{5L}	Power supply pin for LCD drive voltage bias. ● Normally, the bias voltage is used, that is set by a resistor divider. ● Ensure that voltages are set such that $V_{SS} \leq V_5 < V_4 < V_1 < V_0$. ● To further reduce the difference between the output waveforms of LCD drive output pins O_1 and O_{64}, externally connect V_{iR} and V_{iL} (i=0, 1, 4, 5).
DIO_1	Bidirectional shift register shift data input/output pin ● Input pin for right shift, output pin for left shift.
DIO_2	Bidirectional shift register shift data input/output pin ● Input pin for left shift, output pin for right shift.
CK	Bidirectional shift register shift clock pulse input pin ● Data is shifted on the falling edge of the clock pulse.
SHL	Bidirectional shift register shift direction selection pin ● Data is shifted right when set to V_{SS} level "L", and data is shifted left when set to V_{DD} level "H".
$\overline{DISPOFF}$	Control input pin for output deselect level ● The input signal is level-shifted internally from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. ● When set to V_{SS} level "L", the LCD drive output pins (O_1-O_{64}) are set to level V_5. ● While set to "L", the contents of the shift register are reset, and data reading is stopped. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_1 or V_4), and the shift data is read on the falling edge of the CK. At this time, if $\overline{DISPOFF}$ removal time (t_{SD}) can not keep regulation (shown in "AC CHARACTERISTICS"), the Shift data won't be read correctly.
FR	AC signal input for LCD drive waveform ● The input signal is level-shifted internally from logic voltage level to LCD drive voltage level, and controls LCD drive circuit. ● Normally, inputs a frame inversion signal. ● The LCD drive output pin's output voltage level can be set using the shift register output signal and the FR signal. For details, see "TRUTH TABLE".
MODE	Mode select pin ● When set V_{SS} level "L", Single Mode operation is selected, when set to V_{DD} level "H", Dual Mode operation is selected.
DMIN	Dual Mode data input pin ● According to the data shift direction of the data shift register, data can be input starting from the 33rd bit.
$TEST_1$ $TEST_2$	Test Mode select pin ● During normal operation, tie to V_{SS} level "L".
O_1-O_{64}	LCD drive output pins ● Corresponding directly to each bit of the shift register, one level (V_0, V_1, V_4, or V_5) is selected and output.

TRUTH TABLE

($V_{SS} \leq V_5 < V_4 < V_1 < V_O$)

FR	LATCH DATA	$\overline{DISPOFF}$	LCD DRIVE OUTPUT VOLTAGE LEVEL (O_1-O_{64})
L	L	H	V_4
L	H	H	V_O
H	L	H	V_1
H	H	H	V_5
X	X	L	V_5

NOTES :

- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care.
- "Don't care" should be fixed to "H" or "L", avoiding floating.
- There are two kinds of power supply (logic level voltage and LCD drive voltage) for LCD driver. Please supply regular voltage which assigned by specification for each power pin.

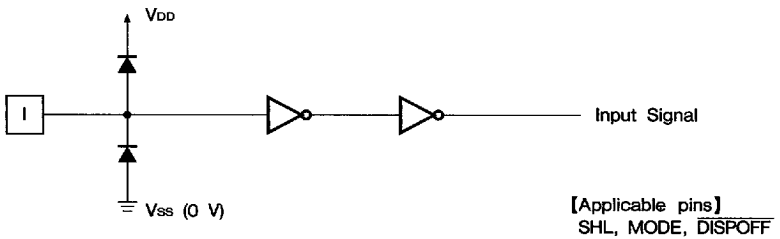
RELATIONSHIP BETWEEN THE DATA I/O PINS AND THE DATA TRANSFER DIRECTION

MODE	SHL	DIO_1	DIO_2	DMIN	DATA TRANSFER DIRECTION
L (Single)	L (shift to right)	Input	Output	X	$O_1 \rightarrow O_{64}$
	H (shift to left)	Output	Input	X	$O_{64} \rightarrow O_1$
H (Dual)	L (shift to right)	Input	Output	Input	$O_1 \rightarrow O_{32}$ $O_{33} \rightarrow O_{64}$
	H (shift to left)	Output	Input	Input	$O_{64} \rightarrow O_{33}$ $O_{32} \rightarrow O_1$

NOTES :

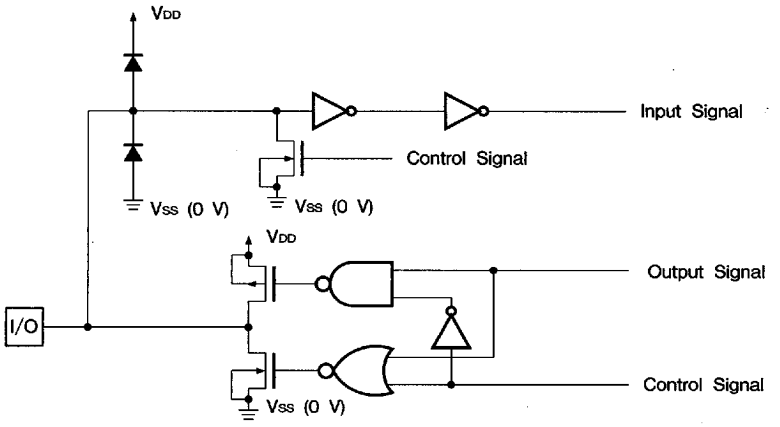
- L : V_{SS} (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care.
- "Don't care" should be fixed to "H" or "L", avoiding floating.

INPUT/OUTPUT CIRCUITS



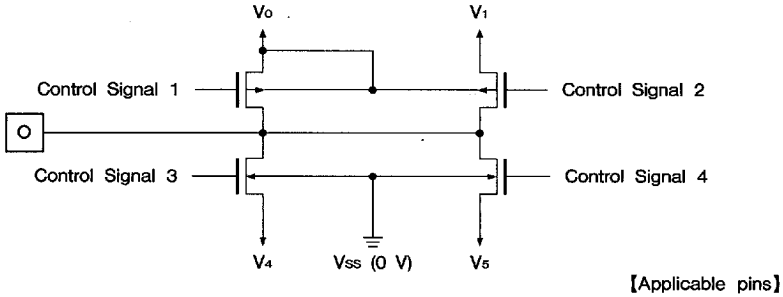
【Applicable pins】
SHL, MODE, $\overline{\text{DISPOFF}}$
FR, CK, DMIN

Fig. 1 Input Circuit



【Applicable pins】
DIO_1, DIO_2

Fig. 2 Input/Output Circuit



【Applicable pins】
O_1-O_{64}

Fig. 3 LCD Drive Output Circuit

CONNECTION EXAMPLES FOR PLURAL COMMON DRIVERS

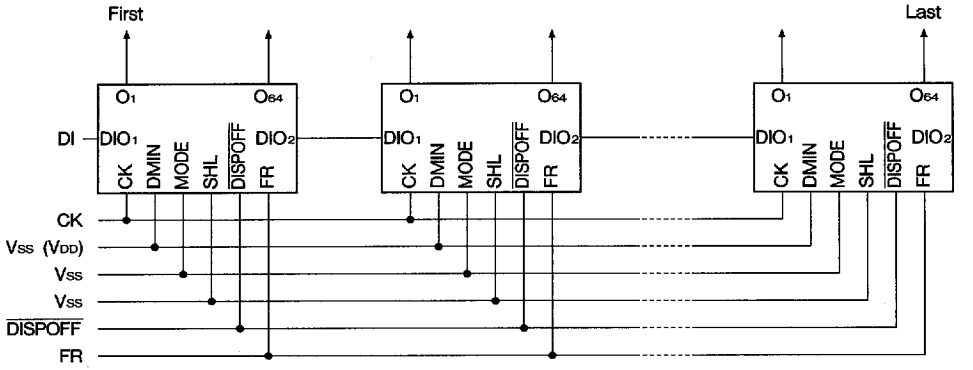


Fig. 4 Single Mode (Shifting toward right)

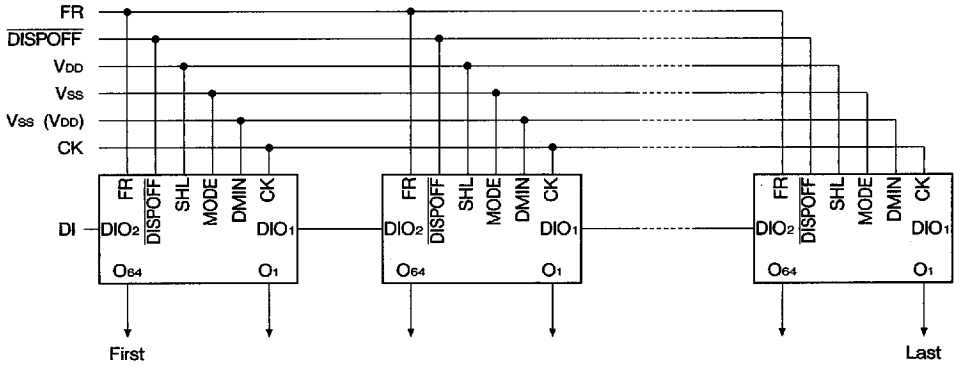


Fig. 5 Single Mode (Shifting toward left)

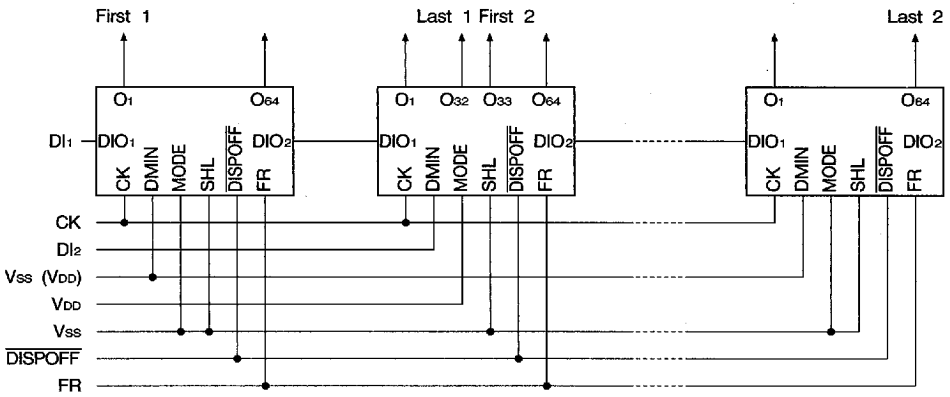


Fig. 6 Dual Mode (Shifting toward right)

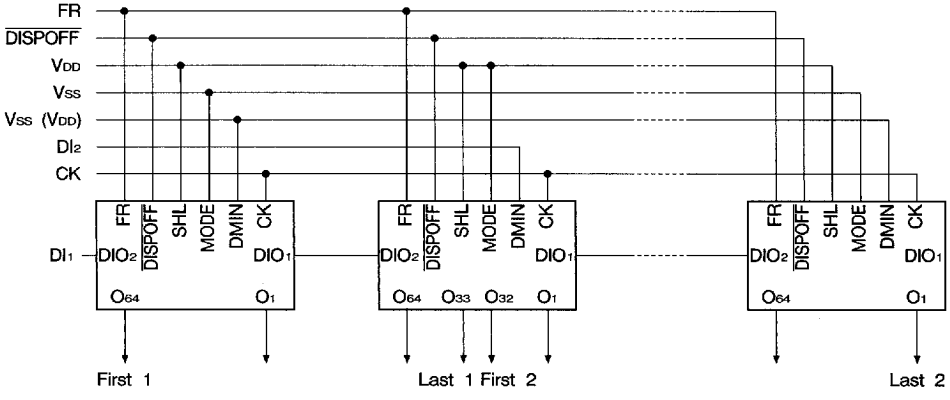


Fig. 7 Dual Mode (Shifting toward left)

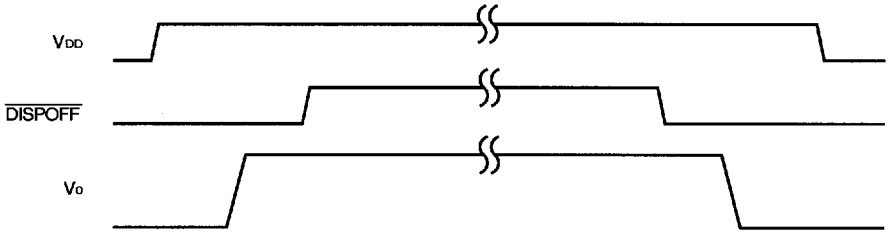
PRECAUTION

Precaution when connecting or disconnecting the power

This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power.
- We recommend you connecting the serial resistor (50 to 100 Ω) to the LCD drive power V_O of the system as a current limitter resistor. And set up the suitable value of the resistor in consideration of LCD grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore when connecting the logic power supply, connect the LCD drive power supply after resetting logic condition of this LSI inside on $\overline{DISPOFF}$ function. After that, cancel the $\overline{DISPOFF}$ function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power supply, set the LCD drive output pins to level V_5 on $\overline{DISPOFF}$ function. After that, disconnect the logic system power after disconnecting the LCD drive power. When connecting the power supply, show the following recommend sequence.



SYSTEM CONFIGURATION EXAMPLE