DATA SHEET

APPIAN TECHNOLOGY INC

POACH/ATF™

POACH 7/POACH 8

T-52-33-05

FEATURES

- fully IBM PC AT-compatible
- two chip set replaces the major logic functions of the IBM PC AT motherboard including the functions of all the microprocessor peripherals:
  - — 8259A Programmable Interrupt Controller (Master)
  - — 8259A Programmable Interrupt Controller (Slave)
  - — 8254 Programmable Interval Timer
  - — 8284A Clock Generator (Timer)
  - — 8284A Clock Generator (Coprocessor)
  - — 82284 Clock Generator & Ready Interface
  - — 82288 Bus Controller
  - — 8237 DMA Controller (Byte)
  - — 8237 DMA Controller (Word)
  - — 6818 Real Time Clock
  - — 74LS612 Memory Mapper
- includes:
  - — 10-bit Refresh Generation Logic
  - — Refresh/DMA Arbitration
  - — Address/Data Bus Control
  - — 16- to 8-bit Conversion Logic
- 16-MHz operation
- high integration 80286 design solution
- numerical processor control with independent 8284A for asynchronous coprocessor clock
- single +5V power supply
- low-power CHMOS-3
- microprocessor peripheral functions available as standard cells in the ZyMOS cell library for unique design integration
- generation of an early RAS signal
- support of multispeed systems through dynamic clock switching
- provides high system speed with provision for lower-speed expansion bus
- additional I/O command delay
- special PCB test mode
- DRAM on local data bus
- Schmitt inputs on POWERGOOD, REFRESH, IOCHRDY

DESCRIPTION

The ZyMOS POACH/ATF (PC On A CHip) chip set is a high performance two-chip implementation of LSI/MSI/SSI logic controlling the IBM Personal Computer AT. POACH/ATF operates at 16 MHz using cost-effective DRAMs. The devices provide a low-power, highly integrated PC AT design solution that may also be applied to any 80286-based system.

POACH 7 performs the functions of the 82284 Clock Generator and READY Interface, 82288 Bus Controller for 80286 processors, 6818 Real Time Clock/RAM, and the Master/Slave implementation of the dual 8259A Programmable Interrupt Controllers as well as Command Delay, Shut Down, Address/Data Bus Control and READY Generation logic and the 8284A Coprocessor Clock Generator. POACH 8 includes the 8254 Programmable Interval Timer, 8284A Clock Generator, LS612 Memory Mapper and the dual 8237 DMA Controller functions as well as Refresh Generation and Refresh/DMA Arbitration Logic.

POACH/ATF peripherals are fully compatible with those used in standard PC AT designs; the chip set is fully IBM PC AT-compatible. High-speed operation is possible by selecting the optimum RAM/buffer combination. Occupying only two 84-pin plastic leaded chip carriers on the AT motherboard, POACH/ATF implementation results in a dramatic reduction in board size.

FUNCTIONAL DESCRIPTION

POACH/ATF (POACH 7 and 8) has been developed to maximize the full performance capabilities of the basic PC AT system architecture. The high performance POACH 7 and 8 ICs are similar to POACH 1 and 2, and include features which support the development of systems operating above 12 MHz. The system enhancements available from POACH/ATF include:

1. Memory Path Timing Enhancements
2. Dynamic Processor Speed Switching
3. Additional Command Delays
4. Independent 80287 Clocking
5. POWERGOOD Signal Conditioning
6. Board Test Mode

Memory Path Timing Enhancements

To allow the use of slower, lower-cost memories in a high performance PC AT system, POACH 7 supports local data bus memory connections and provides an -ERAS control signal. The -ERAS (Early RAS) signal supports higher speed memory designs than +RAS of the standard PC AT.

The new -LMEM (local memory) input signal provided on POACH 7 supports direct connection of system board memory to the 80286 processor's local data bus. This feature also allows slower memories to be used by eliminating transceiver delays in the critical memory timing path. The -LMEM signal controls the outputs -DTR, -MOE, -LOE, and disables -ERAS to reduce system power consumption. When -LMEM is high, the signals -DTR, -MOE, and -LOE operate identically to their POACH 1 equivalents DT/R, MSDEN and LSDEN. When -LMEM is driven low, data transfer is directed to the local data bus via the -DTR, -MOE and -LOE controls during DMA and bus master operations.

Additional Command Delays

Another important feature available from POACH/ATF is the extra command delay added to the -IOR and -IOW signals. In a high performance system with a short clock cycle, there may not be enough command recovery time, or precharge time, to meet the peripheral IC or expansion card requirements even though the actual command time is sufficient. The standard PC AT design provides a command pulse width of 4½ PROCCLK cycles and a recovery time of 1½ cycles. POACH/ATF extends the command delay by an extra half cycle to increase the recovery time by 33%, while reducing the command pulse only 11%. The improved balance between command pulse and recovery time is important in a high speed system.

Dynamic Processor Speed Switching

POACH/ATF provides the ability to switch the system speed dynamically during normal operation via the -HSPEED input. The -HSPEED (high speed) input selects either the X3 or X5 input frequency. In a typical system, the X3 input clock is twice the frequency of the system speed: i.e., 32 MHz for a 16-MHz system. The X5 input clock is typically used to set the expansion bus operating speed and is also twice the required speed: i.e., 16 MHz for a 8-MHz expansion bus. When -HSPEED is high, the X5 input is selected. The frequency of PROCCLK will be equal to the frequency of either X3 or X5, depending on which one is selected. Note that for reliable operation both the X3 and X5 inputs must have a clock input source even if it is the same signal, and even if speed switching is not used.

Dynamic speed switching provides an important capability to high performance systems because some expansion cards cannot operate at speeds beyond the 8-MHz IBM PC AT standard. By detecting an I/O or expansion bus operation, the entire system speed can be slowed to the standard IBM PC AT speed, thereby allowing time for the peripheral or expansion card to respond. As a result, a

universal solution for interfacing with the wide variety of expansion cards is easily implemented with POACH/ATF. Using this feature, keyboard control of system speed can also be easily implemented where low-speed operation for real-time applications, such as games, is needed.

Independent 80287 Clocking

An 80287 coprocessor with a clock rate above 10 MHz is not commercially available, and as a result, the standard coprocessor clock connections of the PC AT will not function for systems faster than 10 MHz. POACH/ATF provides an 8284 clock generator for dedicated asynchronous operation of the coprocessor. This feature of POACH/ATF allows a coprocessor of any specific performance requirement to be included in the system. Maximizing performance of the coprocessor becomes independent of the system operating speed.

The output of an oscillator is connected to the OSC287 input of POACH/ATF. The frequency of this oscillator should be three times the 80287 coprocessor speed; a 30-MHz oscillator for a 10-MHz coprocessor. The 8284 of POACH/ATF produces a clock signal of the recommended 33% duty cycle on the CLK287 output. Note that the clock mode input (CKM) of the 80287 coprocessor must be connected to a high logic level for this POACH/ATF feature to work properly.

POWERGOOD Signal Conditioning

POACH/ATF uses an active-high POWERGOOD input signal. As a result, design flexibility for implementing a very low-power, low-voltage, 32-KHz oscillator circuit is improved since an external battery-powered inverter is not needed.

The input buffer of the POACH/ATF POWERGOOD signal is implemented as a Schmitt trigger. This feature provides additional operating margin, which is especially important for applications that do not have high-quality PC AT-type power supplies.

System Board Testing

To facilitate "bed-of-nails" board testing, a test mode has been added to POACH 7 that enables the switching of all outputs to a high-impedance state. As long as the maximum device limits are not exceeded, this allows a test system to overdrive the POACH 7 outputs without the concern of device degradation resulting from high currents and conflicting signal levels.

Data on the XD0 pin is sampled on the rising edge of the TEST input. If XD0 is sampled as a high logic level, this test mode is enabled. The test mode remains enabled until the TEST input returns to a low logic level. Note that a RESET following TEST mode exit may be needed before normal POACH 7 operation can begin since random test vectors on POACH 7 inputs may latch an erroneous internal condition.

The TEST input of POACH 7 must be connected to an external 10KΩ pulldown resistor if this feature is to be used. If this test mode is not to be used, the TEST input must be tied to ground.

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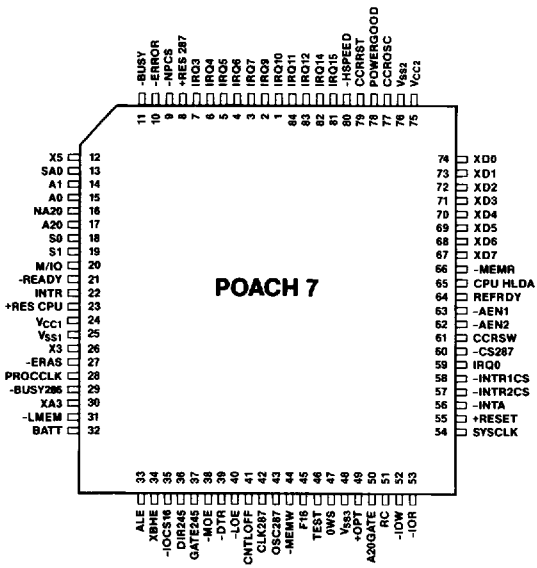
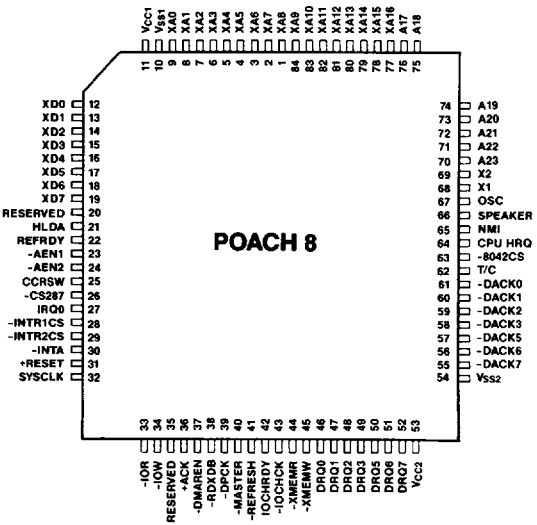


Pin Diagram POACH 7



Pin Diagram POACH 8

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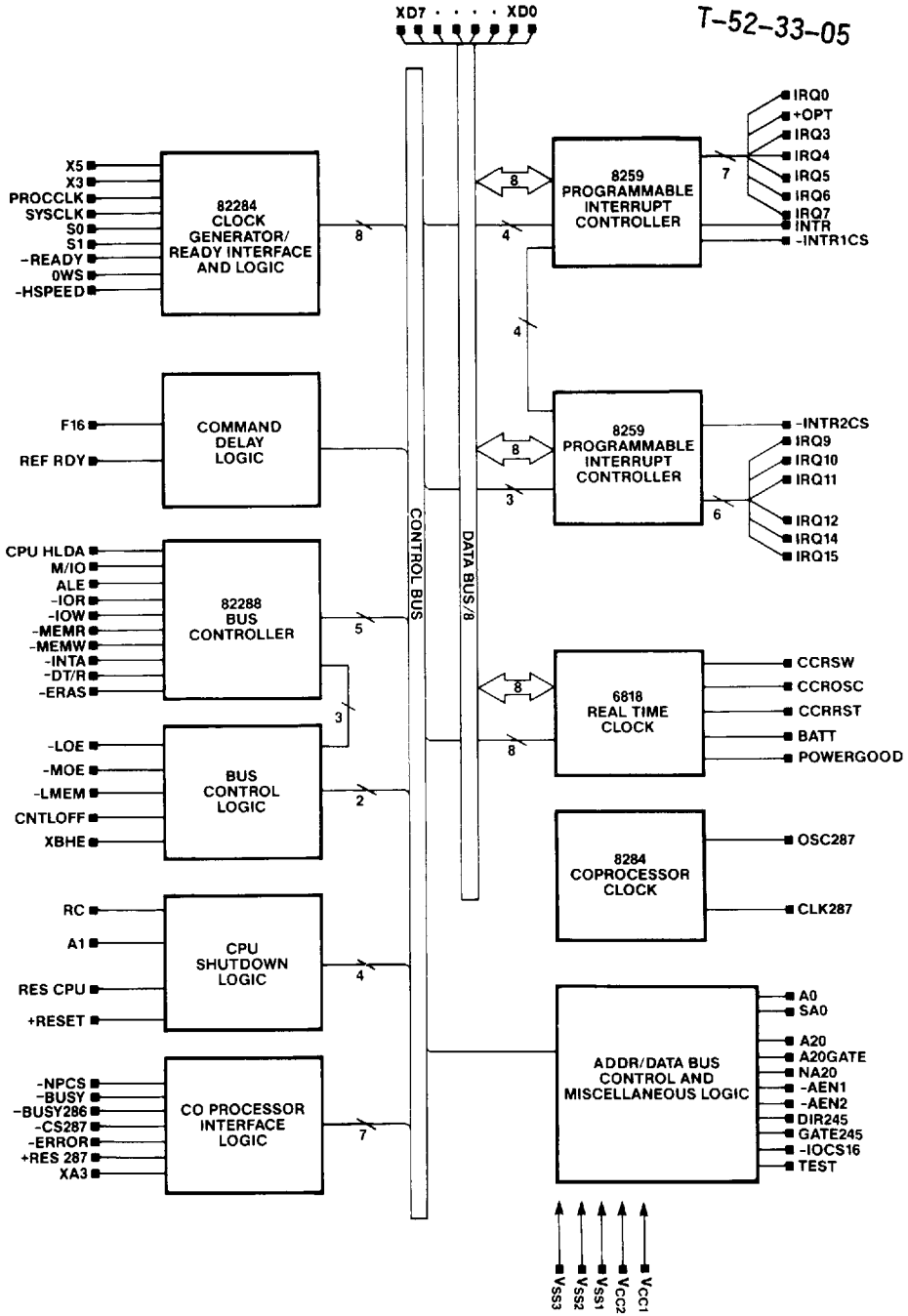
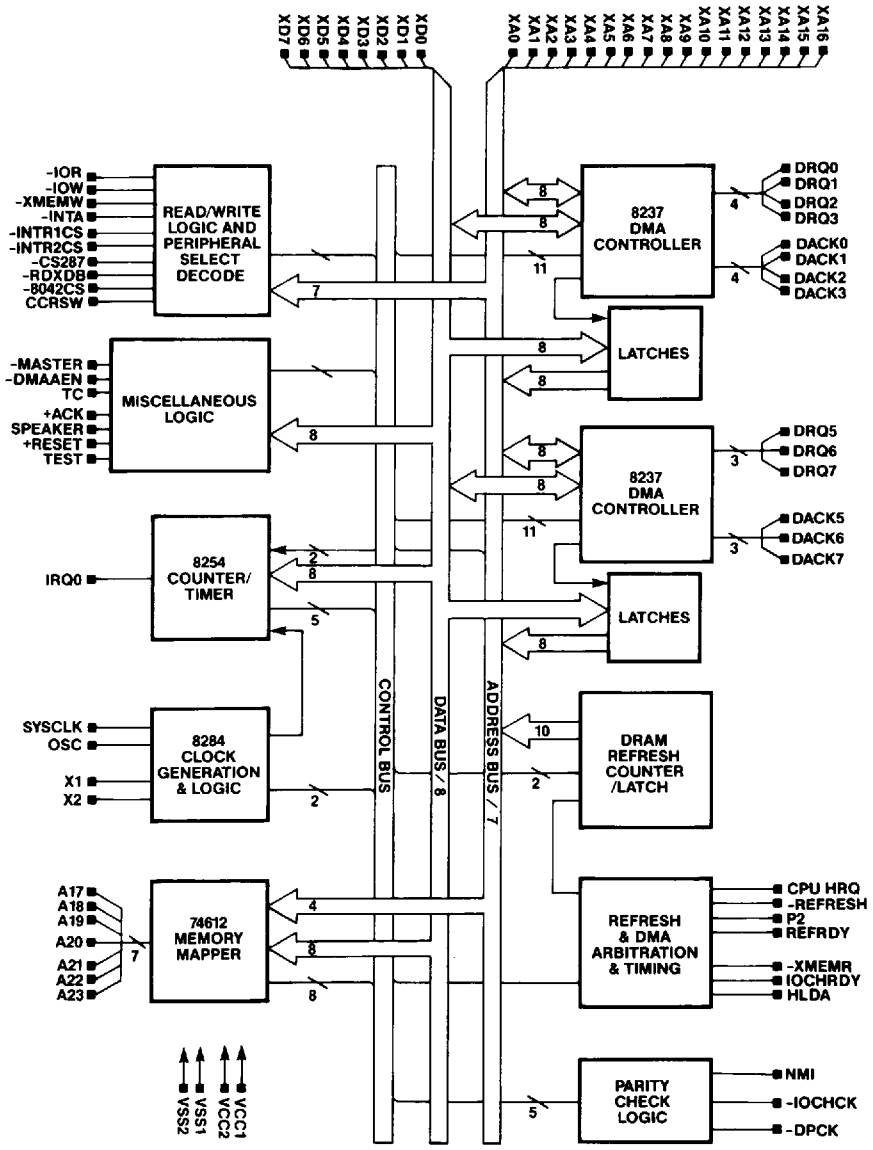
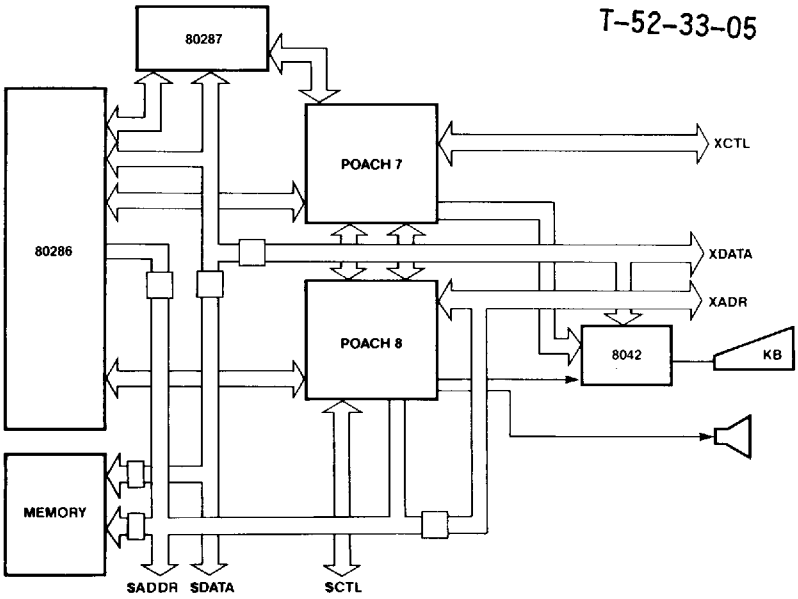


POACH 7—Block Diagram



POACH 8—Block Diagram



Block Diagram of POACH 7 and POACH 8 for PC AT

POACH 7 Pin Description T-52-33-05

Pin No.	Symbol	Type	Description
15	A0	I	ADDRESS 0 input from the CPU. It is used to generate SA0.
14	A1	I	ADDRESS 1 input from the CPU. It is used in conjunction with M/IO, S0 and S1 to detect a CPU shutdown condition.
17	A20	O	ADDRESS 20 is the A20 (NA20) line from the CPU after conditioning by the A20GATE signal.
50	A20GATE	I	A20GATE from the keyboard controller is used to force A20 low. When A20GATE is low, A20 on the CPU address bus is forced low. When A20GATE is high, A20 follows the CPU address 20. Tie directly to the P21 pin of the keyboard controller.
62 63	-AEN2 -AEN1	I	ADDRESS ENABLE 1 & 2 from DMAs 1 & 2, respectively. Each signal is the result of the DMAAEN pin NAND'd with -MASTER. Tie directly from the -AEN1 and -AEN2 pins of POACH 8.
33	ALE	O	ADDRESS LATCH ENABLE is an active high signal that controls the address latches used to hold addresses during bus cycles. ALE is held inactive for halt bus cycles.
32	BATT	I	BATTERY power to the clock calendar and RAM.
29	-BUSY286	O	-BUSY286 is an active low output indicating the operating condition of the 80287 coprocessor to the processor. It is normally tied to the processor BUSY pin.
11	-BUSY	I	-BUSY is an active low input from the 80287 to indicate that it is currently executing a command. It is used to generate the -BUSY286 output signal.
77	CCROSC	I	CLOCK CALENDAR RAM OSCILLATOR.
79	CCRRST	I	CLOCK CALENDAR RAM RESET signal for the Real Time Clock. This is an active low input.
61	CCRSW	I	CLOCK CALENDAR RAM Select signal for the real-time clock. A high enables READ/WRITE operation to the real-time clock. Tie directly to the CCRSW pin of POACH 8.
42	CLK287	O	CLOCK 80287 is a 33% duty cycle clock output with frequency of OSC287 divided by 3, used as the 80287 fundamental clock frequency.
41	CNTLOFF	O	CONTROL OFF is used to enable the low byte data bus latch during byte accesses. This signal is active high.

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POACH 7 Pin Description (Continued)

Pin No.	Symbol	Type	Description
65	CPU HLDA	I	CPU HOLD ACKNOWLEDGE is an active high input from the processor. An active condition indicates that the CPU has relinquished the bus to another bus master in the system.
60	-CS287	I	CHIP SELECT 287 is used to derive the -NPCS signal. Tie directly to the -CS287 pin of POACH 8.
36	DIR245	O	DIRECTION-245 controls the high-to-low byte and low-to-high byte conversion during data transfers to and from 8-bit peripherals.
39	-DTR	O	DATA TRANSMIT/RECEIVE establishes the data direction to and from the local data bus. When high, this output signals a CPU write bus cycle to the memory DATA bus or a DMA read bus cycle from the local DATA bus. A low indicates a CPU read bus cycle from the memory DATA bus or the DMA write bus cycle to the local DATA bus. This signal is conditioned by -LRAM. This signal is high when no bus cycle is active.
27	-ERAS	O	EARLY ROW ADDRESS STROBE is the RAS signal for DRAM. This is an active low output signal conditioned by -LRAM.
10	-ERROR	I	ERROR is an active low input from the numeric processor indicating that an unmasked error condition exists. Tie directly to the -ERROR pin of the 80287.
45	F16	I	F16 is an active high input indicating a word memory access. It is used to inhibit command delays for memory accesses.
37	GATE245	O	GATE245 is an active low output. When active it enables the bus transceiver that performs the high-to-low byte conversion with the DIR245 signal. Conversion does not take place if A0 = 0 which indicates a word transfer.
80	-HSPEED	I	-HSPEED is an active low input. When -HSPEED is low, PROCCLK has the same frequency as the X3 input clock. When -HSPEED is high, PROCCLK is the frequency of the X5 input clock.
56	-INTA	O	INTERRUPT ACKNOWLEDGE instructs an interrupting device that its interrupt request is being acknowledged. This output signal is active low. -INTA is tri-stated when CPU HLDA is high and CNTLOFF is low. Tie directly to the -INTA pin of POACH 8.

POACH 7 Pin Description (Continued) T-52-33-05

Pin No.	Symbol	Type	Description
22	INTR	O	INTERRUPT REQUEST is connected directly to the CPU's interrupt pin. INTR is active high, and is generated when a valid interrupt request has been asserted.
58	-INTR1CS	I	INTERRUPT CONTROLLER 1 (MASTER) CHIP SELECT is an active low input that is used to select the interrupt controller as an I/O device. This allows communication between the master interrupt controller and the CPU via the 'X' Data Bus. Tie directly to the -INTR1CS pin of POACH 8.
57	-INTR2CS	I	INTERRUPT CONTROLLER 2 (SLAVE) CHIP SELECT is an active low input that is used to select the interrupt controller as an I/O device. This allows communication between the slave interrupt controller and the CPU via the 'X' data bus. Tie directly to the -INTR2CS pin of POACH 8.
35	-IOCS16	I	I/O 16-BIT CHIP SELECT signals the system that the current data transfer is a 16-bit, one wait-state, I/O cycle. It is derived from an address decode and is an active low signal.
53	-IOR	O	I/O READ instructs a selected I/O device to drive its data onto the data bus. The -IOR signal is active low. It is tri-stated when CPU HLDA is high and CNTLOFF is low.
52	-IOW	O	I/O WRITE instructs a selected I/O device to read the data on the data bus. The -IOW signal is active low. It is tri-stated when CPU HLDA is high and CNTLOFF is low.
59	IRQ0	I	INTERRUPT REQUEST 0 (system timer) receives interrupt requests from channel 0 of the timer/counter. Tie directly to the IRQ0 pin of POACH 8.
3-7 1-2 83-84 81-82	IRQ7-IRQ3 IRQ10-IRQ9 IRQ12-IRQ11 IRQ15-IRQ14	I I I I	INTERRUPT REQUESTS 3-7, 9-12, and 14-15 are used to signal the CPU that an I/O device needs attention. The interrupt requests are prioritized with IRQ9-IRQ12; IRQ14-IRQ15 having the highest priority (IRQ9 highest) and IRQ3-IRQ7 having the lowest priority (IRQ7 lowest). IRQn signals are active high. The requesting signal is held high until the CPU acknowledges the interrupt request.
40	-LOE	O	LEAST SIGNIFICANT DATA ENABLE is an active low output. When active, it enables the transceiver/receiver connected to the least significant byte of the local data bus. This signal is conditioned by -LRAM.

POACH 7 Pin Description (Continued)

Pin No.	Symbol	Type	Description
31	-LMEM	I	This active low input signal indicates a memory transaction with the local DATA bus.
66	-MEMR	I/O	MEMORY READ COMMAND instructs a memory device to drive data onto the data bus. This signal is active low. -MEMR is active on all memory read cycles. It is tri-stated when CPU HLDA is high and CNTLOFF output is low.
44	-MEMW	I/O	MEMORY WRITE COMMAND instructs a memory device to read the data on the data bus. This signal is active low. -MEMW is active on all memory write cycles. It is tri-stated when CPU HLDA is high and CNTLOFF output is low.
38	-MOE	O	MOST SIGNIFICANT DATA ENABLE is an active low output. When active, it enables the transceiver connected to the most significant byte of the local data bus. This signal is conditioned by -LRAM.
20	M/$\overline{IO}$	I	MEMORY-$\overline{INPUT\ OUTPUT}$ is the M/$\overline{IO}$ signal from the CPU. When high, it indicates a memory access. When low, it indicates an I/O access. It is used to generate the memory and I/O signals for the system.
16	NA20	I	NA20 is the CPU address 20. POACH 7 conditions this signal with A20GATE to produce A20. This pin is tied directly to the CPU A20 output.
9	-NPCS	O	NUMERICAL PROCESSOR CHIP SELECT is an active low output used to select the 80287 numerical processor. It is tied directly to the NPS1 pin of the 80287.
49	+OPT	I	KEYBOARD OUTPUT BUFFER FULL is an active high signal from the keyboard controller P24 pin. The signal is an interrupt request (IRQ1) signaling a full keyboard buffer.
47	0WS	I	ZERO WAIT STATE option. When pulled active (low), the current processor cycle can be terminated.
43	OSC287	I	OSCILLATOR 80287 is the clock input for the co-processor clock generator.
28	PROCCLK	O	PROCESSOR CLOCK provides the clock signal for the CPU. Tie directly to the CLK pins of the 80286.
78	POWER-GOOD	I	POWERGOOD is an active high input that indicates that system power is sufficient to maintain the integrity of the system. A low-to-high transition will initiate a system reset.

POACH 7 Pin Description (Continued) T-52-33-05

Pin No.	Symbol	Type	Description
51	RC	I	RESET CPU from the keyboard controller P21 pin.
21	-READY	O	READY is an active low output that signals when the current bus cycle is to be completed. S0, S1, +POWER GOOD, and 0WS control the -READY output.
64	REFRDY	I	REFRESH/IO-CHANNEL-READY is generated by POACH 8. It is used to preset the READY Interface Asynchronous READY (ARDY).
8	+RES 287	O	RESET 80287 is the reset signal for the 80287 numerical processor.
23	RES CPU	O	RESET CPU is the reset signal for the CPU. Active high, RESCPU is generated when either +POWERGOOD or RC become active, or when the CPU generates a HALT status by forcing M/IO high, S0, S1 and A1 low. If this signal is initiated by RC, or by M/IO, S0, S1 and A1, it will remain active for 16 PROCCLK cycles.
55	+RESET	O	RESET (SYSTEM) is an active high output derived from the POWER GOOD input. +RESET is used to force the system into an initial state. When +RESET is active, -READY will also be active (low).
18, 19	S0, S1	I	STATUS inputs from the CPU. The status signals are used by the bus controller to determine the state of the CPU.
13	SA0	I/O	ADDRESS 0 of the CPU bus. SA0 outputs A0 from the CPU during local CPU cycles. The expansion bus can also force this pin when another master on the expansion bus has control. During an interrupt acknowledge this signal will be forced low. This signal becomes an input during non-CPU bus cycles.
54	SYSCLK	O	SYSTEM CLOCK is the result of PROCCLK divided by two, thus synchronized to the processor's T-states. It may be used to clock peripheral devices that must be synchronized to the CPU.
46	TEST	I	TEST is an input which enables test modes. It should be connected to VSS through 10KΩ resistor.
24 75	Vcc1 Vcc2		POWER: +5-Volt supply.
25 76 48	Vss1 Vss2 Vss3		GROUND.

POACH 7 Pin Description (Continued)

Pin No.	Symbol	Type	Description
26	X3	I	X3 is the clock input used to generate PROCCLK and SYSCLK. It is selected when the -HSPEED input is low.
12	X5	I	X5 is the clock input used to generate PROCCLK and SYSCLK. It is selected when the -HSPEED input is high.
30	XA3	I	ADDRESS 3 is used for generating the chip select and reset signals for the 80287.
34	XBHE	I/O	BUS HIGH ENABLE is an active low signal used by POACH 7 to generate the -MOE signal.
67-74	XD7-XD0	I/O	Data Bus 0-7 for the peripheral bus. The direction of the bus is determined by the RDXDB signal from POACH 8. It is used by the 8259A to decipher command words the CPU issues.

POACH 8 Pin Description

63	-8042CS	O	8042 CHIP SELECT is an active low, chip select signal for the keyboard controller.
70-76	A23-A17	O	A23-A17 are the address bits 17-23 of the CPU address bus. They are outputs directly from the memory mapper pins MO1-MO7 and supply page information during DMA transfers.
36	+ACK	O	ACKNOWLEDGE is an active low output. When active it enables the bus transceiver between the system and peripheral (XBUS) bus. +ACK is used in conjunction with -RDXDB, which controls the direction of the bus transceiver.
23 24	-AEN1 -AEN2	O O	ADDRESS ENABLE FROM DMAs 1 & 2, respectively. The signal is the result of the DMA's AEN signal NAND'd with -MASTER. Tie directly to the -AEN1 and -AEN2 pins of POACH 7.
25	CCRSW	O	CLOCK CALENDAR RAM Select signal for the real-time clock. A high enables READ/WRITE operations to the real-time clock. Tie directly to the CCRSW pin of POACH 7.
64	CPU HRQ	O	CPU HOLD REQUEST is an active high output indicating a DMA request to the CPU. It is also active during refresh cycles. CPU HRQ is normally connected to the 80286 HOLD pin.
26	-CS287	O	CHIP SELECT 287 is used by POACH 7 to derive the -NPCS signal. Tie directly to the -CS287 pin of POACH 7.

POACH 8 Pin Description (Continued) T-52-33-05

Pin No.	Symbol	Type	Description
61-58 57-55	-DACK0-3 -DACK5-7	O O	DMA ACKNOWLEDGE 0-3 and 5-7 are used to acknowledge DMA requests (DRQ0-3 & 5-7). The output signal is an active low.
37	-DMAAEN	O	DMA ADDRESS ENABLE is an active low signal and is active when an I/O device is making a DMA access to system memory or during refresh.
39	-DPCK	I	DATA PARITY CHECK is used to generate NMI. This input is active low.
46-49 50-52	DRQ0-3 DRQ5-7	I I	DMA REQUEST 0-3 & 5-7 are synchronous channel requests used by peripheral devices and I/O processors to gain DMA service. The requests are prioritized with DRQ0 having the highest and DRQ7 having the lowest priorities. A DRQ line must be held active (high) until the corresponding DACK line goes active.
21	HLDA	I	HOLD ACKNOWLEDGE is an active high input that is equivalent to CPU HLDA. An active condition indicates that the CPU has relinquished the bus to another bus master in the system.
30	-INTA	I	INTERRUPT ACKNOWLEDGE instructs an interrupting device that its interrupt is being acknowledged, and the device may place its interrupt vector onto the data bus.This input signal is active low. -INTA is used by POACH 8 in the generation of -RDXDB. From POACH 7 pin 56.
28	-INTR1CS	O	INTERRUPT CONTROLLER 1 (MASTER) CHIP SELECT is an active low output that is used by POACH 7 to select the interrupt controller as an I/O device. This allows communication between the master interrupt controller and the CPU via the 'X' data bus. Tie directly to the -INTR1CS pin of POACH 7.
29	-INTR2CS	O	INTERRUPT CONTROLLER 2 (SLAVE) CHIP SELECT is an active low output that is used by POACH 7 to select the interrupt controller as an I/O device. This allows communication between the slave interrupt controller and the CPU via the 'X' data bus. Tie directly to the -INTR2CS pin of POACH 7.
43	-IOCHCK	I	I/O CHANNEL CHECK is an active low input. It is used to indicate an uncorrectable system error. Usually provides the system with parity error information about memory or devices on the I/O channel.

POACH 8 Pin Description (Continued) T-52-33-05

Pin No.	Symbol	Type	Description
42	IOCHRDY	I	I/O CHANNEL READY is generated by an I/O device. When low it indicates a 'not ready' condition and forces the insertion of wait states in I/O or memory accesses by the I/O device. When active (high), it will allow the completion of a memory or an I/O access by the I/O device.
33	-IOR	I/O	I/O READ signal instructs a selected I/O device to drive its data onto the data bus. The -IOR signal is active low. It is used for data transfers between the CPU and by DMA transfers.
34	-IOW	I/O	I/O WRITE signal instructs a selected I/O device to read the data on the data bus. The -IOW signal is active low. It is used for data transfers between the CPU and by DMA transfers.
27	IRQ0	O	INTERRUPT REQUEST 0 (system timer) from channel 0 of the timer/counter. Tie directly to the IRQ0 pin of POACH 7.
40	-MASTER	I	-MASTER is an active low input used in conjunction with a DRQ line to gain control of the system. A DMA controller or processor on the I/O channel may issue a DRQ to a DMA channel and receive a -DACK. The I/O processor may then activate -MASTER, which allows it to control the system address, data, and control lines.
65	NMI	O	NON-MASKABLE INTERRUPT is an active high output that is connected to the CPU NMI pin.
67	OSC	O	OSCILLATOR output is the clock frequency of the crystal connected across X1-X2. It is the OSC output from the clock generator.
20 35	Reserved Reserved		Do not connect.
38	-RDXDB	O	READ X-DATA BUS controls the direction of the bidirectional buffer between the least significant byte of the 'S' data bus and the 'X' data bus. -RDXDB is used in conjunction with +ACK to control XBUS activity. When +ACK is active and -RDXDB is low, data is to be read from the peripheral bus. When +ACK is active and -RDXDB is high, data is to be written to the peripheral bus.

POACH 8 Pin Description (Continued) T-52-33-05

Pin No.	Symbol	Type	Description
22	REFRDY	O	REFRESH/IO-CHANNEL-READY is generated by +REFRESH OR'd with IOCHRDY. It is used by POACH 7 to preset the clock generator & ready interface asynchronous ready (ARDY).
41	-REFRESH	I/O	REFRESH is an active low output used to initiate a refresh cycle for the dynamic RAMs.
31	+RESET	I	RESET (SYSTEM) is an active high input from POACH 7. +RESET is used to force POACH 8, as well as the system, into an initial state. From POACH 7 pin 55.
66	SPEAKER	O	SPEAKER DATA is an output of the programmable interval timer tone signal used to drive the speaker.
32	SYSCLK	I	SYSTEM CLOCK input from POACH 7. It is used to synchronize POACH 8 to the system. From POACH 7 SYSCLK pin.
62	T/C	O	TERMINAL COUNT provides a pulse when the terminal count for any DMA channel is reached.
11 53	Vcc1 Vcc2		POWER: +5-volt supply.
10 54	Vss1 Vss2		GROUND.
68 69	X1 X2	I O	CRYSTAL connections for the internal oscillator used to generate clocking for I/O devices. A parallel resonant fundamental frequency mode crystal is required. An alternative CMOS clock may be connected to X1 (pin 68).
1-9 84 77-83	XA8-XA0 XA9 XA16-XA10	I/O I/O O	XBUS ADDRESSES 0-16 are the peripheral addresses for the local I/O bus.
12-19	XD0-XD7	I/O	Data Bus 0-7 for the peripheral bus. The direction of the bus is determined by the -RDXDB signal from POACH 8.
44	-XMEMR	I/O	MEMORY READ signal indicating a DMA read operation from peripheral devices or memory.
45	-XMEMW	O	MEMORY WRITE signal indicating a DMA write operation to peripheral devices or memory.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -65°C to 150°C
Voltage on any pin with respect to ground ..... -0.5V to V_{CC} + 0.5V
Maximum V_{CC} Voltage with respect to Ground ..... 6.0 V
Power Dissipation ..... 1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

POACH/ATF DC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Condition	Value			Units	Notes
			Min	Typ	Max		
INPUTS							
V_{IL1}	Input Low Voltage				0.5	V	1
V_{IH1}	Input High Voltage		2.0			V	1
V_{IL2}	Special Input Low Voltage				0.5	V	2
V_{IH2}	Special Input High Voltage		4.5			V	2
I_{IL1}	Input Low Current	V_{IN} = 0V	-100			μA	3
I_{IL2}	Special Input Low Current	V_{IN} = 0V	-10			μA	4
I_{IH}	Input High Current	V_{IN} = V_{CC}			10	μA	
OUTPUTS							
I_{OL1}	Output Low Current	V_{OL} = 0.45V	4	20		mA	5
I_{OL2}	Output Low Current	V_{OL} = 0.45V	24	35		mA	6
I_{OL3}	Open Drain Output Low Current	V_{OL} = 0.45V	24	36		mA	7
I_{OH}	Output High Current	V_{OH} = 2.4V		-20	-4	mA	8
I_{OZ}	Off State Current	V_O = 0 to V_{CC}	-10		10	μA	9

POACH/ATF DC CHARACTERISTICS (Continued)

T-52-33-05

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Condition	Value			Units	Notes
			Min	Typ	Max		
INPUTS							
I_{CC7}	POACH 7 Operating Supply Current	f_{SYSCLK} = 12.5MHz f_{SYSCLK} = 16MHz		28 32	55 60	mA mA	10
I_{STAT7}	POACH 7 Static Supply Current			60		µA	11
I_{BATT}	POACH 7 Battery Supply Current	V_{BATT} = 5V V_{BATT} = 2.8V		10	25 20	µA µA	12
V_{BATT}	POACH 7 Battery Supply Voltage		2.8			V	12
I_{CC8}	POACH 8 Operating Supply Current	f_{SYSCLK} = 12.5MHz f_{SYSCLK} = 16MHz		26 30	45 50	mA mA	13

Notes:

1. Includes all inputs, and I/O pin inputs except for POACH 7 pins POWERGOOD, X3, X5, CCRRST, CCROSC and POACH 8 pins X1, IOCHRDY and -REFRESH.
2. Special input pins include the crystal input pins and inputs needed for battery backup. On POACH 7 these signals are POWERGOOD, X3, X5, CCRRST and CCROSC. On POACH 8 they are signals X1, IOCHRDY and -REFRESH. Note that CCROSC is the only signal that should switch in the battery back up mode. For backup operation with $V_{BATT} < 4.75V$ CCROSC input levels V_{IL}/V_{IH} should be 10% and 90% of V_{BATT}, respectively.
3. All input pins include a high impedance pullup with the static protection network except for the special inputs POWERGOOD, X3, CCROSC, CCRRST and X1. I/O pins do not have this pullup.
4. Includes pin POWERGOOD, X3, CCROSC and CCRRST of POACH 7; and X1 of POACH 8.
5. Includes all outputs, and I/O pin outputs except for POACH 7 pins PROCCLK, SYSCLK, -IOR, -IOW, -MEMR, -MEMW, INTA, ALE, SA0, and POACH 8 pins -IOR, -IOW, OSC and -REFRESH.
6. Includes outputs PROCCLK, SYSCLK, -IOR, -IOW, -MEMR, -MEMW, INTA, ALE, SA0 of POACH 7 and -IOR, -IOW and OSC of POACH 8.
7. For the -REFRESH output of POACH 8.
8. Includes all outputs and I/O pin outputs except for -REFRESH of POACH 8.
9. For all 3-state and I/O pin outputs.
10. Includes I_{BATT} current with $V_{BATT} = V_{CC}$, and f_{CCROSC} = 32.768 KHz.
11. Inputs not switching at $V_{IN} = V_{CC}$, except f_{CCROSC} = 32.768 KHz. Includes I_{BATT} current with $V_{BATT} = V_{CC}$.
12. Tested with CCROSC input toggling at 32.768 KHz and CCRRST = V_{BATT}, all other inputs and V_{CC} supply pins open.
13. Tested with input X1 switching at 14.3181 MHz.

POACH 7 AC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_A = 0° C to 70° C)

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Symbol -Figure	Parameter	12.5 MHz			16 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
53-15	0WS Setup Time to PROCCLK↓	25	22		15			ns	
54-15	0WS Hold Time from PROCCLK↓	0	0		0			ns	
69-22	A0 Setup Time to ALE	25	11		15			ns	
	A0 Hold Time from ALE	0	0		0			ns	
26-6	A1 Setup Time to S1, S0	22	10		15			ns	
27-6	A1 Hold Time from S1, S0	0	0		0			ns	
43-13	A20 Delay from NA20		14	22			20	ns	
44-13	A20 Delay from A20GATE		24	32			31	ns	
45-13	A20 Disable Delay from CPUHLDA↑			30			30	ns	4
46-13	A20 Enable Delay from CPUHLDA↓			30			30	ns	
72-24	-AEN1, -AEN2 Setup Time to SYSCLK↓		15			15		ns	
73-24	-AEN1, -AEN2 Hold Time from SYSCLK↓		0			0		ns	
17-15	ALE Active Delay from PROCCLK↓		16	23			20	ns	
18-15	ALE Inactive Delay from PROCCLK↓		15	25			22	ns	
68-21	-BUSY286 Delay		20	35			31	ns	
	CCROSC High Time	15			15			μs	5
	CCROSC Low Time	15			15			μs	5
	CCROSC Input Rise/Fall Time			20			20	ns	
39-10,11	CCRR/W Setup Time to IOR/IOW↓		0			0		ns	
40-10,11	CCRR/W Hold Time from IOR/IOW↑		15			15		ns	
	CCRRST Pulse Width	83			62			ns	
12-3	CLK287 Delay from OSC287↑			35			35	ns	
67-20	CNTLOFF Delay from PROCCLK↓		17	25			20	ns	
70-23	CPUHLDA Setup Time to PROCCLK↓		18			15		ns	
71-23	CPUHLDA Hold Time from PROCCLK↓		0			0		ns	
47-14	DIR245 Delay from -IOR, -IOW		6	15			15	ns	
49-14	DIR245 Delay from -MEMR, -MEMW		6	15			15	ns	
	DIR245 delay from -AEN1, -AEN2			35			35	ns	

POACH 7 AC CHARACTERISTICS (Continued) T-52-33-05
(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	12.5 MHz Min	12.5 MHz Typ	12.5 MHz Max	16 MHz Min	16 MHz Typ	16 MHz Max	Units	Notes
55-16	-DTR Delay High from PROCCLK↓		29	40			35	ns	
56-16	-DTR Delay Low from PROCCLK↓		22	40			35		
13-15	-ERAS Active Delay from PROCCLK↓			40			30	ns	
14-15	-ERAS Inactive Delay from PROCCLK			40			30	ns	
60-16	F16 Setup Time to PROCCLK↓	30	12		20			ns	
61-16	F16 Hold Time from PROCCLK↓	0	-10		0			ns	
48-14	GATE245 Delay from -IOR, -IOW		11	20			20	ns	
50-14	GATE245 Delay from -MEMR, -MEMW		11	20			20	ns	
85-26,27	-HSPEED Setup Time to PROCCLK↓	15			15			ns	
86-26,27	-HSPEED Hold Time to PROCCLK↓	5			5			ns	
37-9	Interrupt Request Pulse Width	100			100			ns	8
29-7,8	-IOR, -IOW active delay from PROCCLK↓			35			30	ns	
30-7,8	-IOR, -IOW inactive delay from PROCCLK↓			35			30	ns	
	-IOR, -IOW enable/disable delay from CPUHLDA		35			30		ns	
	-INTA active delay from PROCCLK↓			35			30	ns	
	-INTA inactive delay from PROCCLK↓			35			30	ns	
	-INTA enable/disable delay from CPUHLDA		35			30		ns	
38-9	INTR Delay from Interrupt		67	150			125	ns	
33-7,8	-INTR1CS, -INTR2CS Setup Time to -IOR, -IOW↓		0			0		ns	
34-7,8	-INTR1CS, -INTR2CS Hold Time from -IOR, -IOW↑		0			0		ns	
72-24	-IO CS 16 Setup Time to SYSCLK↓	75			62			ns	
73-24	-IO CS 16 Hold Time from SYSCLK↓	0			0			ns	
57-16	-LOE, -MOE Active Delay from PROCCLK↓		23	40			30	ns	
58-16	-LOE, -MOE Inactive Delay from PROCCLK↓		20	30			30	ns	
66-19	-LOE, -MOE Delay from -NPCS		10			10		ns	

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POACH 7 AC CHARACTERISTICS (Continued) T-52-33-05

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	12.5 MHz			16 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
77-15	-LMEM Setup to PROCCLK↓	40				40		ns	
78-15	-LMEM Hold from PROCCLK↑	5				5		ns	
79-16	-MEMR, -MEMW Active Delay from PROCCLK↓	5		35			30	ns	
80-16	-MEMR, -MEMW Inactive Delay from PROCCLK↓	5		35			30	ns	
	-MEMR, -MEMW Enable/Disable Delay from CPUHLDA		35			30		ns	
64-17	MSDEN Delay from XHBE		16	25			25	ns	
62-16	M/$\overline{IO}$ Setup Time to PROCCLK↓	25	17		25	17		ns	
63-16	M/$\overline{IO}$ Hold Time from PROCCLK↓	0	-10		0	-15		ns	
65-18	-NPCS Delay		26	35			30	ns	
81-3	OSC287 Period	33			33			ns	
82-3	OSC287 Low Time	12			12			ns	
83-3	OSC287 High Time	15			15			ns	
81-3	OSC287 Rise/Fall Time			5			5	ns	
19-4	POWERGOOD Setup Time to PROCCLK↓	26			25			ns	3
	POWERGOOD Hold Time from PROCCLK↓	41			30			ns	3
8-4	POWERGOOD Rise/Fall Times			20			20	ns	
	POWERGOOD Inactive Pulse Width	1			1			μs	
5-2	PROCCLK Delay from X3, X5			35			30	ns	
6-2	PROCCLK High Time	13			11			ns	
7-2	PROCCLK Low Time	11			7			ns	
9-2	PROCCLK Rise/Fall Times			8			4	ns	
22-5	RC Setup Time to SYSCLK↑		30			30		ns	3
23-5	RC Pulse Width	83	15		62			ns	
51-15	-READY Active Delay from PROCCLK↓		14	18			18	ns	
52-15	-READY Inactive Delay		15	60			30	ns	
	REFRDY Pulse Width	40			30			ns	
	REFRDY Setup Time to PROCCLK↓	0			0			ns	
	REFRDY Hold Time to PROCCLK↓	35			35			ns	
74-25	RES 287 Delay from -IOW		8	50			50	ns	
21-4	RES CPU Delay from PROCCLK↓			22			18	ns	
20-4	+RESET Delay from PROCCLK↓		30	50			50	ns	

POACH 7 AC CHARACTERISTICS (Continued)

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

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Symbol -Figure	Parameter	12.5 MHz Min	12.5 MHz Typ	12.5 MHz Max	16 MHz Min	16 MHz Typ	16 MHz Max	Units	Notes
41-12	SA0 Enable Time from CPU HLDA			50			50	ns	
42-12	SA0 Disable Time from CPU HLDA			50			50	ns	4
15-15	S1, S0 Setup Time to PROCCLK↓	22	17		15			ns	
16-15	S1, S0 Hold Time from PROCCLK↓	0	-11		0			ns	
10-2	SYSCLK Delay from PROCCLK↓	5	15	20	5	12	18	ns	
89-28	TEST↑ to Output Disable Time		100			100		ns	
89-28	TEST↓ to Output Enable Time		100			100		ns	
1-2	X3, X5 Period	40			31			ns	
2-2	X3, X5 Low Time	15			12			ns	
3-2	X3, X5 High Time	20			16			ns	
4-2	X3, X5 Rise/Fall Times			5			3	ns	
87-28	XD0 Setup Time to TEST↑	35			35			ns	
88-28	XD0 Hold Time from TEST↑	35			35			ns	
35-8,11	XD0-XD7 Delay Time from -IOR↓			40			30	ns	
36-8,11	XD0-XD7 Hold Time from -IOR↑			15			15	ns	
31-7	XD0-XD7 Setup Time to -IOW↑	83			62			ns	
32-7	XD0-XD7 Hold Time from -IOW↑	0			0			ns	

POACH 8 AC CHARACTERISTICS

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

Symbol -Figure	Parameter	12.5 MHz Min	12.5 MHz Typ	12.5 MHz Max	16 MHz Min	16 MHz Typ	16 MHz Max	Units	Notes
96-37	-8042CS delay from XA_X		40	48			48	ns	
98-38	A17-A23 delay from SYSCLK↑			125			125	ns	
99-38	A17-A23 enable delay from HLDA or -MASTER			83			83	ns	
97-38	A17-A23 disable delay from HLDA or -MASTER			83			83	ns	4
100-39	+ACK delay from HLDA		30	40			40	ns	
101-39	+ACK delay from -MASTER		31	40			40	ns	
109-40	-AEN1, -AEN2 delay from SYSCLK↑		75	115			115	ns	
94-37	CCRSW delay from XA_X			48			48	ns	
102-39	CCRSW delay from HLDA or -MASTER			41			41	ns	
108-40,49	CPU HRQ delay from SYSCLK↑		52	70			62	ns	

POACH 8 AC CHARACTERISTICS (Continued)
(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

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Symbol -Figure	Parameter	12.5 MHz Min	12.5 MHz Typ	12.5 MHz Max	16 MHz Min	16 MHz Typ	16 MHz Max	Units	Notes
95-37	-CS287 delay from XA_X			48			48	ns	
103-39	-CS287 delay from HLDA or -MASTER			41			41	ns	
113-40	-DACK0-3, -DACK5-7 delay from SYSCLK↑		63	100			100	ns	
110-40	-DMAAEN delay from SYSCLK↑		75	120			120	ns	
	-DMAAEN delay from -REFRESH			120			120	ns	
132-42	-DPCK setup time to -XMEMR↑	6			6			ns	
133-42	-DPCK hold time from -XMEMR↑	5			5			ns	
107-40	-DRQ0-3, -DRQ5-7 setup time to SYSCLK↑	0	-18		0			ns	3,7
	HLDA setup time to SYSCLK↑	65	12		62			ns	
	HLDA hold time from SYSCLK↑	0	0		0			ns	
28-7	-INTR1CS, -INTR2CS delay from XA_X		32	41			41	ns	
104-39	-INTR1CS, -INTR2CS delay from HLDA or -MASTER		32	41			41	ns	
134-43	-IOCHCK pulse width		20			20		ns	
130-41	IOCHRDY setup time to SYSCLK↑	25	1		25			ns	
131-41	IOCHRDY hold time to SYSCLK↑	25	6		25			ns	
114-40	-IOR, -IOW active delay from SYSCLK↑ (during DMA transfers)		73	100			100	ns	
115-40	-IOR, -IOW inactive delay from SYSCLK↑ (during DMA transfers)		78	100			100	ns	
116-40	-IOR, -IOW float to inactive delay from SYSCLK↑ (during DMA transfers)		80	100			100	ns	
117-40	-IOR, -IOW inactive to float delay from SYSCLK↑ (during DMA transfers)		130	156			150	ns	4
152-47	-IOW active pulse width (during CPU transfers)	75			62			ns	
137-44	IRQ0 delay from X1		42			42		ns	
	NMI delay from -XMEMR↑		37	83			62	ns	
135-43	NMI delay from -IOCHCK↓		40	83			62	ns	

POACH 8 AC CHARACTERISTICS (Continued)
(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

T-52-33-05

Symbol -Figure	Parameter	12.5 MHz			16 MHz			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
143-45	OSC low time	20			20			ns	
144-45	OSC high time	20			20			ns	
145-45	OSC rise/fall times			15			15	ns	
146-45	OSC delay from X1			24			24	ns	
148-46	-RDXDB inactive delay from -IOR		30	83			62	ns	
149-46	-RDXDB delay from -INTA		45				62	ns	
	REFRDY delay from IOCHRDY	10	25	35	10		35	ns	
157-49	-REFRESH delay from HLDA		15	24			24	ns	
158-49	-REFRESH delay from SYSCLK↑		45	83			62	ns	
	+RESET active pulse width	160			125			ns	
138-44	SPEAKER delay from X1		43			43		ns	
91-36	SYSCLK period	83			62			ns	
92-36	SYSCLK low time	30	13		15			ns	
93-36	SYSCLK high time	30	10		15			ns	
124-40	TC delay from SYSCLK↑		73	100			100	ns	
140-45	X1 low time	30			30			ns	
141-45	X1 high time	30			30			ns	
142-45	X1 rise/fall times			5			5	ns	
150-47	XA_X input setup time to -IOW↑ (during CPU transfers to POACH 8)	83	0		62			ns	
151-47	XA_X input hold time from -IOW↑ (during CPU transfers to POACH 8)	40	20		40			ns	
	XA_X input hold time from -IOR↑ (during CPU transfers from POACH 8)	67	20		62			ns	
111-40	XA_X valid delay from SYSCLK↑ (during DMA transfers)		81	150			150	ns	
159-40	XA_X valid delay from SYSCLK↑ (during REFRESH)		40	75			75	ns	
112-40	XA_X disable delay from SYSCLK↑ (during DMA transfers)		70	130			125	ns	4
153-47	XD_X input setup time to -IOW↑	83	20		62			ns	
153-47	XD_X input hold time from -IOW↑	15	0		15			ns	
155-48	XD_X output delay from -IOR↓		84	100			100	ns	
156-48	XD_X output hold time from -IOR↑	15	35	60	15		50	ns	

POACH 8 AC CHARACTERISTICS (Continued)

(V_{DD} = 5V ± 5%, T_A = 0°C to 70°C)

T-52-33-05

Symbol -Figure	Parameter	12.5 MHz Min	12.5 MHz Typ	12.5 MHz Max	16 MHz Min	16 MHz Typ	16 MHz Max	Units	Notes
125-41	-XMEMR active delay from SYSCLK↑		65	100			100	ns	
126-41	-XMEMR inactive delay from SYSCLK↑		72	100		72	100	ns	
127-41	-XMEMR enable/disable delay from SYSCLK↑		120			120		ns	4
121-40	-XMEMW active delay from SYSCLK↑		42	100			100	ns	
122-40	-XMEMW inactive delay from SYSCLK↑		75	100			100	ns	
123-40	-XMEMW enable/disable delay from SYSCLK↑		120			120		ns	4

Notes:

1. To provide clearly understood information, the complex timing diagrams depict operation in a standard IBM PC AT system design. Combinational logic data paths are shown with less complex timing diagrams. The signal source (POACH, PROCESSOR, LOGIC, etc.) follows the signal name.
2. Typical AC specification values are given for V_{CC} = 5V and T_A = 27°C.
3. This signal is an asynchronous input. The timing specification is provided for testing purposes only to assure recognition at a specific clock edge.
4. The output float or high impedance condition occurs when output current is less than I_{OZ} in magnitude.
5. The frequency of CCROSC sets the count rate for the real time clock. CCROSC frequency, accuracy and stability, should be maintained as close as possible to 32.768Hz to insure the validity of time and date information.
6. Input rise and fall times are assumed to be less than 20ns unless otherwise specified.
7. DRQ_X must be held active with $DACK_X$ is returned.
8. The interrupt request inputs include IRQ0, IRQ3-7, IRQ9-12, IRQ14-15, and +OPT.
9. Address XA_{0-15} are output for byte DMA operations from the DMA controller in POACH 8, with XA_{16-23} from the memory mapper. Address XA_{1-16} are output from the POACH 8 DMA controller for word DMA operations, with XA0 low and XA_{17-23} from the POACH 8 memory mapper.
10. A minimum of 16 PROCCLK cycles must occur before POWERGOOD becomes valid.

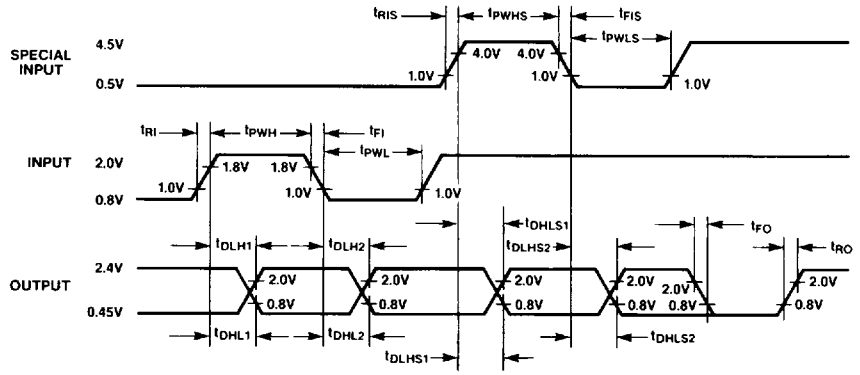

Figure 1A. Delay Time and Pulse Width Measurements

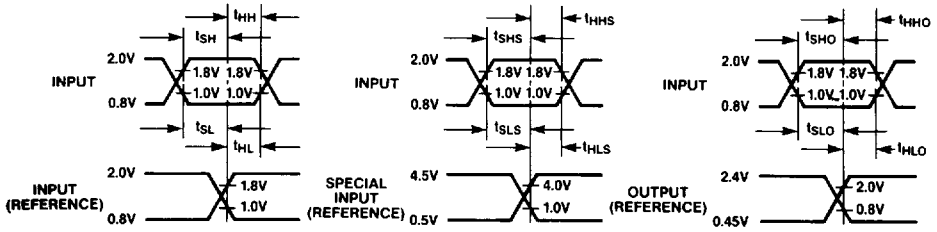

Figure 1B. Setup/Hold Time Measurements

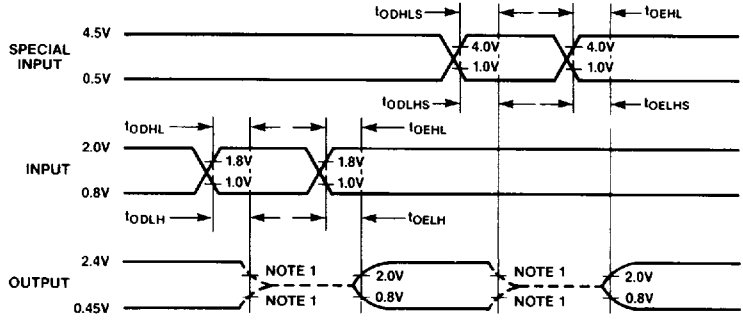

Figure 1C. Output Enable/Disable Time Measurement

Figure 1. AC Measurement Points

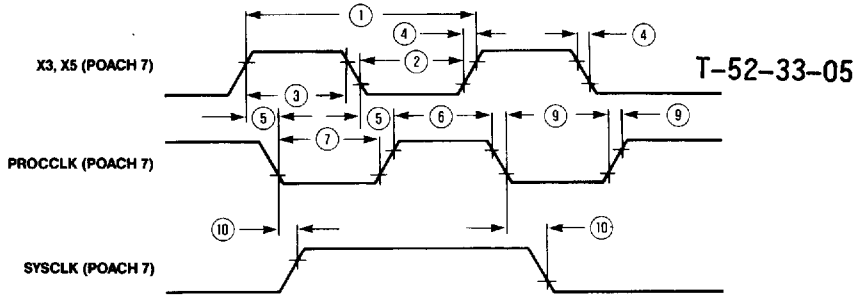

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Figure 2. POACH 7 Clock Timing

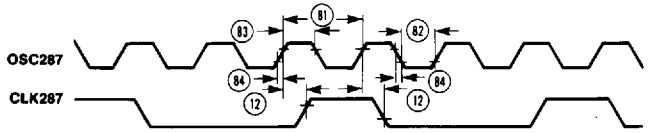


Figure 3. POACH 7 80287 Clock Timing

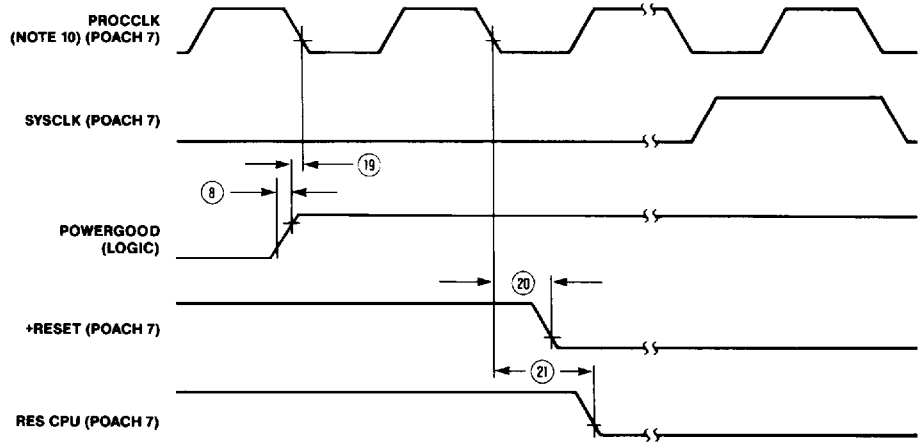


Figure 4. POACH 7 Power on Initiated Reset

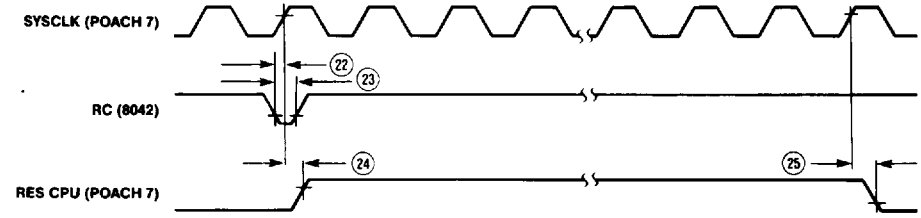


Figure 5. POACH 7 Keyboard Initiated Reset

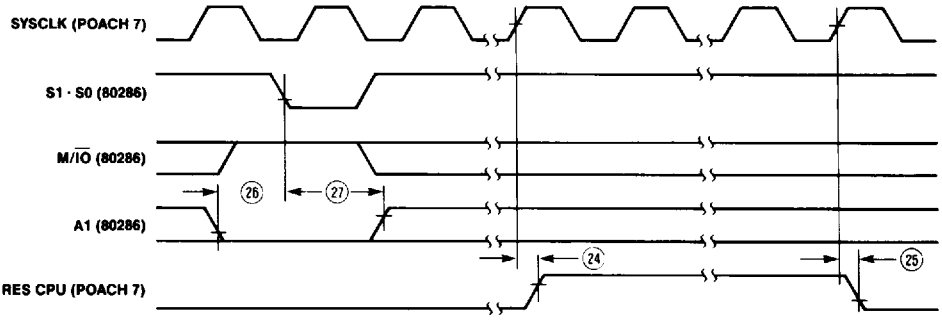


Figure 6. POACH 7 Processor Shutdown Initiated Reset

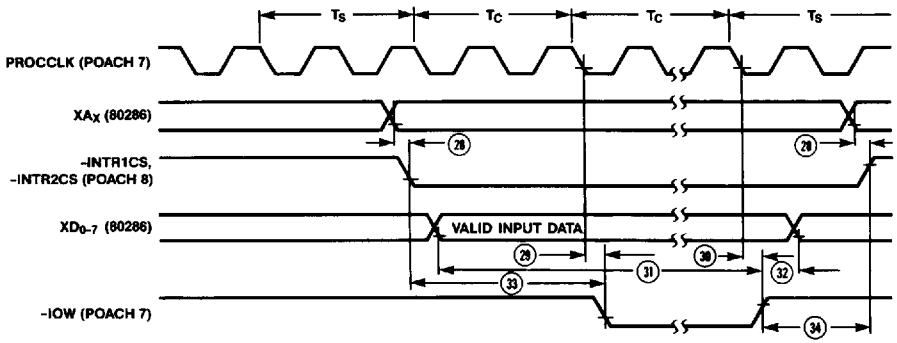


Figure 7. POACH 7—8259 Bus Write Timing

T-52-33-05

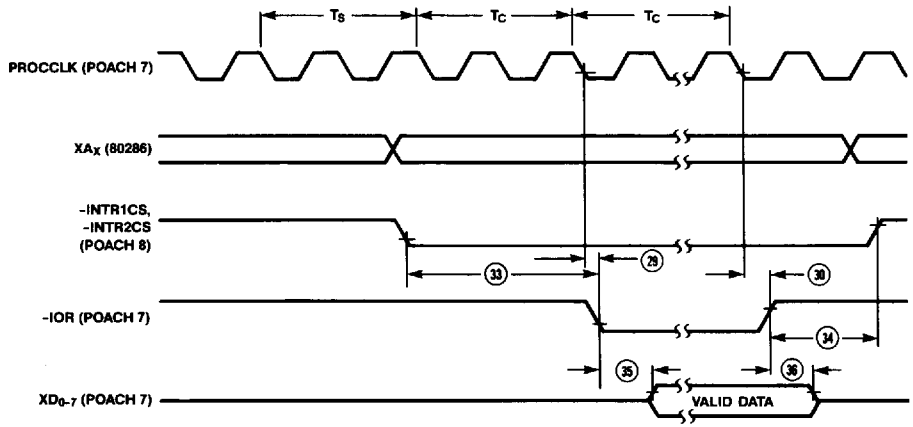


Figure 8. POACH 7—8259 Bus Read Timing

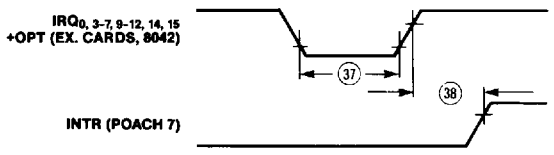


Figure 9. Interrupt Request Timing

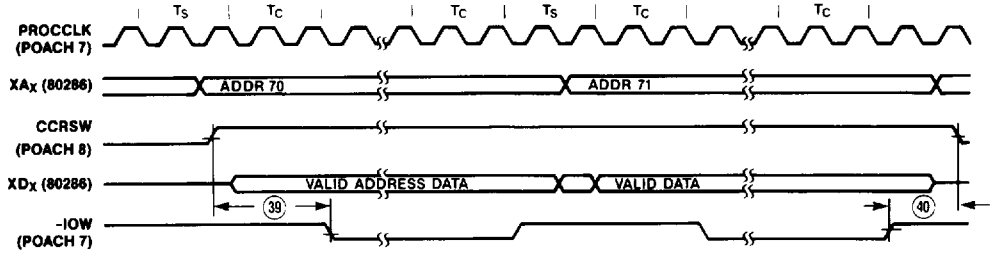


Figure 10. POACH 7 6818 Write Cycle

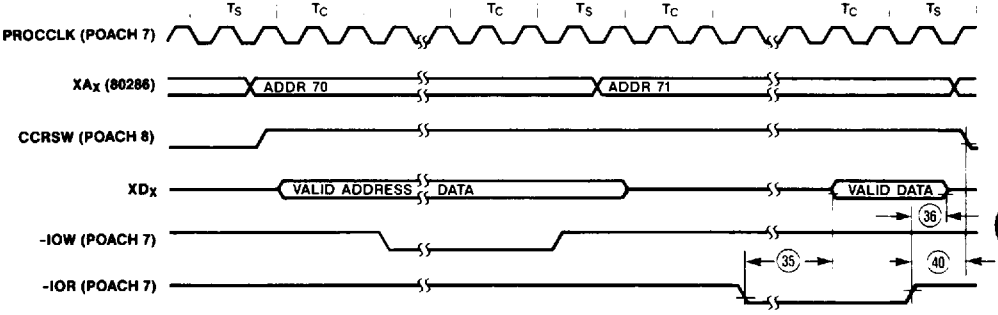


Figure 11. POACH 7 6818 Read Cycle

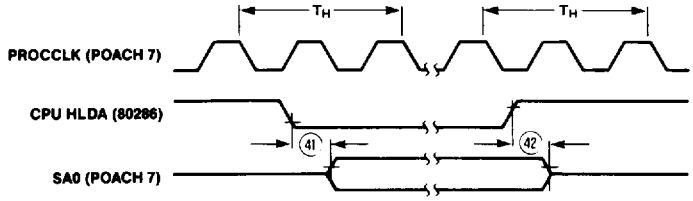


Figure 12. POACH 7 SA0 Timing

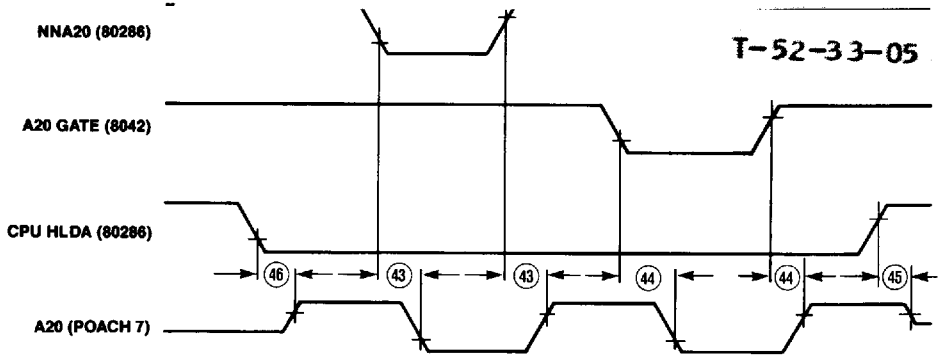


Figure 13. POACH 7 A20 Timing

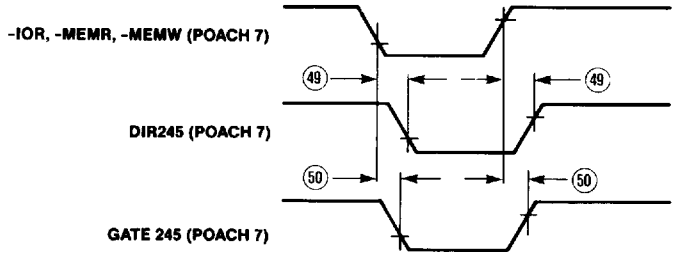


Figure 14. POACH 7 DIR245, GATE245 Timing

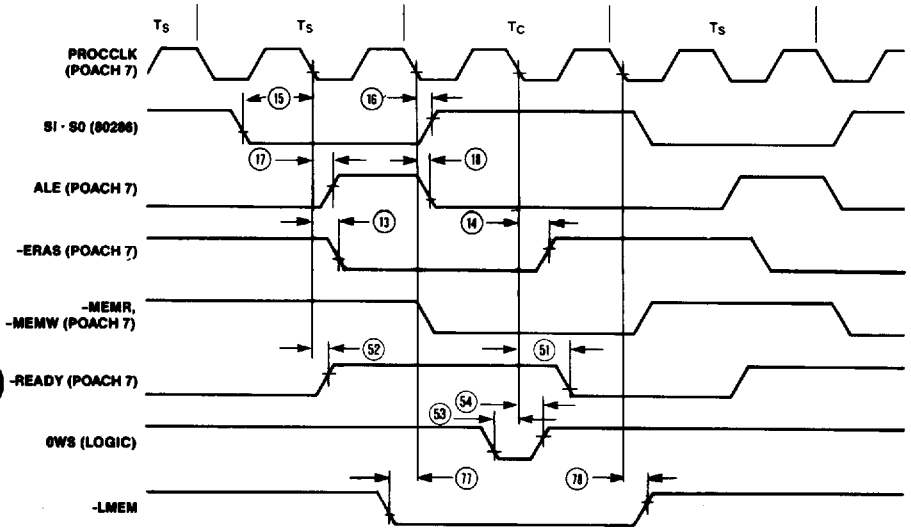


Figure 15. POACH 7 Zero Wait State Timing

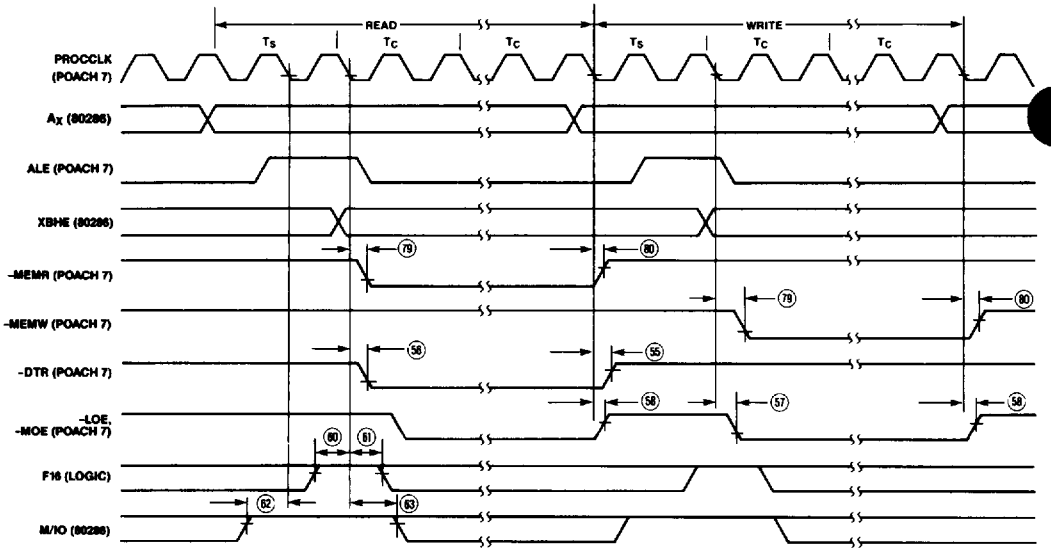


Figure 16. Memory Read/Write Cycles

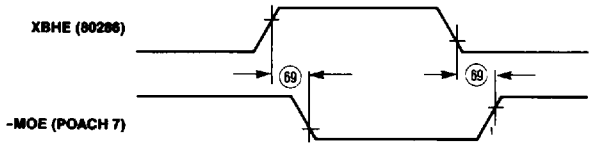


Figure 17. POACH 7 XBHE Timing

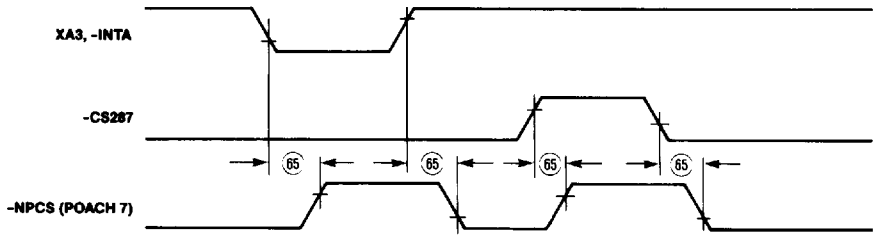


Figure 18. POACH 7 NPCS Timing

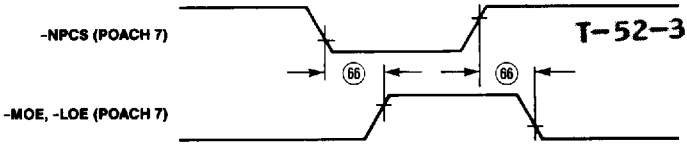


Figure 19. POACH 7 -MOE, -LOE Timing

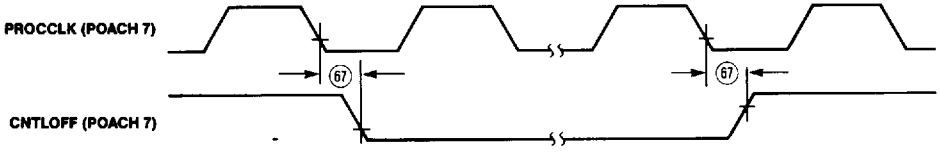


Figure 20. CNTLOFF Timing

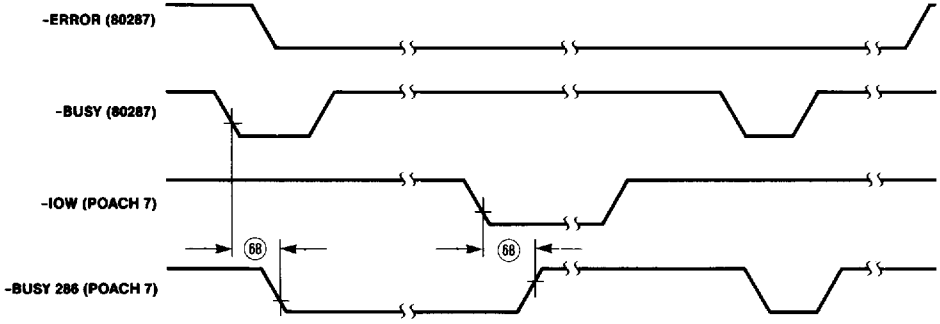


Figure 21. -BUSY286 Timing

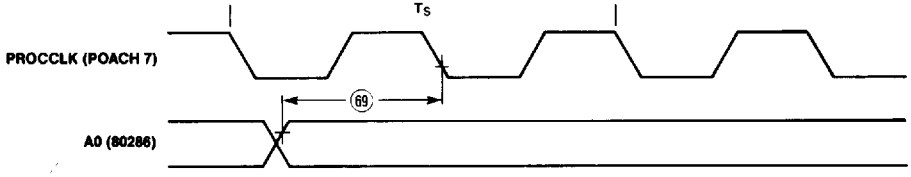


Figure 22. POACH 7 A0 Timing

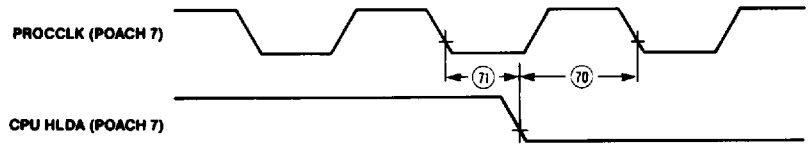


Figure 23. POACH 7 CPU HLDA Timing

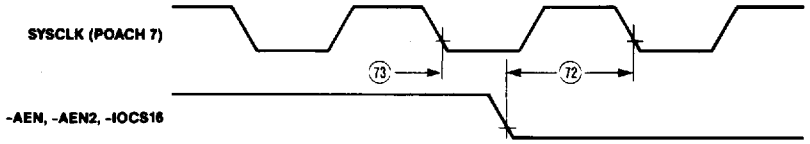


Figure 24. Bus Control Signal Timing

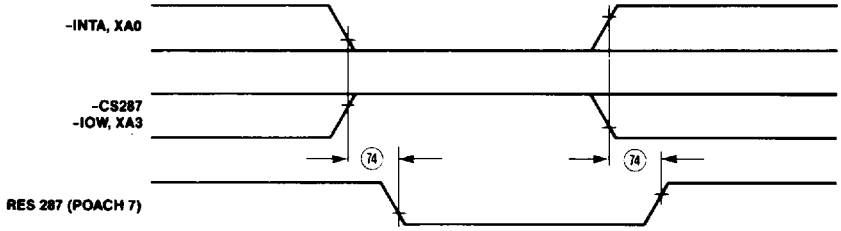


Figure 25. RES 287 Timing

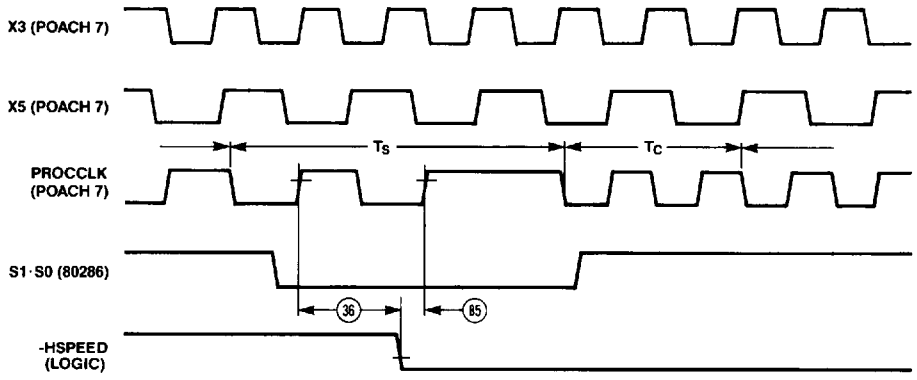


Figure 26. POACH 7 X5 (Low) to X3 (High) Speed Switching

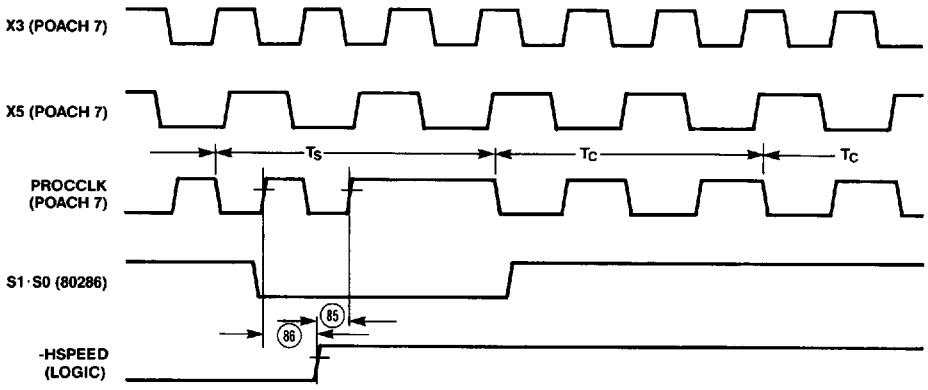


Figure 27. POACH 7 X3 (High) to X5 (Low) Speed Switching

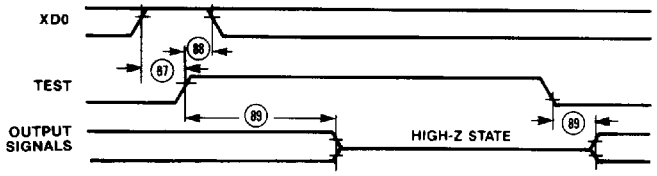


Figure 28. POACH 7 Test Mode Timing

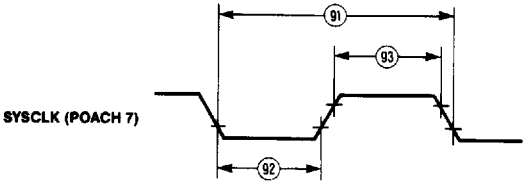


Figure 36. POACH 8 SYSCLK Timing

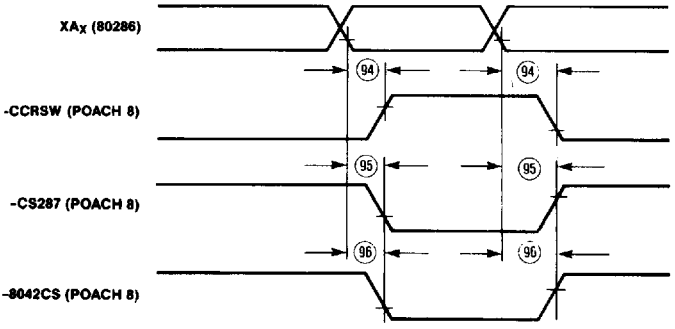


Figure 37. POACH 8 CCRSW and CS287 Timing

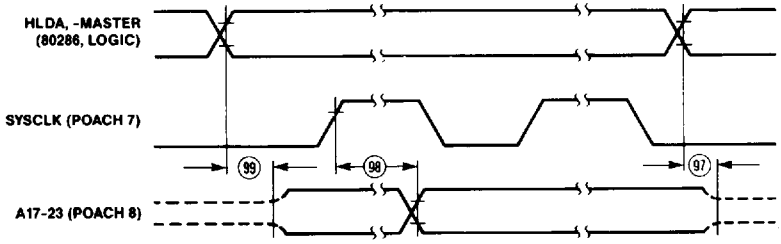


Figure 38. POACH 8 A17 to A23 Timing

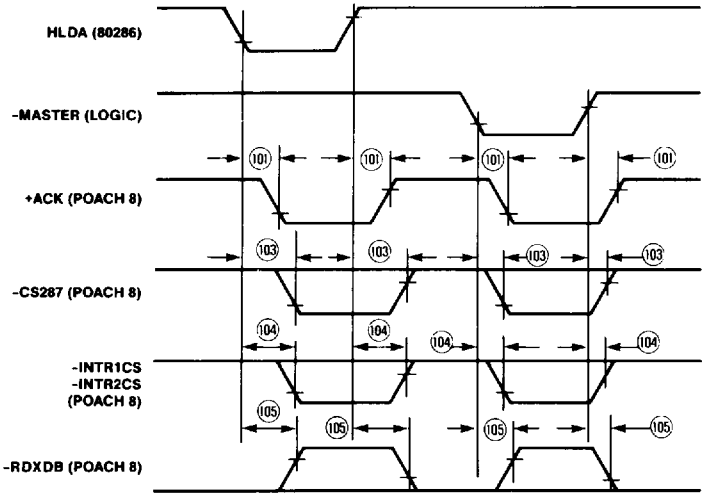


Figure 39. POACH 8 HLDA and -MASTER Timing

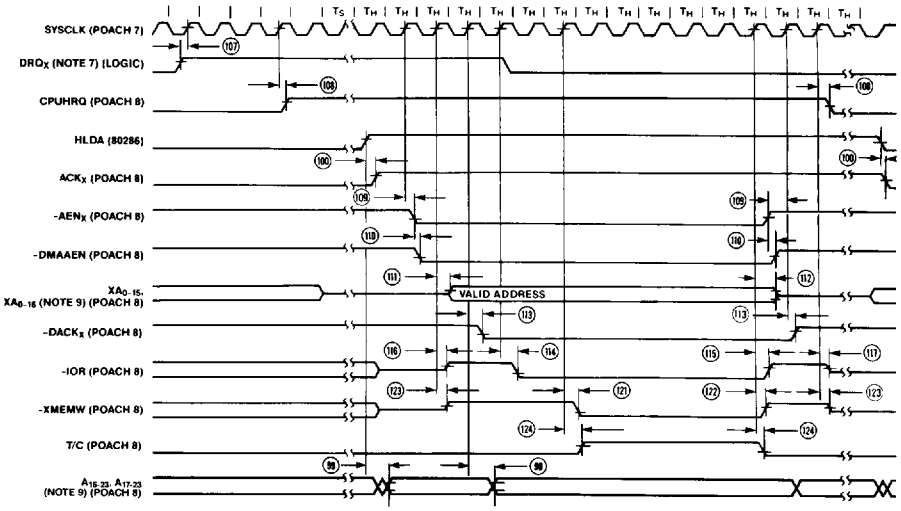


Figure 40. POACH 8 DMA I/O Read Timing (Single Transfer Shown)

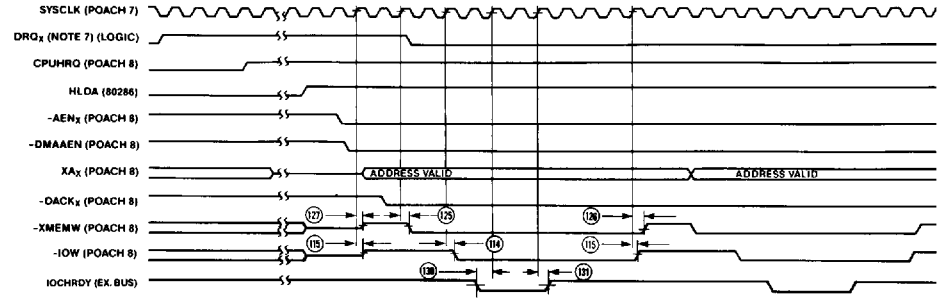


Figure 41. POACH 8 DMA I/O Write Timing (Block Transfer with Extension Shown)

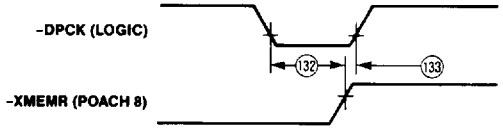


Figure 42. POACH 8 DPCK Timing

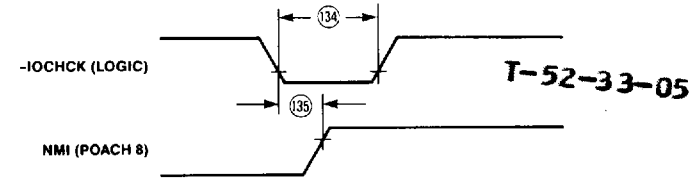


Figure 43. POACH 8 IOCHCK and NMI Timing

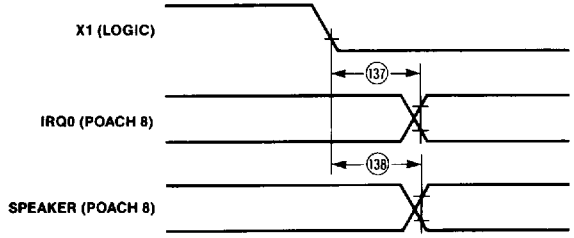


Figure 44. POACH 8 IRQ0 and SPEAKER Timing

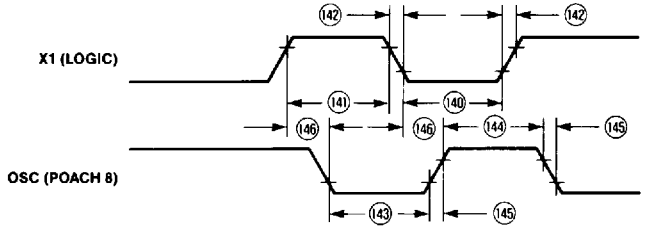


Figure 45. X1 and OSC Timing

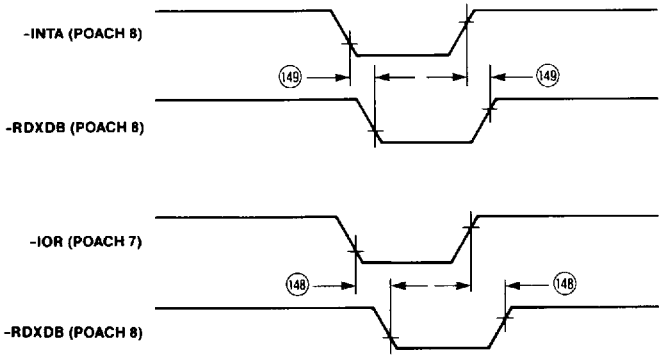


Figure 46. POACH 8 RDXDB Timing

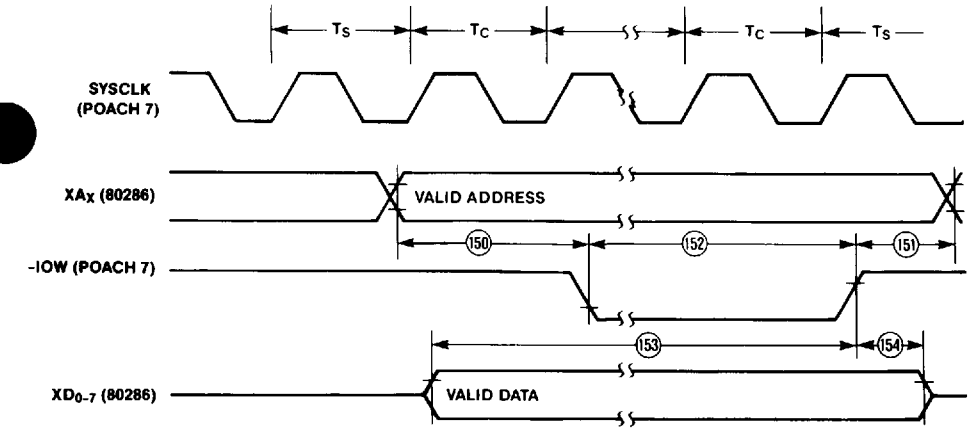


Figure 47. POACH 8 CPU Write Timing

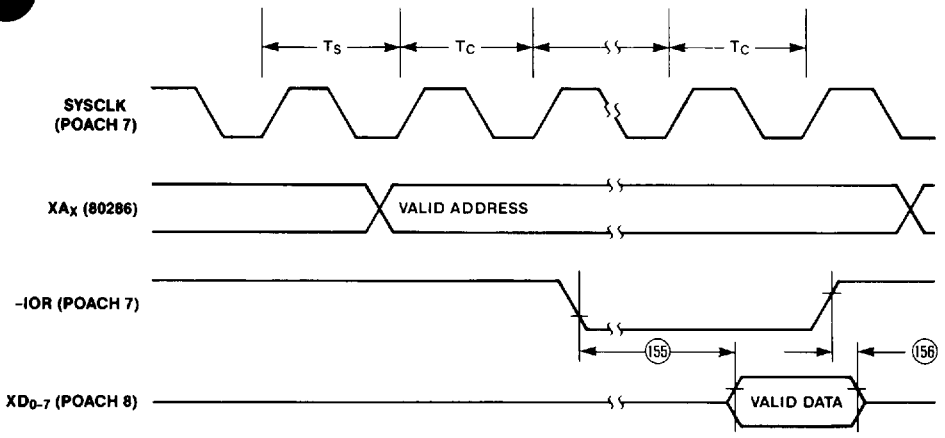


Figure 48. POACH 8 CPU Read Timing

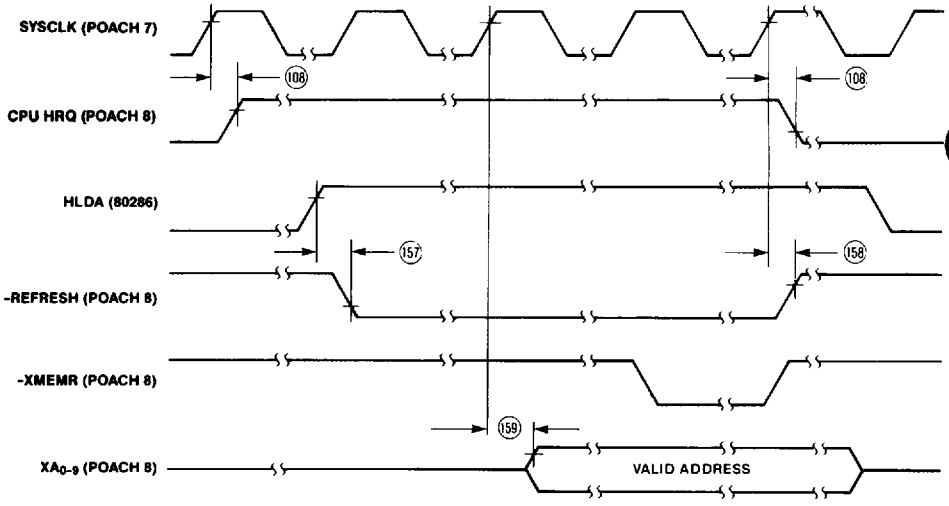
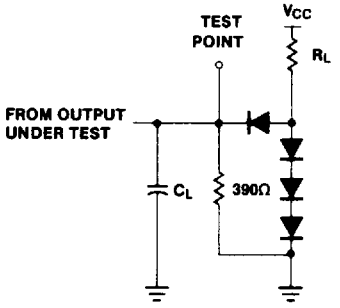
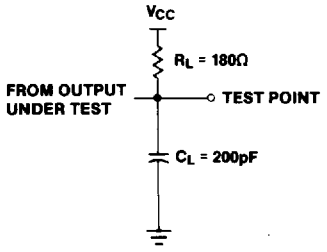


Figure 49. POACH 8 REFRESH Timing

TEST LOADS



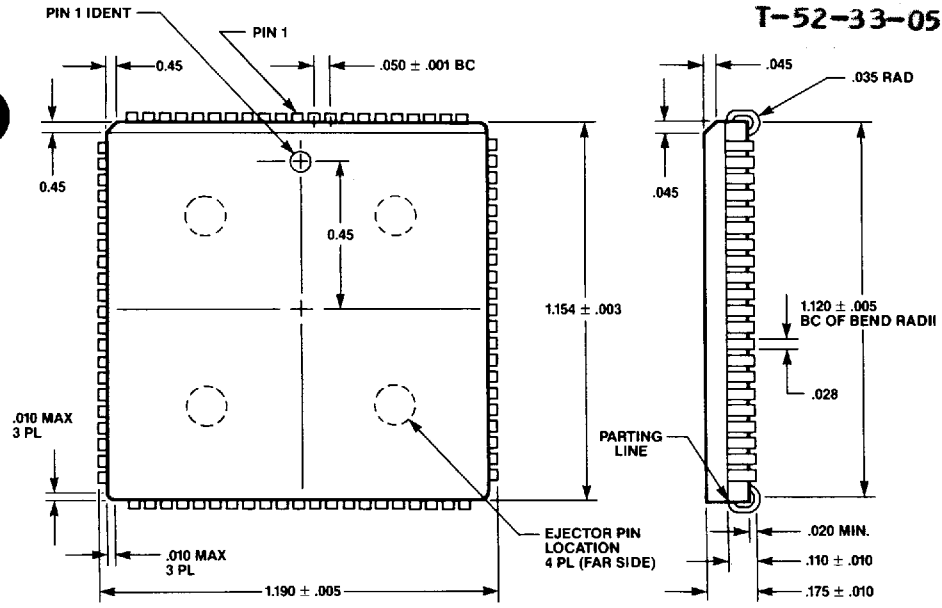
Output Load Circuit



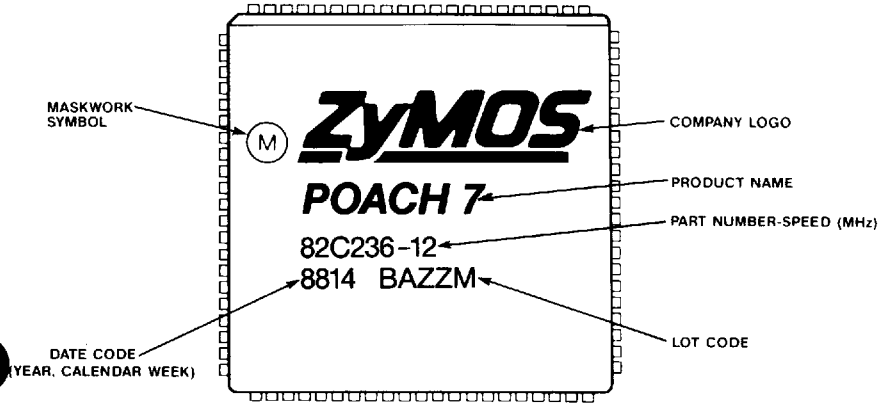
Load Circuit for Open-Collector Output

C_L = 50pF, R_L = 620 ohms for all outputs except the following.
C_L = 50pF, R_L = 180 ohms for:

POACH 7 pins	PROCCLK	-MEMR
	-IOR	-MEMW
	-IOW	INTA
	SA0	ALE
	SYSCLK	-ERAS
POACH 8 pins	-IOR	OSC
	-IOW	



84-PIN PLCC PACKAGE DIMENSIONS



MARKING DETAILS